S E R V I C E N O T E

SUPERSEDES: None

E4430A (ESG-D1000A) RF Digital Signal Generator
E4400-60043 UN3 - A8 1 Meg Data Generator Assembly
E4400-60057 UN4 - A8 8 Meg Data Generator Assembly

Serial Numbers: US37040000 / US37239999 GB37040000 / GB37239999

Corrects PHS Frame Trigger Errors for Options UN3/4

Duplicate Service Notes:

E4431A-02 US37040000 / US37239999 - GB37040000 / GB37239999
E4432A-02 US37040000 / US37239999 - GB37040000 / GB37239999
E4433A-02 US37040000 / US37239999 - GB37040000 / GB37239999

To Be Performed By: Agilent-Qualified Personnel or Technical Customer

Parts Required:

P/N	Description	Quantity
E4400-60147	Option UN3/4 PHS Modification Kit	1 ea.

Continued

DATE: April 1998

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

MODIFICATION AVAILABLE

ACTION CATEGORY: AGREEABLE TIME		☐ PERFORMANCE ENHANCEMENT ■ SERVICE/RELIABILITY ENHANCEMENT
LOCATION CATEGORY:	■ CUSTOMER INSTALLABLE ☐ ON-SITE ■ SERVICE CENTER	AVAILABLE UNTIL: Product's support life
AUTHOR: AS	ENTITY: 5320	ADDITIONAL INFORMATION: For S/N US/GB 37239999 & I below, Agilent will pay costs.

Agilent Technologies

Situation:

Condition 1 -- No REF or BIT CLK lock available between DUT & Sig. Gen.

For the Device Under Test (DUT), when a 10 MHz Reference, BIT CLK or Symbol CLK output from DUT is NOT available to sychronize and lock the Sig Gen BIT CLK frequency to the DUT BIT CLK. The DUT and the Sig. Gen. will have slightly different BIT CLK rates.

Condition 2 -- Sig. Gen. is in Frame Generation and is Externally Triggered by the DUT

When the frame trigger output from the DUT is used to sychronize the Sig. Gen's. frame generation in the Sig. Gen's. Ext Frame Trig Mode (with or without delay enabled).

Description of Fault:

The Sig. Gen's. Frame Generation re-synchronizes with the EXT Frame Trigger Input on the Sig. Gen. BIT CLK boundaries. Due to the frequency difference (stated above) the phase change will cause the Sig. Gen's. frame synchronization to periodically reset ± 1 BIT CLK period. This ± BIT CLK period jump can cause the DUT's Demodulation or Recovery circuits to lose symbol sychronization and BIT Errors will occur until symbol sync is re-established in the DUT.

Typically during Bit Error Rate Test (BERT), under the above conditions, there will be periodic bursts of BIT errors at the point in time where the Sign. Gen. jumps ± 1 BIT CLK period during External Frame Triggering. The period of the BERT error burst depends on the frequency difference between the Sig. Gen. and the DUT, i.e. how long the phase change takes to accumulate one BIT CLK period of difference. This rate can be increased by modifying the Sig. Gen's. BIT Rate to increase frequency difference between the Sig. Gen and DUT.

NOTE:

Installing this kit may, depending on the firmware previously installed in the instrument, change the User Insterface (UI). The UI differences are due to instrument feature evolution which is currently supported by the new firmware and may become functional as a result of the installation of the PHS kit.

Solution / Action:

Installing the PHS Modification Kit will require the installation of a new DSP Configuration ROM (U203), on the A7 Data Generator Board, and a upgrade of the firmware to the appropriate revision.