

MODIFICATION RECOMMENDED –
CORRECTS MANUFACTURING OR DESIGN DEFECTS

86130A-02A

S E R V I C E N O T E

Supersedes:
86130A-02

86130A BitAlyzer and Error Performance Analyzer

Serial Numbers: US40480393 and earlier

2.13GHz PLD Reprogram PG and ED I/O PLD U7 to allow instrument to operate error-free at 2.13GHz.

To Be Performed By: Agilent-Qualified Personnel

Parts Required:

P/N	Description	Qty.
86130-80040	PG PLD Code - U7	1
86130-80029	ED PLD Code – U7	1

No hardware parts required, only Programmable Logic Device (PLD) code.

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:			
MODIFICATION RECOMMENDED			
ACTION CATEGORY:	<input type="checkbox"/> IMMEDIATELY <input type="checkbox"/> ON SPECIFIED FAILURE <input checked="" type="checkbox"/> AGREEABLE TIME	STANDARDS: LABOR: 2.0 Hours	
LOCATION CATEGORY:	<input type="checkbox"/> CUSTOMER INSTALLABLE <input type="checkbox"/> ON-SITE <input checked="" type="checkbox"/> SERVICE CENTER	SERVICE INVENTORY: <input type="checkbox"/> RETURN <input type="checkbox"/> SCRAP SEE TEXT	USED PARTS: <input type="checkbox"/> RETURN <input type="checkbox"/> SCRAP <input type="checkbox"/> SEE TEXT
AVAILABILITY:	PRODUCT'S SUPPORT LIFE AGILENT RESPONSIBLE UNTIL: Product's Support Life		
AUTHOR: RBS PRODUCT LINE: PL8F, 5340			
ADDITIONAL INFORMATION: Factory Reference: SoCo PCO64548 and ATM# 3Gig_Caliber.24			

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March 24, 2003

Latest PLD code is available from 86130A Support page:

http://lwd.marketing.agilent.com/Service_Support/Product_Support/86130a/PLD%20Code%20-%20Current/PLD_Code_Current.htm or contact Support Engineer for assistance.

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Situation:

Early shipments of 86130A would not operate error-free at 2.13GHz (+/- 10MHz) due to a Vitesse MUX reset problem. Instrument will not Auto-Align when connected back-back (no customer DUT). Affects customers who are working at data rates around 2x FibreChannel. Operation elsewhere is not affected.

Solution/Action:

This fix is a firmware-only fix however the instrument must be disassembled, reprogrammed, and retested at a qualified Agilent Service location.

Step 1. IDENTIFY the Problem

* **MANUAL** process to identify the problem:

Identify existence of problem by setting up 86130A back-back operation:

1. PG Data Out to ED Data In, and PG Clock Out to ED Clock In
2. Press Instrument Preset
3. Change Freq = 2.13GHz
4. Turn on Data and Clock amps.
5. Press Auto-Align.

If instrument does not Auto-align within a few seconds (still has Sync Loss and Error indicators ON), it requires new PLD fix.

* **AUTOMATED** process to identify the problem:

The automated BERT Test Station code has been modified to detect this problem:
Test 8.4 will FAIL at 2130 MHz if the correct PLD is not programmed.

Step 2. CORRECT the Problem

* **Service Strategy** to correct the problem:

Using the Altera Programming SW program installed on the BERT Test Station and the ByteBlaster programming cable, follow the 'Programmed Parts' instructions in the 86130A Service Guide to reprogram the PLDs:

- On PG Tray (PG Digital Board 86130-60003), update U7 PLD code with 86130-80040 or later.
- On ED Tray (ED Digital Board 86130-60006), update U7 PLD code with 86130-80029 or later.

Following programming, confirm proper error-free operation by re-running either the MANUAL or AUTOMATED tests above.

END.