Agilent PN 8791-5

Tips on External Clock Operation with FASS

Product Note

Abstract

This product note provides helpful tips and examples of external clock operation with the Agilent Technologies 8791/10 Frequency Agile Signal Simulator. Examples of successful external clock operation are considered in the context of two real applications: secure communication receiver test and radar target simulation.

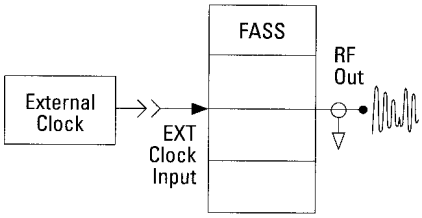

Figure 1. External clock operation with FASS

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Introduction

Standard operation of Agilent Technologies FASS uses an internal clock of 134.217728 MHz (2^{27} Hz) to provide synthesized frequency resolution of 0.125 Hz nominal. This power-of-two timebase was selected to provide "convenient" frequency resolution when used with the direct digital synthesizer inside FASS. Because the direct digital synthesizer uses a binary phase accumulator, any timebase other than a power-of-two would result in an awkward frequency resolution.

The tradeoff here is that the power-of-two timebase—while providing a convenient frequency increment—has a non-power-of-ten reciprocal timing interval. Specifically, the 2^{27} Hz clock yields a nominal system sampling period of $1/2^{27}$ seconds, giving roughly 7.45 ns data resolution. For most applications, this timing resolution is of little consequence, hence the FASS internal clock can be used directly.

However, there are some applications where exact timing is critical, particularly in many radar and secure communication simulations where trigger jitter or timing skew between the simulator and the D.U.T. may be intolerable. In such cases, the FASS can be successfully synchronized to the system under test by using a suitable external clock source. Of course, there are certain ramifications of external clock operation that must be understood before one can proceed without consequence. Some of these issues concern the range of valid clock operation, triggering and synchronization, effect of external clocks on spectral purity, and possible residual Doppler drift. We will examine these effects along with two practical application examples in communications and radar.

System Clock Fundamentals

Let's begin by understanding how FASS clocks are distributed. Figure 2 shows a block diagram of the system clocks where CLK represents the system clock, whether internal or external.

When you are using the standard INTERNAL system clock, connect the 134.217728 MHz signal, CLK OUT (134 MHz), from the Agile Upconverter (AUC) to the EXT CLK INPUT of the Agile Carrier Synthesizer (ACS).

To use an EXTERNAL user-supplied clock, you must input the clock into the EXT CLOCK INPUT of ACS. For specified operation, the clock must not exceed these conditions:

- Frequency: 120 to 140 MHz
- Power Level: 0 to 10 dBm

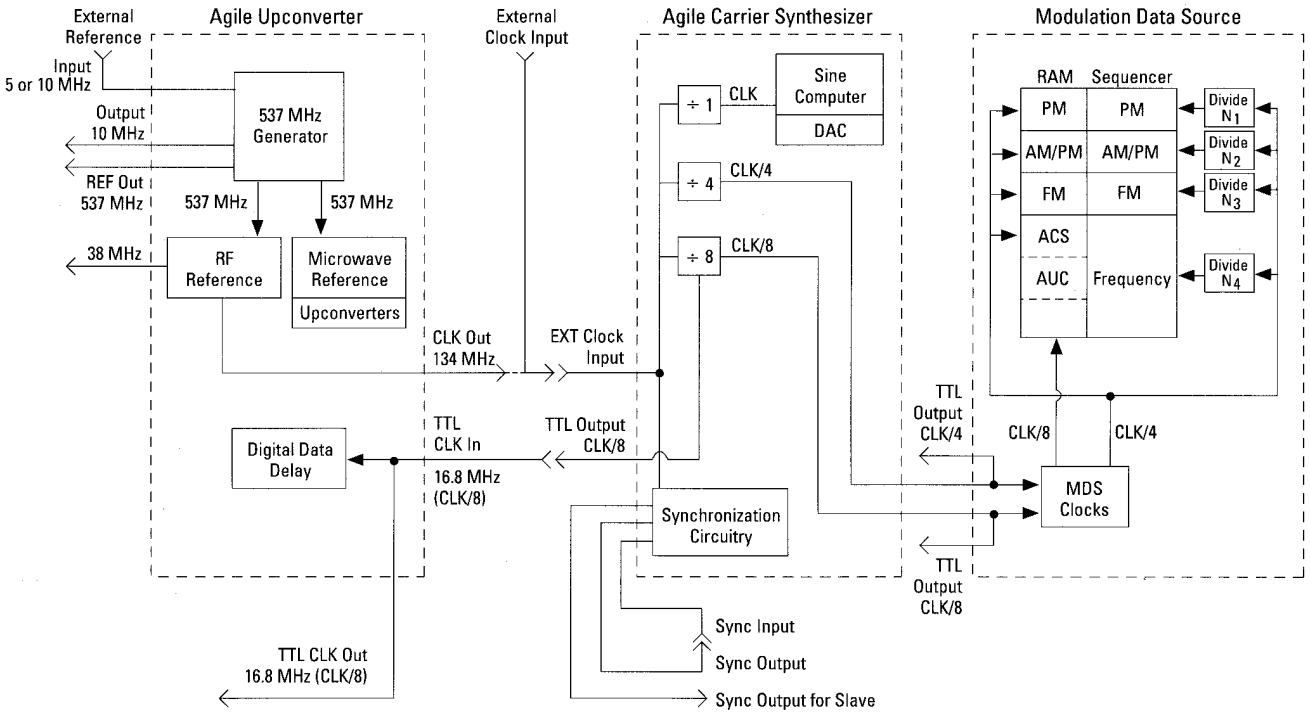

Figure 2. System clock distribution

Once an external clock frequency is chosen and connected to FASS, ACS divides the clock into CLK, CLK-4, and CLK/8 signals which drive the ACS, MDS, and Direct Digital Delay circuitry.

Although the specified external clock frequency range is 120 to 140 MHz, optimal signal performance is obtained by using a 134.217728 MHz clock. Figure 3 shows worst-case spur performance for three different CW signals given an external clock ranging from 110 MHz to 160 MHz. The consistent increase in spur level on either side of the 134 MHz clock results from factory spur optimization at the standard 2^{27} internal clock frequency. These spurs could be optimized for your specific clock frequency by following a special calibration procedure. Consult your Agilent representative for assistance if you require more information.

Note also that Agilent FASS may successfully operate beyond the 120 to 140 MHz external clock range, however such operation is not tested at the factory and, therefore, is not guaranteed or recommended. The system used for this particular example worked reliably from 100 MHz to nearly 160 MHz. Other units have been observed to operate over a lesser range, depending on the particular batch of digital boards inside the system. Operation at unspecified clock frequencies will not damage FASS, however you may not get the signal you expect. Please consult with Agilent if you have any questions regarding this matter.

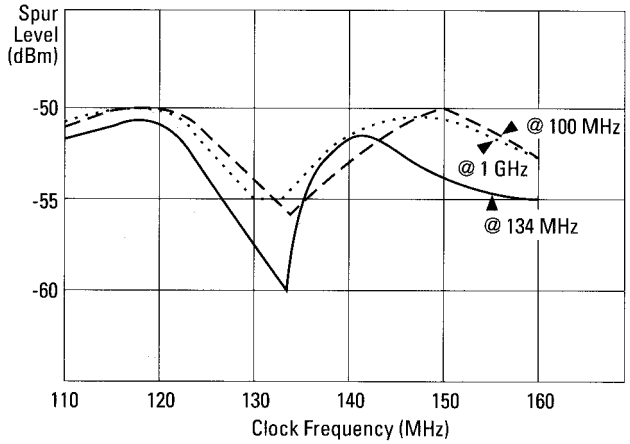

Figure 3. Spectral purity at 134 MHz using various external clocks

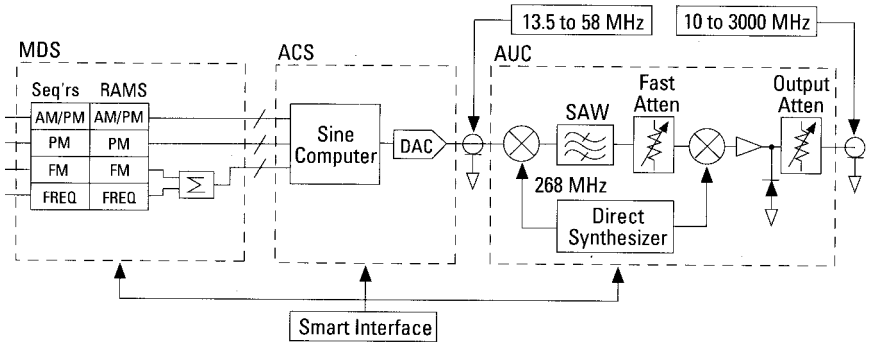

Figure 4. Simplified FASS block diagram

As alluded to above, the external clock drives most, but not all, of FASS. Thus, it is important to note the following rule:

ACS AND AUC DO NOT NECESSARILY RUN OFF THE SAME CLOCK.

In external clock mode, ACS uses external clock signals to perform calculations and latch data while AUC uses its internal standard reference clocks and oscillators. This results from a design restriction of the AUC which is a direct synthesizer/upconverter. For optimal performance, AUC uses filters with bandwidths of 2% or less. These narrow bandwidths are necessary to minimize spurs. However, wider bandwidths are necessary to accommodate the mixed signals which would result from the LO dependency on an external clock. For instance, if the 268 MHz LO in AUC (a LO used for upconversion referenced in Figure 4) were varied by 10% then mixed with the instantaneous signal from ACS, the resultant signal would not be in the bandpass of the SAW filter! (See section 6 of Product Note 8791-3 *"Theory of Operation for the 8791 Model 10 Frequency Agile Signal Simulator"* for more information on AUC system theory.)

Programming Considerations

An important point to consider is that when using a non-standard clock you must account for any frequency offsets when programming the system. Table 1 summarizes the effects of an external clock on FASS modulation types.

FREQ RAM Data. Data loaded into the FREQ RAM must be divided into an ACS frequency and an AUC band. Normally, the ACS frequency is a baseband frequency of 33.554432 MHz (2^{25} Hz) plus an offset ranging from 0 to 4 MHz for fine-tuning the carrier frequency with 0.125 Hz resolution. The AUC band tells the AUC which frequency band to engage.

Using an external clock requires that you scale the ACS data (by 2^{27}/EXTCLK) before downloading to the FREQ RAM. Since AUC does not use the external clock, its values do not have to be scaled. For your convenience, lines 160 through 180 of the BASIC code shown in Figure 5, illustrate how to calculate the proper ACS and AUC values for any clock frequency. Note that line 180 is necessary to account for the architecture of the phase accumulator which has a minimum frequency resolution of 0.125 Hz.

Figure 6 shows the results calculated by the BASIC code shown in Figure 5 using the following inputs:

- Desired output frequency = 1 GHz
- External clock frequency = 120 MHz

```
10                          ! BASIC PROGRAM CALCULATES ACS, AUC VALUES FOR SETTING
20                          ! A FREQUENCY IN HP FASS USING A VARIABLE EXTERNAL CLOCK.
30                          ! IF AN EXTERNAL CLOCK IS NOT USED, SIMPLY SET F_clock = 2^27 Hz
40                          !
50                          ! INPUTS:   F_desired = desired output frequency
60                          !           F_clock   = external clock frequency
70                          ! OUTPUTS: F_actual = actual output frequency
80                          !           ACS = value to load into ACS memory field
90                          !           AUC= value to load into AUC memory field
100                         !           Frequency Error = F_actual - F_desired
110                         !
120 F_desired=1.E+9         ! User-selectable value between .01 and 3 GHz
130 F_clock=1.20E+8         ! User-selectable value typically between
140                         ! 120 and 140 MHz.
150                         !
160 Auc=INT(F_desired/2^22)
170 Acs=[F_desired-(Auc-8)*2^22]*2^27/F_clock
180 Acs=[INT(8*Acs+.5)]/8   ! accounts for phase accumulator freq resolution
190                         ! and rounds to nearest fractional value
200                         !
210 F_actual=[Acs*(F_clock/2^27)+(Auc-8)*2^22]
220 PRINT "F_desired = " ;F_desired
230 PRINT "F_actual = " ;F_actual
240 PRINT "F_clock = " ;F_clock
250 PRINT "Frequency Error (Hz) = " ;F_actual-F_desired
260 PRINT
270 PRINT "Program AUC band = " ;Auc
280 PRINT "Program ACS frequency = " ;Acs
290 END
```

Figure 5. BASIC code used to calculate ACS and AUC values for external clock operation

Table 1. Effects of an external clock on modulation deviations.

	Correction
AM	No effect
PM	No effect
FM	Scale data by 2^{27}/EXTCLK before loading into memory
ACS	Scale data by 2^{27}/EXTCLK before loading into memory
AUC	No effect
FLC	No effect
PULS	No effect

```
F_desired = 1.E+9
F_actual = 1.00000000005E+9
F_clock = 1.2E+8
Frequency Error (Hz) = .0514221191406

Program AUC band = 238
Program ACS frequency = 3.9493656E+7
```

Figure 6. Frequency calculations based on a desired output frequency of 1 GHz and an external clock frequency of 120 MHz

The actual output frequency is calculated in line 210. As expected, this value is slightly higher than the desired frequency—by +0.05 Hz. This is due to the clock shift of the phase accumulator in ACS FM RAM data. Data from the FM and ACS memory fields combine in the MDS before being passed to the phase accumulator in ACS. Thus, the FM data must also be scaled by the internal clock divided by the external clock frequency (2^{27}/CLK).

How to Calculate Frequency Resolution

The following equation demonstrates how to calculate frequency resolution for any clock frequency:

- Freq_res = CLK_freq/2^{30}

This is the frequency resolution of a 30-bit phase accumulator. When using the internal clock, frequency resolution is given by $2^{27}/2^{30} = {}^{1}/_{2}{}^{3}$ or 0.125 Hz.

WGL Considerations

The Agilent 11776K Waveform Generation Language Software (WGL) assumes a clock frequency of 134 MHZ at start-up. This clock frequency affects commands such as FASSFREQ, FREQ, HZ, INHZ, SECS, and INSECS. Thus, when using a non-standard clock frequency, you should set the WGL clock to your external clock frequency using the command CLOCK. Although FASSFREQ conveniently calculates the proper values to load into the ACS and AUC memory fields for setting CW frequencies, there is no command which automatically scales FM data. FM data must be scaled by 2^{27}/CLK, otherwise modulation bandwidth compression or expansion will occur.

This is also true when using Instrument-on-a-Disk software such as RSID (Radar Simulator). That is, when using an external clock, you must artificially compensate for this when setting FM deviation. Carrier frequency is automatically corrected.

Sequencer Limitations

Sequencer limitations such as

1. number of packets
2. wave segment length (by points)
3. minimum points in segment, and
4. minimum points scanned

remain the same regardless of the clock frequency used. However, since each point represents a sampling period which is clock dependent, dwell times for sequencer characteristics 2 through 4 above will differ for different clock frequencies. To calculate dwell time, simply divide the number of points you are using by your clock frequency.

Dynamic Data

All dynamic data characteristics remain the same regardless of the clock frequency used. See Chapter 5 “Specifications and Limitations” of Product Note 8791-1 *“Using Dynamic Data with FASS”* for more detail regarding the characteristics of synchronous and asynchronous dynamic data operation.

Secure Communications Example

Most secure communication systems derive their clocks from 5 or 10 MHz crystal references. For example, as described in PN 8791-4, the JTIDS and PLRS systems both operate with a 5 MHz data rate yielding a 200 ns chip width. To avoid inadvertent data dropouts and possible timing skew during a simulation, it is advisable to operate FASS from an external clock whose fundamental period is, in this example, an integral submultiple of 200 ns (or integral multiple of 5 MHz). Because FASS is specified to operate over a 120 to 140 MHz range, the 120 MHz clock is chosen, giving a fundamental period of 1/120 MHz, or 8.33 ns. Because 8.33 ns divides wholly into 200 ns, synchronism with the device under test is then possible. Table 2 provides a useful reference for determining clock frequencies to obtain a given timing resolution. Figure 7 shows the output of the FASS generating a secure communication signal used to test a PLRS (Position Location Reporting System) radio. The signal is MSK (Minimum-Shift Keying) with a 5 MHz data rate and a 2.5 MHz p-p frequency toggle.

Note in this example that because the external 120 MHz clock controls the direct digital synthesizer, and not the agile upconverter (AUC), the final output frequency of FASS will no longer have 0.125 Hz resolution. For most applications, this is of little consequence as you will be able to program any frequency with a worst-case error of $\pm 1/16$ Hz, typically.

Table 2. Timing resolution for given clock frequencies

CLK FREQ MHz	Period ns	MIN Trigger INT ns	Common µS RES	Other Convenient Values
110	9.0909	72.727	4	
111	9.009	72.072	8	
112	8.9286	71.429	1	0.500 µs
113	8.8496	70.796	8	
114	8.7719	70.175	4	
115	8.6957	69.565	8	
116	8.6207	68.966	2	
117	8.547	68.376	8	
118	8.4746	67.797	4	
119	8.4034	67.227	8	
120	8.3333	66.667	1	0.200 µs
121	8.2645	64.516	2	
122	8.1967	65.574	4	
123	8.1301	65.041	8	
124	8.0645	64.516	2	
125	8	64	8	
126	7.9365	63.492	4	
127	7.874	62.992	8	
128	7.8125	62.5	1	0.250 µs, 0.500 µs
129	7.7519	62.016	8	
130	7.6923	61.538	4	
131	7.6336	61.069	8	
132	7.5758	60.606	2	
133	7.5188	60.15	8	
134	7.4627	59.701	4	
135	7.4074	59.259	8	
136	7.3529	58.824	1	
137	7.2993	58.394	8	
138	7.2464	57.971	4	
139	7.1942	57.554	8	
140	7.1429	57.143	2	
141	7.0922	56.738	8	
142	7.0423	56.338	4	
143	6.993	55.944	8	
144	6.9444	55.556	1	0.500 µs
145	6.8966	55.172	8	
146	6.8493	54.795	4	
147	6.8027	54.422	8	
148	6.7568	54.054	2	
149	6.7114	53.691	8	
150	6.6667	53.333	4	

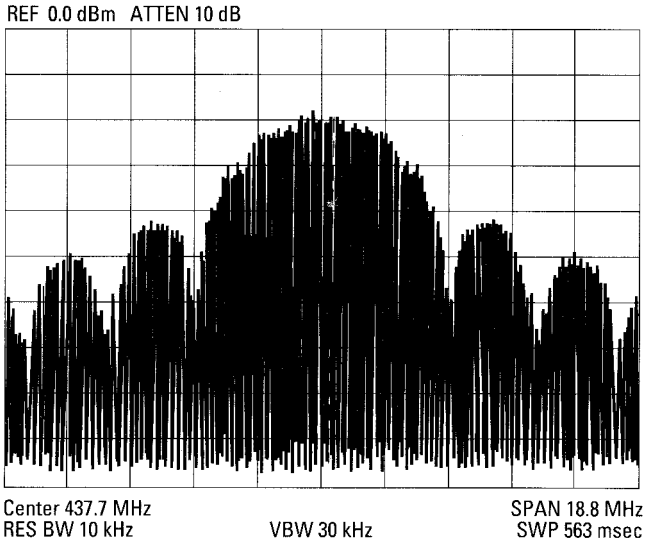

Figure 7. PLRS (Position Location Reporting System) test signal

This small frequency offset can be observed with the test setup of Figure 8. Here an external RF source (the Agilent 8780A Vector Signal Generator) provides a 120 MHz clock to FASS. The 10 MHz timebase output of the external clock is also used to phase lock the agile upconverter to minimize additional phase drift between the two sources. The agile upconverter can also accept a 5 MHz phase lock signal if a 10 MHz signal is not available. In many applications where a few Hertz residual frequency error is unimportant, then no phase locking is required. The coherent reference output of the 8780A provides the COHO reference for the Agilent 8981A Vector Modulation Analyzer, which is basically a two-channel digital scope with an integral I/Q demodulator (synchronous detector). The RF output of FASS is programmed for 120 MHz, or as close to 120 MHz as is possible given that an external clock is employed. Running the BASIC program of Figure 5 (with the appropriate inputs) predicts the exact frequency error. The FASS RF output is then fed into the RF input of the 8981A demodulator. With the modulation analyzer in DEMOD mode and the display in VECTOR mode (Q vs. I), any residual Doppler shift relative to the coherent external clock will show up as a rotating vector on the display. The period of rotation is exactly the reciprocal of the frequency error resulting from external clock operation. Without this test setup, it would be difficult to observe frequency errors so small.

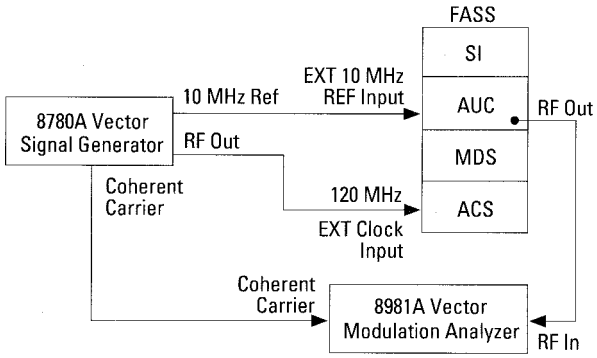

Figure 8. Test setup to observe effect of frequency offset

Radar Target Simulation

Let's examine a slightly more complex example. Suppose we wish to simulate a coherent target return to a radar under test. The simplified radar block diagram in Figure 9 is a UHF radar with a 450 MHz center frequency. It is desired to inject the target return at RF (450 MHz) or IF (75 MHz). This radar also provides a PRF trigger which is synchronized to an internal 5 MHz clock. The PRF trigger intentionally varies between 10 and 15 µs, with a 200 ns jitter resolution. Both a 5 MHz timebase and a 75 MHz coherent reference are available from the radar.

At first glance, one solution might be to double and condition the radar COHO to provide a 150 MHz clock to FASS. From Table 2, the 150 MHz clock rate gives a 6.66 ns period. But to guarantee no time slipping, FASS also requires that an external trigger be synchronized to CLK/8. This would give a 53.3 ns trigger period which, unfortunately, is not an integral submultiple of the required 200 ns jitter resolution.

Rather than quitting here, a more general solution to this and similar problems is to phase lock an external COHO to the radar. This way we have complete flexibility in choosing an appropriate clock to drive FASS. One solution uses the 5 MHz radar timebase to lock up an 8662 RF signal generator. The 8662 can accept a 5 or 10 MHz external timebase. (If an alternative source were available that could only accept a 10 MHz external timebase, then the 5 MHz signal could be doubled and conditioned).

Because of the 200 ns timing resolution imposed by the radar, a 120 MHz clock makes a good choice for both triggering and synchronization.

Choosing the 120 MHz clock means that FASS will have a residual frequency error of roughly –0.047 Hz for a 450 MHz nominal center frequency and +0.0059 Hz for a 75 MHz center IF. Such a slow Doppler offset is negligible for most systems.

Furthermore, because the error is precisely predictable, its effect can often be subtracted during signal processing. For a moving target simulation, this type of frequency error is much less than the Doppler bin resolution of the DSP. As such, any slight Doppler offset will be undetectable. Despite this offset, the target return will still be coherent with respect to the radar, such that coherent processing gain will be preserved. Even for MTI canceller systems, Doppler errors of this order are typically well below the high-pass filter threshold that separates moving targets from stationary targets.

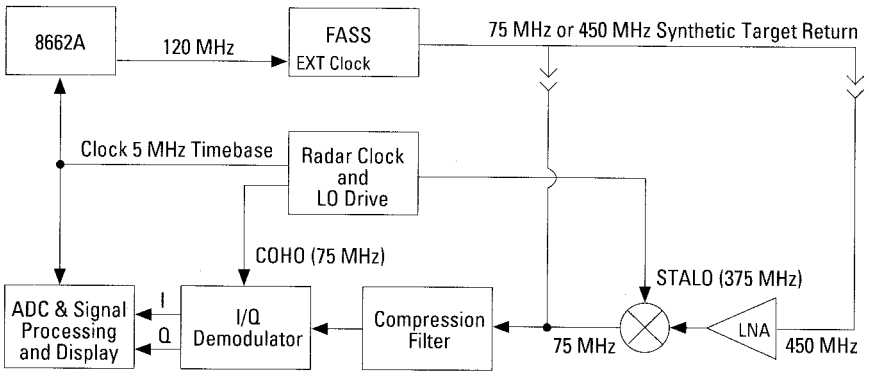

Figure 9. Simplified block diagram of a radar under test

Use of Agilent FASS in external clock mode is relatively straightforward. But because every situation is different, it is impossible to anticipate all potential problems when trying to synchronize a simulator to a device under test. However, if you run into unusual circumstances that are not readily addressed by this product note, please contact your Agilent representative for assistance. In some situations, we may be able to supply special clocks, calibration methods, or other hardware to solve your particular challenge.

External Clock Operation Specifications

The main clock reference signal enters the ACS from an external source. The signal should have the following characteristics:

- Frequency: 120 to 140 MHz
- Amplitude: 0 to +10 dBm into 50 ohms

Waveshape

Square wave to sinewave (approximately 50% duty cycle).

Summary of Clock Signals

		Input/Output	Power	Effect of External Clock (EXTCLOCK)
AUC	Frequency standard			
	Input 5 or 10 MHz	Input	+10 to 13 dBm for 5 MHz; 0 to 13 dBm for 10 MHz	5 or 10 MHz
	Output 10 MHz	Output	7 to 10 dBm	10 MHz
	CLK Out 134 MHz	Output	2.5 dBm	134 MHz (2^{27} Hz)
	TTL CLK In 16.8 MHz (CLK/8)	Input	TTL	EXTCLOCK/8
	38 MHz Output*	Output	–9 dBm	37.748736 MHz
	REF Out 537 MHz**	Output	10 dBm (typical)	537 MHz (2^{29} Hz)
	TTL CLK Out 16.8 MHz (CLK/8)	Output	TTL	EXTCLOCK/8
MDS	TTL Output			
	CLK/4	Output	TTL	EXTCLOCK/4
	CLK/8	Output	TTL	EXTCLOCK/8
ACS	TTL Output CLK/8	Output	TTL	EXTCLOCK/8
	10 MHz Reference			
	Output 1			(not used)
	Output 2			(not used)
	Input			(not used)
	System Sync			
	Sync Input	Input	ECL	EXTCLOCK
	Sync Output	Output	ECL or –2 V	EXTCLOCK
	Sync Output for Slave	Output	ECL or –2 V	EXTCLOCK
	EXT CLOCK Input	Input	ECL	EXTCLOCK

* Used for performance tests
** Used to drive AMUC

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