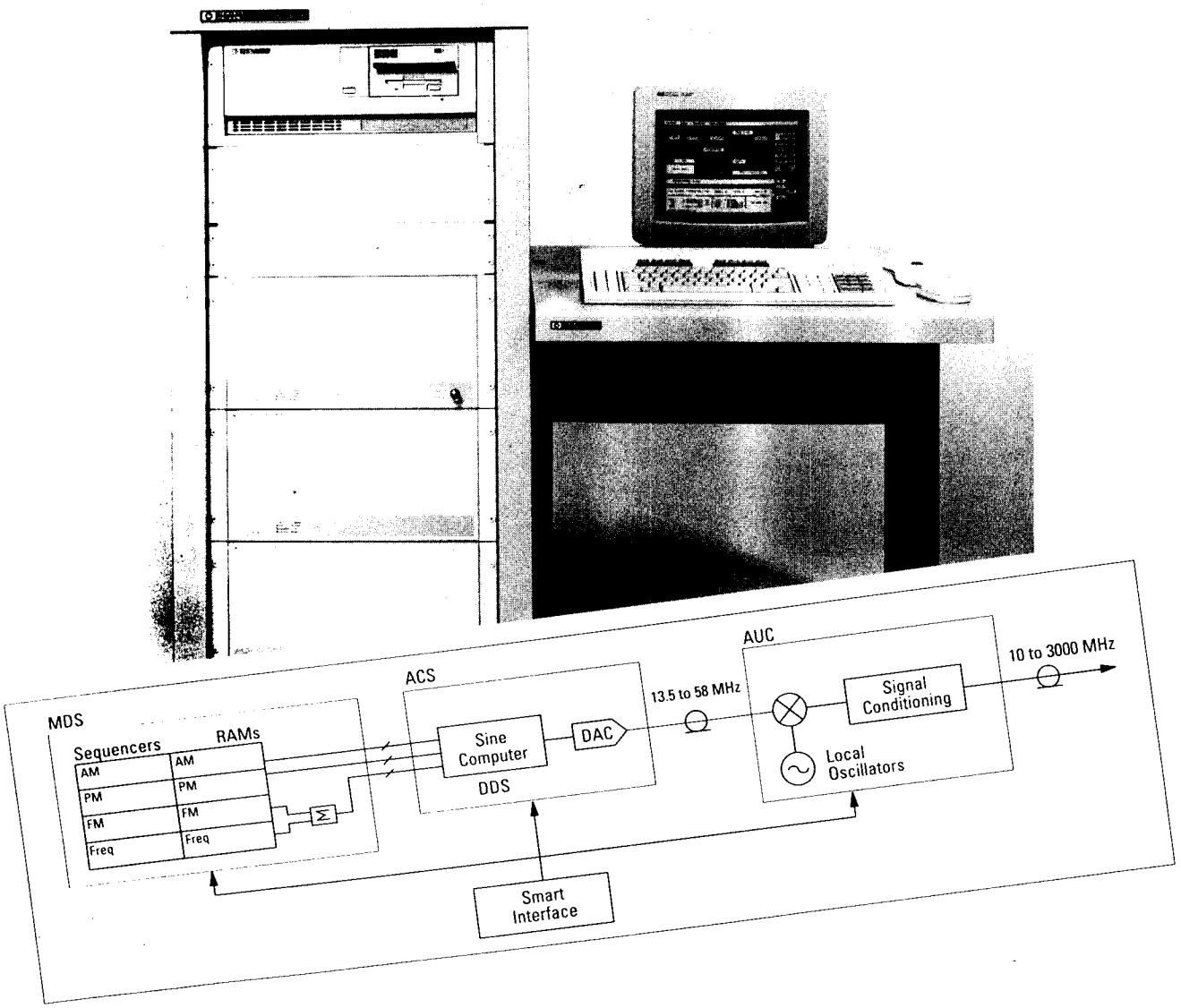
HEWLETT PACKARD

Product Note 8791-3

Theory of Operation for the HP 8791 Models 7/10/11/21 Frequency Agile Signal Simulator



Abstract:

Based on digital-synthesis technology, the HP 8791 Frequency Agile Signal Simulator (HP FASS) family meets the need for exotic, agile test signals for modern communication, radar, and EW systems. By combining a powerful data source, direct digital synthesizer, frequency-agile upconverters, and an easy-to-use software-reconfigurable user interface, HP FASS allows easy simulation of modulated signals ranging from simple amplitude-modulated sine waves to advanced waveforms such as nonlinear FM chirped signals with antenna scan modulation. This comprehensive product note details the operational theory and hardware architecture of this advanced simulator.

ACS	Agile Carrier Synthesizer
AM	Amplitude Modulation mode of AM/PM RAM or Amplitude Modulation
AM/PM	One of four HP FASS RAM memories
AMUC	Agile Microwave Upconverter
AUC	Agile Upconverter
CLK	System Clock (typically 134.217728 MHz)
CLK/4	System Clock/4 (typically 33.554432 MHz)
CLK/8	System Clock/8 (typically 16.777216 MHz)
DAC	Digital-to-Analog Converter
DAV	Data Valid
DRAM	Dynamic Random Access Memory
ECM	Electronic Countermeasures
EW	Electronic Warfare
EXTCLK	External Clock
FASS	Frequency Agile Signal Simulator
FLC	AUC Fast Level Control
FM	One of four HP FASS RAM memories or Frequency Modulation
FREQ	One of four HP FASS RAM memories
GPIO	General Purpose Input/Output
HP-IB	Hewlett-Packard Interface Bus
ID	Instrument-on-a-Disk
LO	Local Oscillator
MDS	Modulation Data Source
PM	One of four HP FASS RAM memories or Phase Modulation
PRF	Pulse Repetition Frequency (1/PRI)
PRI	Pulse Repetition Interval (1/PRF)
PSID	Precision Signal Generator ID
PULSE	Pulse Modulation
PW	Pulse Width
RAM	Random Access Memory
RSID	Radar Simulator ID
SAW	Surface Acoustic Wave
SI	Smart Interface
SID	System ID
WGL	Waveform Generation Language (Software)

This product note provides complete HP FASS hardware and operational theory information. It is intended for readers with some familiarity with HP FASS who need to understand the operational theory in order to use or troubleshoot the instrument effectively.

This document is divided into nine sections. Sections 1 and 2 present an overview of the entire system. Sections 3, 4, and 5 detail the architecture and discuss data/signal flow through each of the three sub-instruments which are common to all models of the HP FASS. The Agile Upconverter of Models 10/11/21 is discussed in Section 6, while Section 7 presents the architecture of the Agile Microwave Upconverter, which is present in the Model 21 system. Section 8 discusses system-level issues, while section 9 covers triggering and synchronization.

The following references are also available:

- Product Note 8791-1, *Real-time Control of HP FASS*
- Product Note 8791-2, *Programming HP FASS with WGL*
- Product Note 8791-4, *Secure Communications Testing with the HP FASS*
- Product Note 8791-5, *Tips on External Clock Operation with HP FASS*
- Product Note 8791-6, *Jamming Signal Capability of the HP FASS*
- Product Note 8791-7, *Spectral Purity of the HP FASS*
- Product Note 8791-8, *A Survey of Radar Test Applications Using HP FASS*
- Product Note 8791-9, *Effective Application of User Patterns for HP FASS*
- Application Note 314-5, *A Guide to Microwave Upconversion*

Consult the HP 8791 Family Ordering Guide or your HP representative for information regarding Instrument Service, Instrument-on-a-Disk, and other HP FASS manuals.

What is HP FASS?

Based on state-of-the-art technology, the HP FASS system combines high-speed direct-digital synthesis with extremely agile direct analog upconversion to generate advanced signals for testing modern systems. The Model 10 and Model 11 systems provide carrier frequencies anywhere within the 10-to-3000 MHz range, while the Model 21 system has an extended frequency range of 18 GHz. The frequency coverage of the Model 7 baseband system is restricted to a DC to 50 MHz range. While the Model 10/11/21 systems are fully agile over their respective frequency ranges with better than 100-ns typical frequency switching speed, the Model 7 system can switch frequencies in 30 ns.

Additionally, signals may have arbitrary AM, PM, FM, and pulse modulation with up to 40 MHz (Models 10/11/21) or 50 MHz (Model 7) instantaneous modulation bandwidth. The digitally-synthesized carrier and modulation provide an overall signal complexity, flexibility, and repeatability unachievable with traditional signal sources or custom simulators.

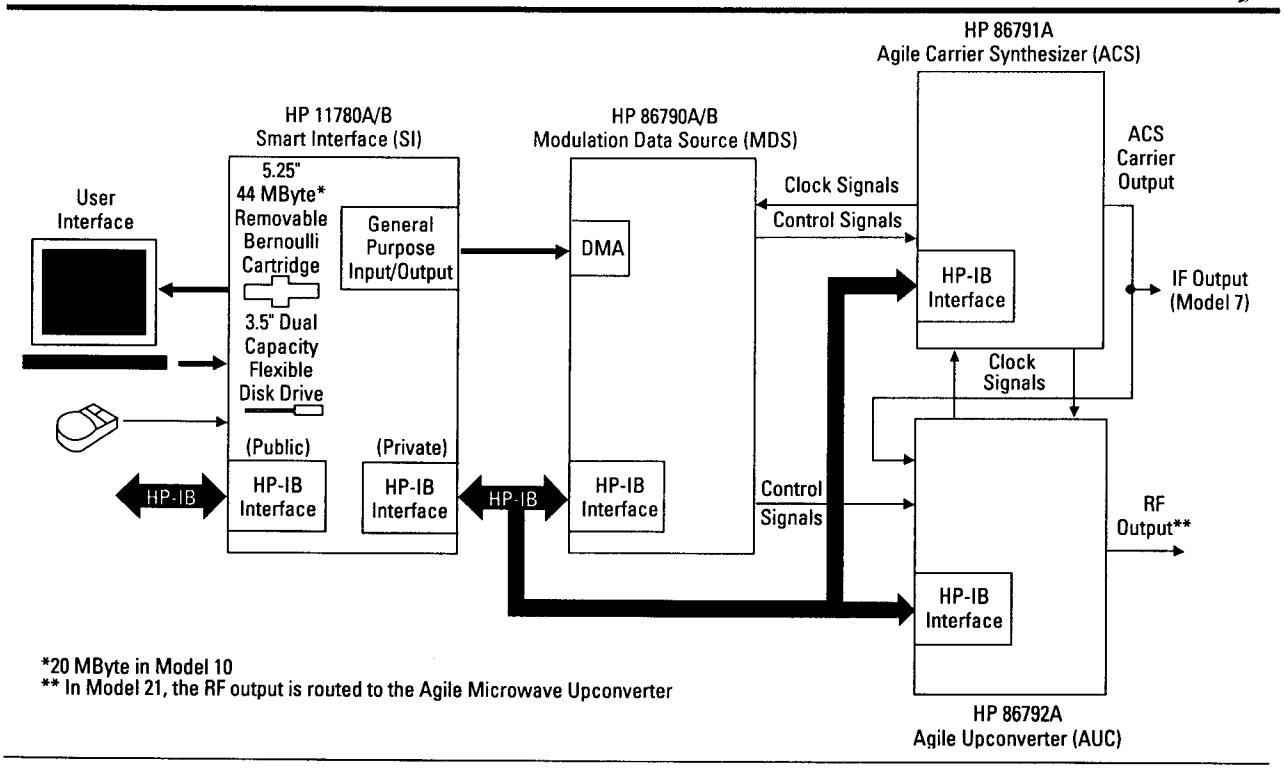
As shown in figure 2-1, the HP FASS system is actually composed of four separate instruments:

- HP 11780A/B Smart Interface (SI). Controls entire system and provides interface to user.
- HP 86790A/B Modulation Data Source (MDS). Stores digital modulation data.
- HP 86791A Agile Carrier Synthesizer (ACS). Digitally generates IF carrier, adds modulation, and converts digital into analog.
- HP 86792A Agile Upconverter (AUC). Upconverts IF signal with fast switching capability. (Models 10, 11, and 21 only.)

The Model 21 adds a fifth instrument to the system:

- HP 86793A Agile Microwave Upconverter (AMUC). Upconverts RF signal with fast switching capability.

Detailed operation of these five instruments, both at an individual level and at a system level, will be discussed in later sections.



*20 MByte in Model 10
** In Model 21, the RF output is routed to the Agile Microwave Upconverter

Figure 2-1. Simplified block diagram of HP FASS.

Finally, the entire HP FASS system is reconfigurable via application-oriented Instrument-on-a-Disk (ID) software or through independent programming over HP-IB. This programming flexibility adapts the system for a variety of applications and allows for easy customization and integration.

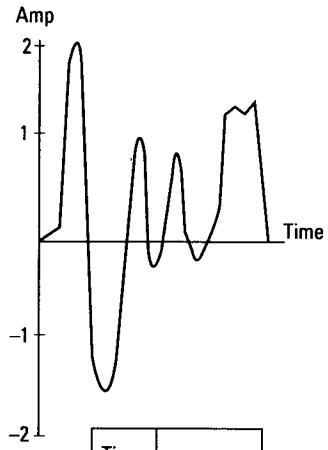
Conceptual Functionality

Digital synthesis of analog signals can be broken into two distinct approaches:

- Arbitrary Waveform Synthesis
- Direct Digital Synthesis

Arbitrary waveform synthesis is conceptually the simplest signal generation method whereby time-domain digital data samples uniquely describe a waveform profile (figure 2-2). Each data point can assume one of 2^n amplitude values into an n-bit digital-to-analog converter. Much like a compact disc player, the waveform data is read from mass storage (either ROM or RAM). Sometimes a memory sequencer is used to efficiently handle certain classes of waveforms that have repeating segments. Arbitrary waveform synthesizers such as the HP 8770A are excellent sources of complex baseband or I/Q signals useful for testing the video and IF portions of radar, EW, and communications receivers. Through suitable upconversion techniques, sophisticated deterministic signals can be simulated for testing a wide variety of RF and microwave systems.

Alternatively, direct digital synthesis allows independent control of the carrier and its modulation, including amplitude, phase, frequency, and pulse (figure 2-3). Common applications that call for this independent control of carrier and modulation include advanced threat simulation, dynamic radar target simulation, and secure communications signal simulation. Using direct digital synthesis, you can define a signal by its carrier frequency and by its modulation content — instant by instant.



Time	Amplitude
1	0.00
2	0.05
3	0.10
4	1.50
5	1.95
6	0.00
Etc.	Etc.

Figure 2-2. Point-by-point simulation using an Arbitrary Waveform Synthesizer.

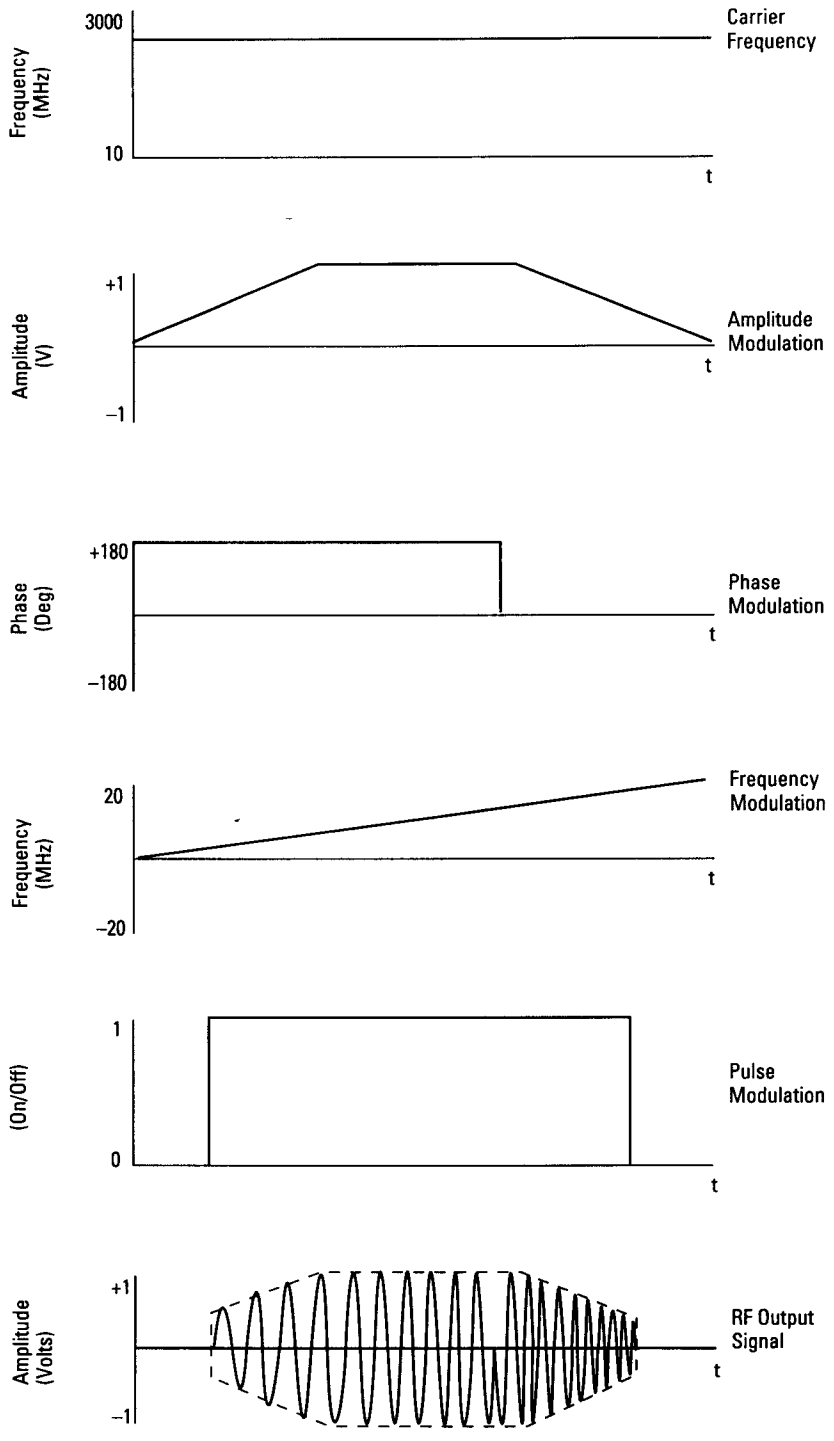
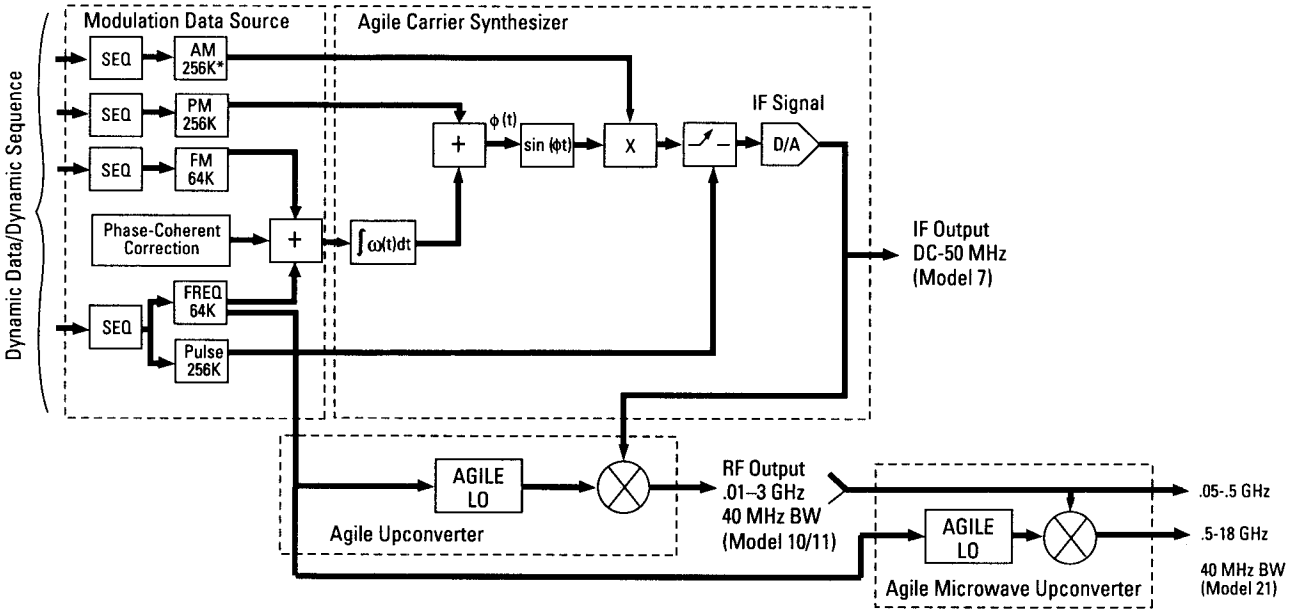


Figure 2-3. Signal simulation by direct digital synthesis.



*For Model 10, all modulation memories are 1/4 the size indicated.

Figure 2-4. Conceptual block diagram of HP FASS. Phase-coherent correction and dynamic sequence not available in Model 10.

Figure 2-4 shows the conceptual block diagram of HP FASS, a direct digital synthesizer. The ACS generates a carrier signal on-the-fly by integrating a frequency input word from the MDS into phase samples vs. time. This is the function of the phase accumulator — a first-order digital integrator. These phase samples are then fed to a sine look-up table whose output amplitude is proportional to the input phase word. By carefully including simple adders and multipliers, it is possible to add AM, PM, FM, and pulse modulation to the basic carrier data. A digital-to-analog converter is used to generate an IF analog signal, which is then upconverted using the AUC. In Model 21, the signal is further upconverted to microwave range using the AMUC.

A mathematical description of HP FASS is presented in figure 2-5.

$$S_o(t) = FLC(t) \bullet P(t) \bullet A(t) \bullet \sin[2\pi \int f_c(t) + 2\pi \int f_m(t) + \Phi(t)]$$

where:

$S_o(t)$ = System RF output signal.

FLC (t) = Fast Level Control Setting for changing AUC attenuation (0 dB to 90 dB).

P (t) = Pulse Modulation (0 or 1).

A (t) = Amplitude Modulation (–1 to +1).

$f_c(t)$ = Carrier frequency. Comprised of ACS frequency ($f_{ACS}(t)$), AUC upconversion frequency ($f_{AUC}(t)$), and AMUC upconversion frequency ($f_{AMUC}(t)$)

$f_m(t)$ = Frequency Modulation (–20 MHz to +20 MHz typical)

$\Phi(t)$ = Phase Modulation (–180° to +180°).

Figure 2-5. Mathematical description of HP FASS.

Hardware Overview

While signal generation with HP FASS is conceptually straightforward, intimate knowledge of each of the instruments in the system is generally recommended for a user to fully appreciate and utilize its capabilities. Therefore, a brief overview of the hardware is presented here, with more complete details being given in sections 3 through 7.

The Smart Interface (SI) acts as an internal controller which unifies the other instruments into a single system. In addition, it handles all system data I/O, runs Instrument-on-a-Disk software, accelerates waveform data calculations, and manages data files on a 44 MB removable Bernoulli Technology*(TM) cartridge. Operation of HP FASS is done through the keyboard, mouse, and interactive soft front-panel display of the SI or via remote programming through the SI's public HP-IB port.

The MDS holds digital modulation and carrier data downloaded from the SI. The data is held in four independent RAM banks, one each for AM, PM, FM, and carrier frequency (FREQ). The frequency RAM further subdivides into four fields. These subfields store pulse modulation and attenuation data in addition to the carrier frequency information. Each RAM has its own memory sequencer which stores addressing information for strobing the RAM data into the ACS and the AUC. Alternatively, external data ports accept dynamic addressing for real-time signal control.

The ACS, a high-speed direct digital synthesizer, has two main sections — a modulation-controlled sine computer and a precise digital-to-analog converter (DAC). Modulation and carrier data from the MDS is fed to the sine computer, which combines digital phase accumulators, adders, and other logic to form 12-bit words that define the instantaneous amplitude values of the signal. With the internal clock of 134 MHz (2^{27} Hz), a spectrally-pure DAC faithfully converts the digital data to an analog level every 7.45 ns. The combination of fast sampling, 12 bits, and specially-designed smoothing circuits provide the necessary fidelity and modulation bandwidth required for today's exotic signals.

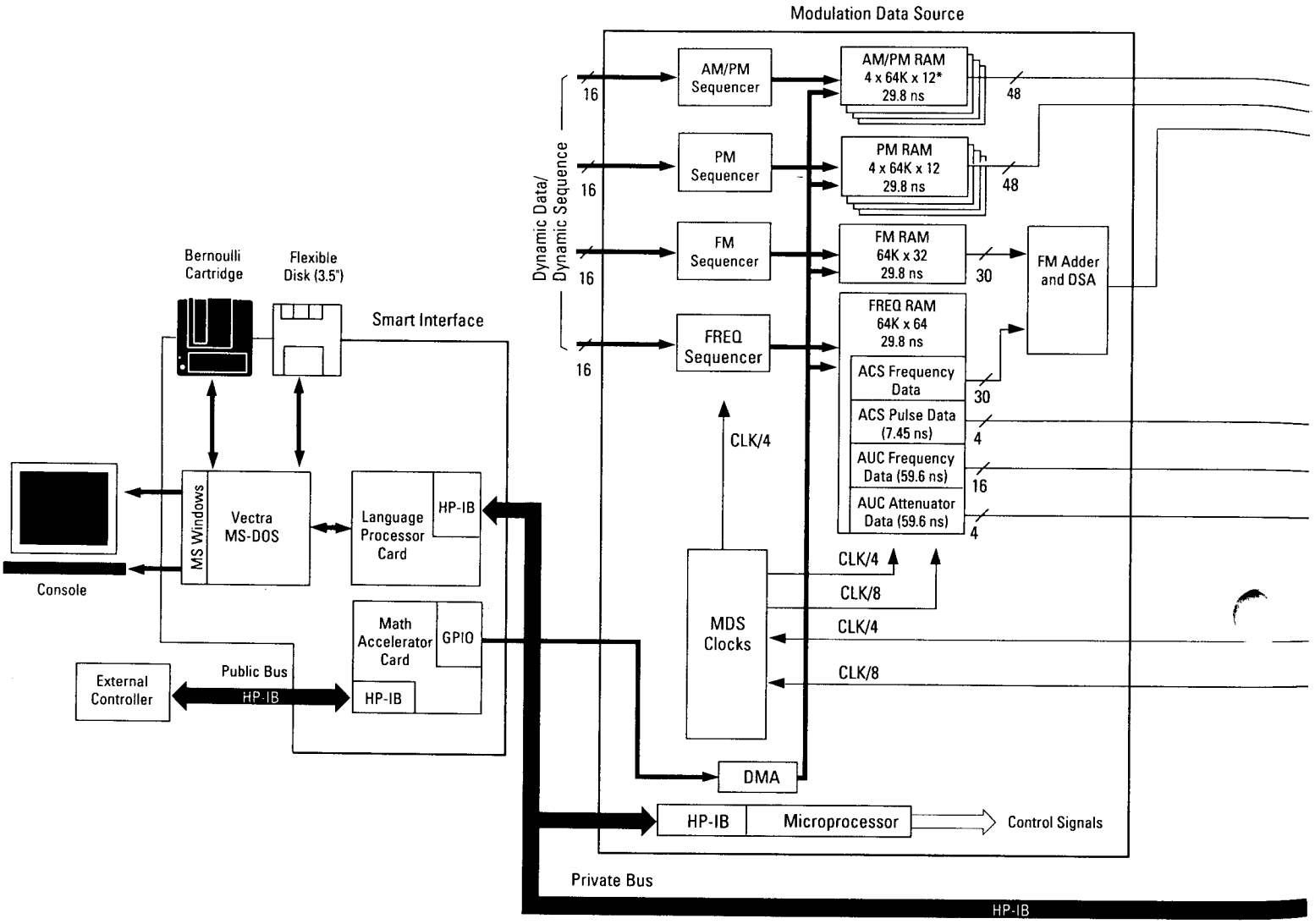
In Models 10/11/21, the AUC filters a 13.5-to-58 MHz modulated output from the ACS and upconverts the signal to the 10-to-3000 MHz range with an overall frequency resolution of 0.125 Hz. A specially-designed four-stage mixing chain combined with a SAW bandpass filter minimizes spurious signals. Direct analog synthesis ensures excellent phase noise coupled with rapid frequency switching over the full 3 GHz range. The AUC also contains attenuators and amplifiers for setting signal levels. These features provide precise signal conditioning for advanced signal simulation.

In Model 21, the output signal from the AUC is then routed to the AMUC, where it is split into two paths. The first path is simply filtered to provide an output in the 0.05-to-0.5 GHz range. The signal in the second path is further upconverted to provide an output in the 0.5-to-18 GHz range. Again, direct analog synthesis techniques are used to ensure fast frequency switching and excellent spectral purity over the full 18 GHz frequency range of Model 21.

Figure 2-6 shows a detailed block diagram of HP FASS. Also shown are the interconnections between the instruments, including clock signals and data lines. The AMUC of Model 21 is not shown in this particular diagram.

NOTE: The block diagram of figure 2-6 is modified slightly for Model 7. See Appendix A for a complete description of the Model 7 configuration.

* Bernoulli Technology is a registered trademark of IOMEGA.


Modulation Data Source
Dynamic Data/
Dynamic Sequence
16
16
16
16
AM/PM Sequencer
PM Sequencer
FM Sequencer
FREQ Sequencer
AM/PM RAM
4 x 64K x 12*
29.8 ns
PM RAM
4 x 64K x 12
29.8 ns
FM RAM
64K x 32
29.8 ns
FREQ RAM
64K x 64
29.8 ns
48
48
30
FM Adder
and DSA
ACS Frequency
Data
ACS Pulse Data
(7.45 ns)
AUC Frequency
Data (59.6 ns)
AUC Attenuator
Data (59.6 ns)
30
4
16
4
CLK/4
CLK/4
CLK/8
CLK/4
CLK/8
MDS
Clocks
DMA
HP-IB
Microprocessor
Control Signals
Private Bus
HP-IB
Bernoulli
Cartridge
Flexible
Disk (3.5")
Smart Interface
Console
MS Windows
Vectra
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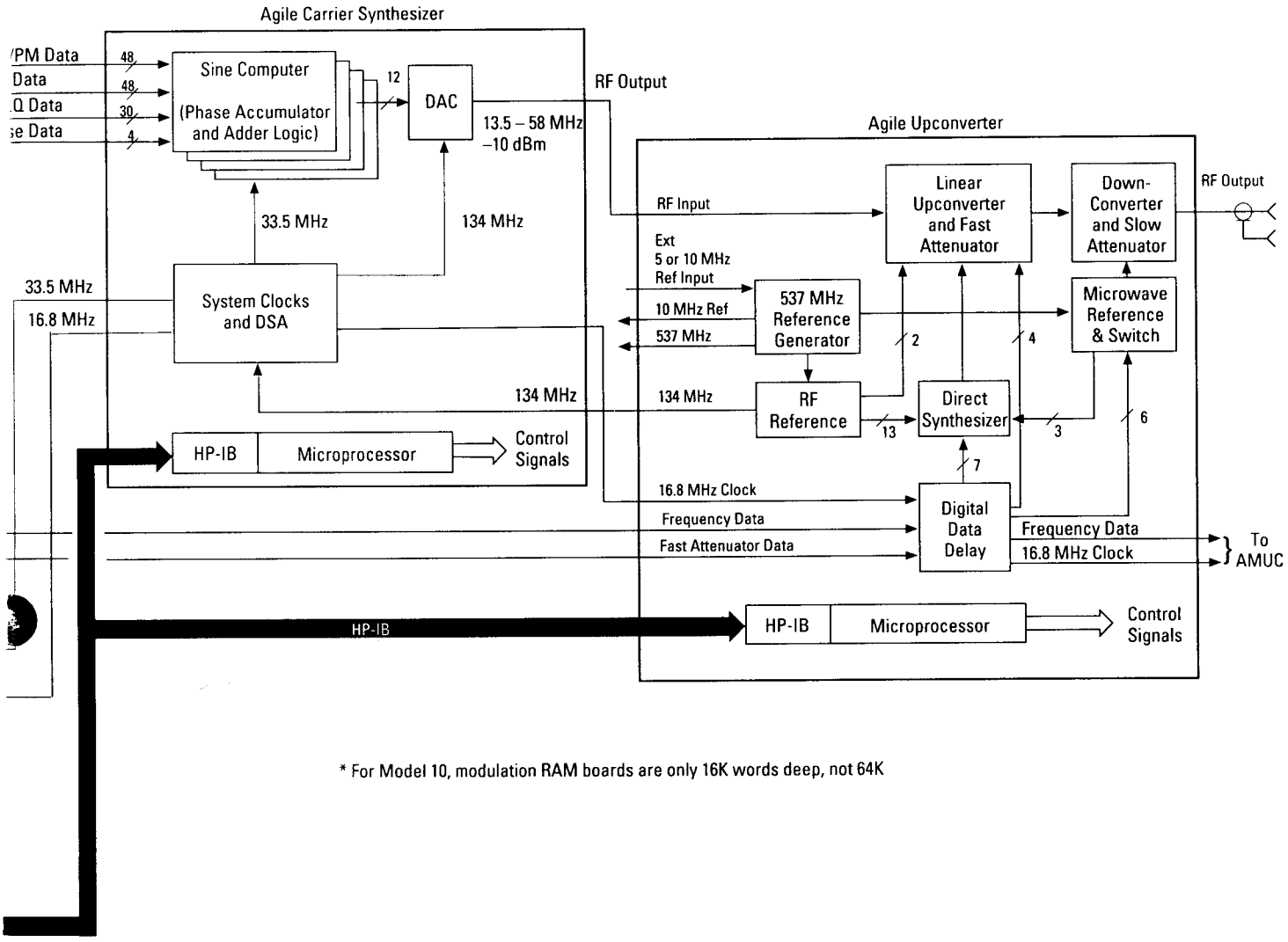
GPIO
External
Controller
Public Bus
HP-IB
HP-IB



* For Model 10, modulation RAM boards are only 16K words deep, not 64K

Figure 2-6. Block diagram of HP FASS instruments.

Ways to Control HP FASS

HP FASS can be controlled using any of the following:

1. Instrument-on-a-Disk (ID) Software
2. Dynamic Data/Dynamic Sequence
3. Waveform Generation Language (WGL) Software
4. HP-IB

A common method of controlling the HP FASS system is by using an ID in either local (front panel) or remote (HP-IB) mode. The ID software provides easy-to-use graphic and HP-IB interfaces for the HP FASS system. At the time of this publication, available IDs include:

- HP 8791 Model 100 Precision Signal Generator ID (PSID)
- HP 8791 Model 200 Radar Simulator ID (RSID).
- System ID (SID)

Model 100 Precision Signal Generator ID software (PSID) configures the HP FASS hardware to mimic a system of four advanced function generators and a high-performance, synthesized agile source. Amplitude modulation, phase modulation, frequency modulation, and carrier frequency are independently controllable and can be driven with sinusoidal, rectangular, and user-defined modulation waveforms.

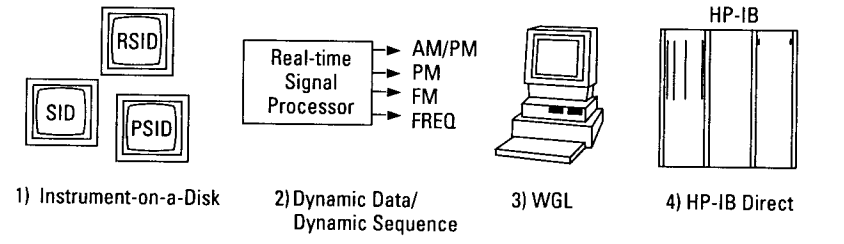


Figure 2-7. Ways to control HP FASS.

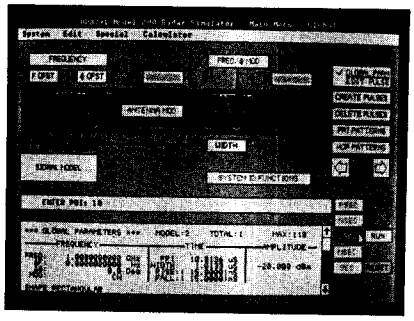


Figure 2-8. The Model 200 Radar Simulator ID provides easy simulation for testing EW receivers.

Model 200 Radar Simulator ID software (RSID) provides advanced single-emitter simulation for testing EW receivers with sophisticated, precision threat signals (figure 2-8). Its flexibility makes it useful for most applications requiring complex pulsed signals. Frequency hopping, intrapulse modulation such as chirps and Barker codes, PRI modulation, pulse shaping and a variety of antenna scan modulations are just a few of the functions provided by RSID.

The System ID (SID) software is resident on the standard Bernoulli Technology 44 MB cartridge and on all application ID cartridges. SID allows easy access to system functions such as running diagnostics, configuring system triggering, setting attenuation levels, and managing ID or user-defined waveforms. SID also allows external control of the system via HP-IB, simplifying integration into turnkey simulators and ATE systems.

Dynamic data refers to the real-time modulation of frequency, phase, amplitude, or pulse characteristics of a signal using an external data source or signal processor. In this mode, the addressing information for the individual modulation RAMs is provided by the external source instead of by the internal sequencers of the HP FASS. Refer to Product Note 8791-1 *Real-time Control of HP FASS* for complete information.

An additional real-time capability known as "dynamic sequencing" is available in the Model 7, Model 11 and Model 21 systems. This mode allows a user to randomly select a signal on-the-fly based on some external event. This feature is extremely useful in applications where the required signals are known ahead of time, but their exact timing is not. Simulation of multi-mode radars is one such application.

For ultimate flexibility and control, the Waveform Generation Language (WGL) Software lets you custom-design signals in both the frequency and time domains. In particular, WGL allows you to:

- Create user-defined modulation patterns for application IDs
- Create dynamic data maps
- Bypass application IDs for direct HP FASS programming.

Refer to Product Note 8791-2 *Programming HP FASS With WGL* for complete information.

Finally, HP FASS can always be controlled over HP-IB using any computer with an IEEE-488 port.

As shown in figure 3-1, the Smart Interface (SI) consists of the following components:

- A modified HP Vectra computer
- An internal 44* MByte Bernoulli Cartridge Drive Subsystem with a removable cartridge
- A 3.5-inch dual-capacity (710/720 KByte or 1.44 MByte) Flexible Disk Drive
- An HP 82310A Pascal Language Processor board with 4 MBytes of internal memory
- A Math Accelerator board with two I/O ports.

The Smart Interface (SI) controls the console (display, keyboard, and mouse), the Bernoulli cartridge and flexible disk drives, and the other HP FASS system instruments. During signal-generation mode, the SI calculates all signal and control data required by the system and programs the individual instruments accordingly. In system-management mode, the SI performs a variety of system functions, including signal-data management and hardware configuration setup.

When an external controller is used with the system, HP-IB commands are sent to the SI over the public HP-IB bus. The SI then interprets the commands and sends appropriate commands and/or data to each of the other system instruments over the private HP-IB bus.

* 20 MByte in Model 10

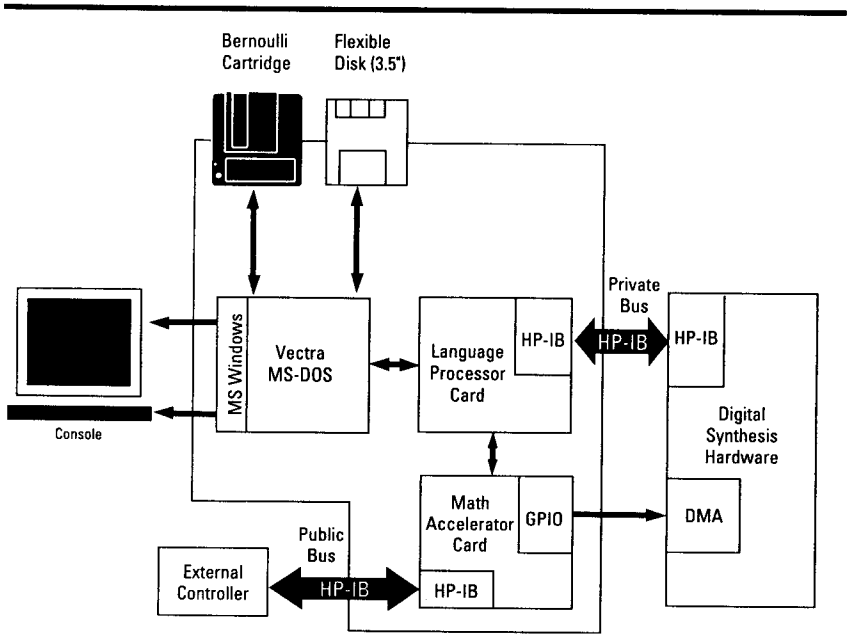


Figure 3-1. HP 11780A/B Smart Interface block diagram.

Vectra

As shown, the Vectra computer portion of the SI provides a platform for the MS-DOS and MS Windows software environments. This software is used in conjunction with Instrument-on-a-Disk software to control the console, thereby providing a "front panel" user interface. The Vectra also provides housing and power for the Bernoulli cartridge drive, flexible disk drive, Language Processor Board, and Math Accelerator Board.

Note: The Vectra computer serves as the "microprocessor" for HP FASS. It has been enhanced with custom hardware and cannot be substituted with another personal computer or used for other personal computer applications.

Bernoulli Cartridge Drive

The Bernoulli cartridge drive is a high-capacity, high-performance, direct-access storage device using Bernoulli media with 44*-MByte data storage capacity. It contains the system operating software, the System ID software, and an optional application ID software package. This software is installed on the removable Bernoulli cartridge before the disk is shipped. The Bernoulli cartridge is also used for non-volatile storage of signal data and ID settings.

If for any reason the contents of the Bernoulli cartridge are compromised, the cartridge can be removed and a back-up cartridge inserted into the cartridge drive. It is the user's responsibility to maintain back-up copies of any signal data that is generated.

Flexible Disk Drive

3.5-inch flexible dual-capacity (1.44 MByte) disks are primarily used to store user patterns, ID settings, and hardware images*. In addition to providing software backup, this capability allows movement of signal data from one HP FASS system to another.

*User Pattern: A user-defined modulation pattern which is stored in a file and accessed from an application ID, thereby extending the ID's modulation capabilities.

ID Setting: The "front panel" button settings of an application ID. An ID setting contains all the information needed to calculate, download, and generate a signal when using an application ID with HP FASS.

Hardware Image: An exact copy of the HP FASS instrument state, including all hardware settings, modulation memory data, and sequencer information.

Language Processor Board

The Language Processor Board emulates the operation of an HP 9000 Series 300 controller using the Pascal Operating System. Extended memory provides a total of 4 MBytes of RAM for this application. The processor board controls the Math Accelerator Board and the other system instruments during signal generation mode. The system instruments interface to the HP-IB port on the Language Processor Board. This internal system is referred to as the private HP-IB bus.

Math Accelerator Board

A Math Accelerator Board interfaces directly to the Language Processor Board to provide improved mathematical calculation performance. In addition, it provides two additional I/O ports. The general purpose input/output (GPIO) port is used to download digital data to the MDS through its DMA interface. The HP-IB port is used to interface the HP FASS system to an external controller. This external HP-IB is referred to as the public bus.

The Modulation Data Source (MDS) receives signal information from the Smart Interface (SI) and stores it as binary data in one of four modulation memories: AM/PM, PM, FM, or FREQ. Each of these memories is controlled by a sequencer, which generates the addresses needed to access the modulation RAM. During signal generation, the data from the memories is clocked into the Agile Carrier Synthesizer (ACS) and the Agile Upconverter (AUC), where it is used to create the analog output signal.

As shown in figure 4-1, the MDS consists of the following:

- Modulation Memories
- Sequencer Memories
- FM Adder and Digital Signature Analysis (DSA)
- MDS Clocks
- Direct Memory Access (DMA)
- HP-IB and Microprocessor

Modulation Memories

The four modulation memories in the MDS are used to store AM, PM, FM, and carrier frequency profiles for the signal to be generated. The structure of each of these memories will now be examined, along with any limits the user must be aware of when programming the system.

Note: The following discussion assumes that the internal 134 MHz (2^{27} Hz) system clock is being used. Also, memory sizes are given for the Model 7/11/21 systems. In Model 10, all modulation memories are one-quarter the indicated size.

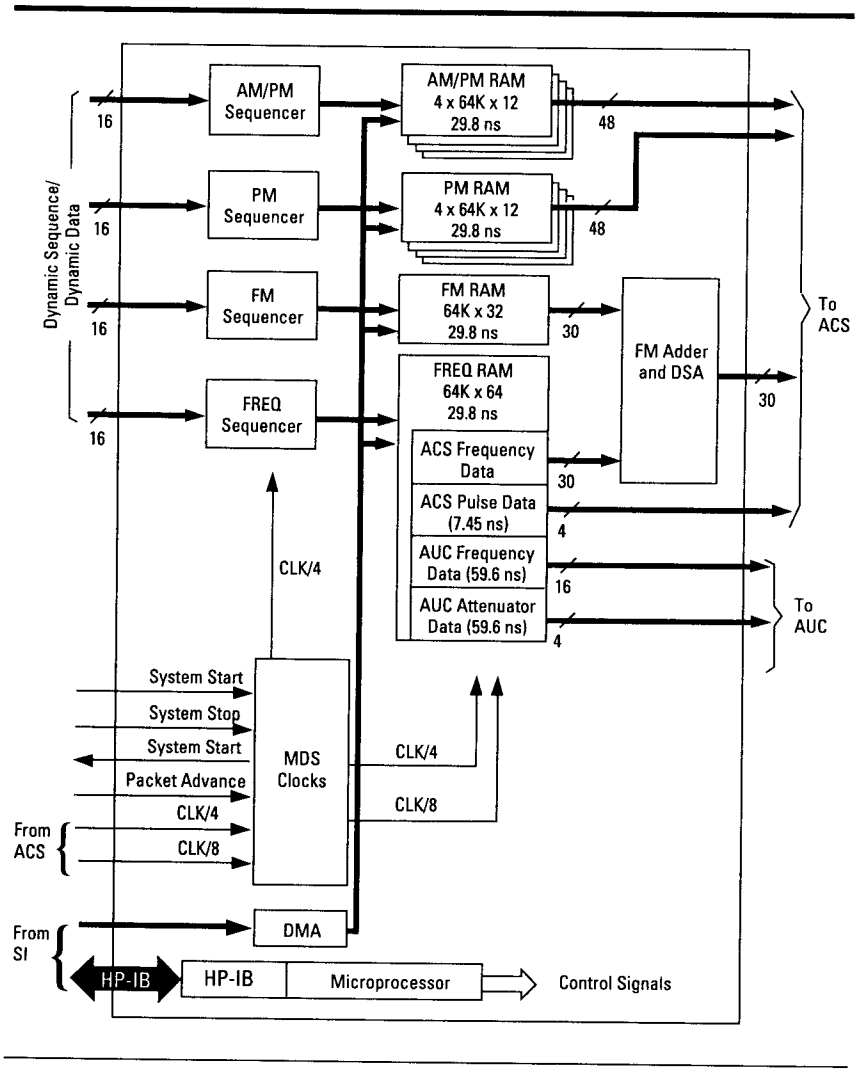


Figure 4-1. HP 86790B Modulation Data Source block diagram.

AM/PM Modulation RAM.

This memory consists of four 64K by 12-bit RAM boards which are accessed in parallel every 29.8 ns (CLK/4). The resulting 48-bit word is passed to the ACS, where data multiplexing gives four serial 12-bit data words, one every 7.45 ns. (See section 5 for complete details of this multiplexing scheme.)

* The HP 86790A is used in Model 10 and the HP 86790B is used in Models 7/11/21.

Figure 4-2 shows the structure of the 48-bit word from the AM/PM memory. The numbers in parenthesis are the effective access times after multiplexing in the ACS.

Note that the data in this memory can be either amplitude modulation data (AM mode) or phase modulation data (PM mode). In AM mode, the data stored can range anywhere from –1 to +1. (A value of +1 represents full amplitude, a value of 0 represents no amplitude, and a value of –1 represents full amplitude with inverted phase.) In PM mode, the AM/PM memory serves as a second phase modulator in the HP FASS system. The data range in PM mode is identical to the data range for the PM RAM. (See figure 4-3.)

PM Modulation RAM. This memory consists of four 64K by 12-bit RAM boards which are accessed in parallel every 29.8 ns (CLK/4). The resulting 48-bit word is passed to the ACS, where data multiplexing gives four serial 12-bit data words, one every 7.45 ns. (See section 5 for complete details of this multiplexing scheme.)

Figure 4-2 shows the structure of the 48-bit word from the PM memory. The numbers in parenthesis are the effective access times after multiplexing in the ACS.

Data stored in the PM memory can range anywhere from –180° to +180° in degrees mode, or from –PI to +PI in radians mode. (See figure 4-3.)

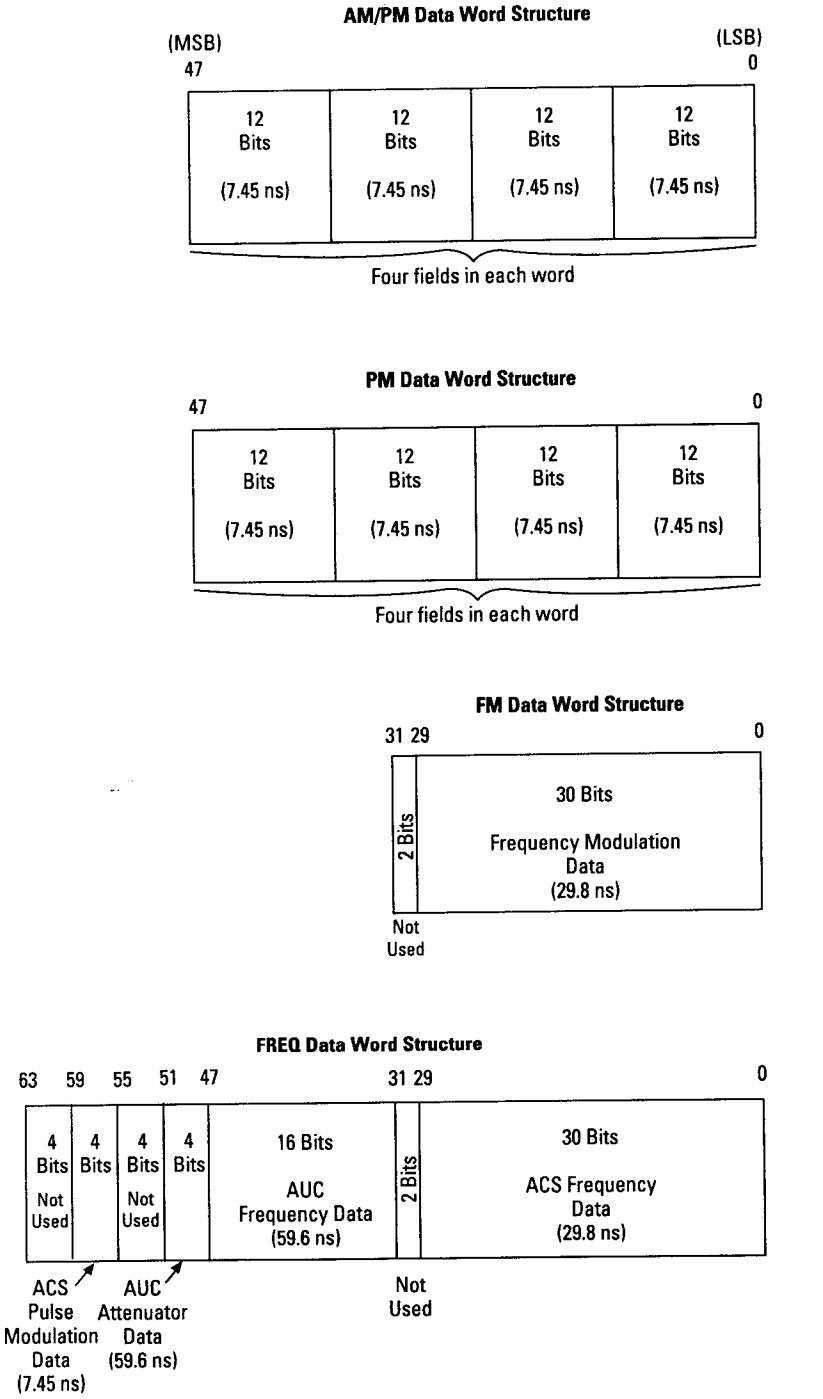


Figure 4-2. Data structure for each of the four modulation memories in the MDS. A data word is clocked from each memory every 29.8 ns.

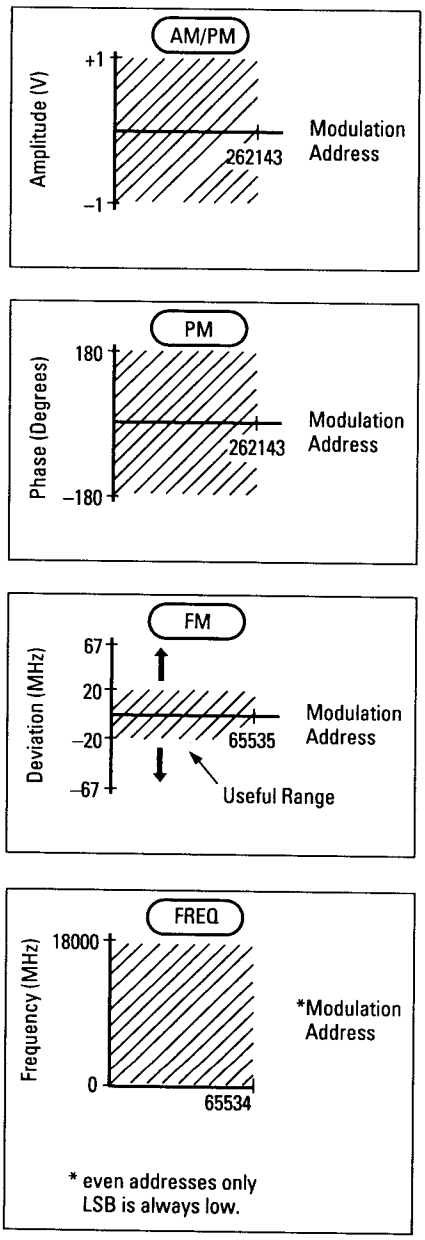


Figure 4-3. Modulation memory data ranges.

Note: Since frequency and phase are related by a derivative/integral operation, it is possible to use the PM memory to do frequency modulation. This feature is useful for applications requiring two FM memories. In radar target simulation, for instance, the PM memory can be programmed with a parabolic phase profile to give a linear chirp, while the FM memory can be programmed with a slowly-varying doppler profile.

FM Modulation RAM. This memory consists of one 64K by 32-bit RAM which is accessed every 29.8 ns (CLK/4). Two bits in each word are unused. The resulting 30-bit word is passed to the FM Adder circuitry in the MDS. Figure 4-2 shows the structure of this word.

Data stored in the FM memory can range anywhere from –67 MHz to +67 MHz. However, the Model 10/11/21 systems have an instantaneous modulation bandwidth of about 40 MHz due to filtering in the Agile Upconverter. For this reason, FM data is usually in the –20 MHz to +20 MHz range. (See figure 4-3.) The Model 7 system has an instantaneous modulation bandwidth of 50 MHz, thereby allowing slightly higher frequency deviations.

FREQ Modulation RAM. This memory consists of one 64K by 64-bit RAM which is accessed every 29.8 ns (CLK/4). Ten bits in each word are unused. The resulting 54-bit word is subdivided into the following memory fields:

- *ACS Frequency Field.* This 30-bit field contains the IF carrier frequency to be generated by the ACS. This data is passed to the FM Adder circuitry in the MDS every 29.8 ns. Data stored in this field can range anywhere from 0 to 67 MHz, however due to filtering in the Agile Upconverter it is best to keep the ACS frequency data around 36 MHz for Models 10, 11, and 21. (See discussion on System Bandwidth in section 8.)

- *ACS Pulse Field.* This 4-bit field contains four consecutive 1-bit ON/OFF states for the ACS. Data from this field is passed to the ACS every 29.8 ns. However, data multiplexing in the ACS ultimately gives four serial 1-bit data words, one every 7.45 ns. (See section 5 for complete details of this multiplexing scheme.) The value stored in each bit of this field is either a one (representing an ON condition for the output signal) or a zero (representing an OFF condition for the signal).

• *AUC Frequency Field.* This 16-bit field contains the upconversion band to be used by the Agile Upconverter of Models 10/11/21. This data is passed to the AUC every 29.8 ns. As we'll see later in section 6, data is only latched into the AUC every 59.6 ns (CLK/8). Therefore, data loaded into the AUC Frequency Field is automatically stretched in firmware so that two consecutive words (address locations) always contain the same AUC band value.

Note: In Model 21, upconversion is done with both the AUC and the Agile Microwave Upconverter. Although data loaded into the AUC Frequency Field is still sent to the AUC, only the lower-order bits are actually used by the AUC. The most significant bits are stripped off and passed on to the AMUC to set its upconversion band. This process is transparent to the user.

• *AUC Attenuator Field.* This 4-bit field contains the Fast Level Control (FLC) setting for the Agile Upconverter. (See section 6.) This data is passed to the AUC every 29.8 ns. As we'll see later in section 6, data is only latched into the AUC every 59.6 ns (CLK/8). Therefore, data loaded into the AUC Attenuator Field is automatically stretched in firmware so that two consecutive words (address locations) always contain the same FLC value. Data stored in this field can range anywhere from 0 to 90 dB in 6.02 dB steps and is automatically rounded to the nearest 6-dB multiple.

Figure 4-2 shows the structure of the 64-bit word from the FREQ memory. The numbers in parenthesis are the effective access times as a result of either multiplexing in the ACS (ACS Pulse Field) or data stretching in the MDS (AUC Frequency Field and AUC Attenuator Field).

Figure 4-3 shows that the overall frequency coverage of the HP FASS ranges from DC for the Model 7 to 18 GHz for the Model 21. However, in Models 10/11/21 the data that is actually stored in the MDS must be separated into two components, an ACS IF frequency and an AUC upconversion band. The relationship between these two values and the overall output frequency is given as follows:

$$Output\ Freq = [(AUC\ BAND - 8) * 2^{22}] + ACS\ FREQUENCY$$

The value 2^{22} Hz = 4.194304 MHz is the frequency step resolution of the Agile Upconverter.

Sequencer Memories (Model 10)

There are four sequencer memories in the MDS, one for each of the four modulation memories. These sequencers serve as address generators for accessing signal data from the RAMs. They provide efficient and flexible use of the modulation RAMs by allowing sections of memory to be repeatedly accessed. We'll use the example in figure 4-4 to illustrate how sequencing in the HP FASS system works.

In this example, one of the modulation memories is loaded with a series of waveforms, each given a unique name (AWAVE, BWAVE, CWAVE, DWAVE, EWAVE, or FWAVE). In practice, when data is being loaded into memory the user can specify either a file name for the data or designate the exact RAM address where the data is to be placed.

The sequencer memory is loaded with information pertaining to the order in which modulation data is to be accessed from RAM.

A few terms are now defined to help explain the operation of the sequencer:

- WAVE SEGMENT. Waveform data which is stored at consecutive addresses in RAM.
- SCAN. A single pass through a wave segment.
- PACKET. One or more scans through a wave segment. For each packet, the following parameters must be specified by the user:

  –File name or RAM address & length of wave segment to be scanned.
  –Number of scans through the wave segment.
  –Method of advancing to the next packet in the sequence, either AUTO, BUS, or GROUP. (See *Packet Advance Triggering* in section 9 for a complete description of these packet advance modes.)

- SEQUENCE. Combination of one or more packets.

In the example of figure 4-4, a sequence of four packets has been defined. (The user can specify up to 2048 packets in a sequence.) Waveform data from the modulation memory is accessed in the following manner:

1. Wave segment AWAVE is scanned twice. Once completed, the sequencer AUTOmatically advances to the next packet.

2. Wave segment FWAVE is scanned five times. Once completed, the sequencer AUTOmatically advances to the next packet.

3. Wave segment AWAVE is scanned 1000 times. Once completed, the sequencer AUTOmatically advances to the next packet.

4. Wave segment DWAVE is scanned 65000 times. Since this is the last packet in the sequence, the sequencer AUTOmatically advances back to the first packet and the sequence repeats.

Note that not all wave segments stored in the modulation memory need to be accessed. (BWAVE, CWAVE, and EWAVE were not used in this example.) Also note that it is possible to access a wave segment more than once within a sequence (AWAVE) and that it does not matter what order the wave segments are stored in RAM.

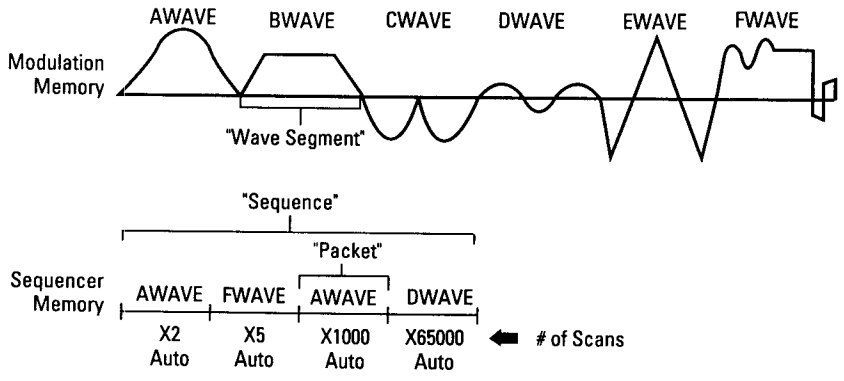


Figure 4-4. HP FASS memory sequencing in Model 10.

Address Generation Rate. The sequencers in HP FASS are driven using the CLK/4 signal in the MDS. This means that a new address is generated every 29.8 ns. However, it is possible to decrease the address generation rate by using an *address rate divider*. Figure 4-5 shows conceptually how this works.

For *each* of the four sequencers in the MDS, the user can specify that address generation is to be slowed down by some factor N, where N can be 1 or any even integer between 2 and $2^{15}-2$. As the access rate of the modulation RAM is reduced, the time duration of the modulation data being accessed is increased. With this feature, it is therefore possible to generate signals with dramatically different AM, PM, FM, and frequency hop rates. It should be noted, however, that address rate reduction leads to coarser time resolution of the waveform data. Thus, it is possible for some modulation profiles to have a stair-stepped appearance as the time between data samples becomes greater and greater.

NOTE: Due to the data multiplexing scheme used in conjunction with the AM/PM and PM memories of HP FASS, special care must be taken when loading data into these memories if the address rate divider is set to some value other than 1 for the corresponding sequencers. See the *FASS Subsystem* section of the *HP FASS System Operating Manual* or the *Stretching Data* section of the *Waveform Generation Language Programming Manual* for complete details.

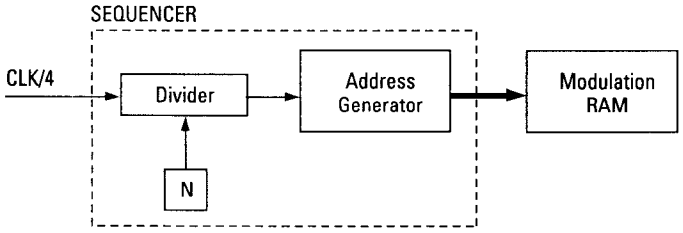


Figure 4-5. Address rate division is used to decrease the address generation rate of the sequencers in the MDS.

Dynamic Data. While the four sequencers in HP FASS serve as internal address generators, it is possible to bypass any or all of them and provide modulation RAM addresses to the system from an external source. (See figure 4-6.) This is referred to as *dynamic data* mode. In this configuration, the HP FASS functions like a traditional microwave synthesizer with external modulation inputs. In this case, however, the inputs are digital rather than analog. This data can be accepted either synchronously or asynchronously. Refer to Product Note 8791-1 *Real-time Control of HP FASS* for an in-depth discussion of this real-time modulation capability.

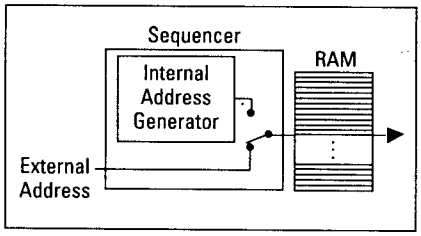


Figure 4-6. In dynamic data mode, the internal address generator is bypassed and the user provides address data externally.

Sequencer Memories (Models 7/11/21)

The sequencing capabilities of Models 7/11/21 are a superset of those present in Model 10. The Advanced Dynamic Memory Sequencer (ADMS) adds the following features:

(1) Loop packets
(2) Expanded sequencer memory
(3) IMMEDIATE packet advance modes
(4) Dynamic sequencing
(5) Dynamic sequence download

Figure 4-7 shows how the enhanced memory sequencing works. As is the case in Model 10, a sequence of packets defines the order in which the data in the modulation memories is to be accessed. Whereas in Model 10 these packets must be played out sequentially, the ADMS in Models 7/11/21 provides an additional level of flexibility; the inclusion of *loop packets* allows portions of this sequence to be repeated. In addition, up to 1024 distinct sequences can be established.

In the example of figure 4-7, three sequences have been defined. These are arbitrarily given sequence ID numbers of 1, 380, and 700. Sequence #1 consists of 4 regular packets and three loop packets, Sequence #380 has 3 regular packets and one loop packet, and Sequence #700 contains 4 regular packets and 2 loop packets. A total of 17 packets (regular and loop) have thus been defined. The user can specify up to 32768 packets across all sequences.

When Sequence #1 is being executed, waveform data from the modulation memory is accessed in the following manner:

1. Wave segment AWAVE is scanned twice. Once completed, the sequencer AUTOmatically advances to the next packet.

2. Wave segment FWAVE is scanned five times, then wave segment AWAVE is scanned 1000 times. This 2-packet combination is then repeated a total of 10 times as a result of the loop packet which has been established around the regular packets. The sequencer advances AUTOmatically within the loop.

3. Finally, wave segment DWAVE is scanned 65000 times. Since this is the last packet in the sequence, the sequencer AUTOmatically advances back to the first packet and the sequence repeats.

In the scenario described above, the specified number of scans for each regular packet or loop packet are completed before the sequencer advances to the next packet, as specified by the AUTO parameter for each packet. With the ADMS of Models 7/11/21, it is possible to advance to the next packet in the sequence on-the-fly through the use of an external TTL trigger signal or via an HP-IB interrupt; advancement from one packet to the next can be done without waiting for the specified number of wave segment scans to be completed. This is referred to as the *immediate* packet advance mode.

While three separate sequences (1, 380, 700) have been defined in this example, only one of these sequences can be executed at a time. The other sequences are executed using the *sequence jump* mechanism of the ADMS. Using either an HP-IB bus command or external data ports on the rear panel of the MDS, the user can jump to a different sequence on-the-fly by simply supplying a sequence ID number and a jump trigger. Such jumps can be programmed to take place either immediately or after the last packet of the current sequence has been completed.

This feature, referred to as *dynamic sequencing*, is advantageous in those applications for which the signals to be generated are known a priori, but their exact timing is not known. Multi-mode radar simulation and time-multiplexed multi-emitter simulation are two such applications. For an in-depth discussion of this dynamic sequencing capability, refer to Product Note 8791-1, *Real-time Control of HP FASS*.

Finally, with Models 7/11/21 it is possible to be executing one sequence of packets while another sequence is being loaded over HP-IB. Thus, signal scenarios can be calculated on-the-fly and continuously loaded into the hardware without interruption of the current test signal. This is referred to as *dynamic sequence download*.

Address Generation Rate. The ADMS of Models 7/11/21 allows for address rate division when accessing the modulation RAMs. (See figure 4-5 and accompanying discussion for Model 10 on page 23.) In this case, N can by any integer from 1 to 2^{16}.

Dynamic Data. The dynamic data mode of Models 7/11/21 is the same as that found in Model 10. (Refer to discussion on page 24.) In this case, there is four times as much memory which can be accessed via external data lines.

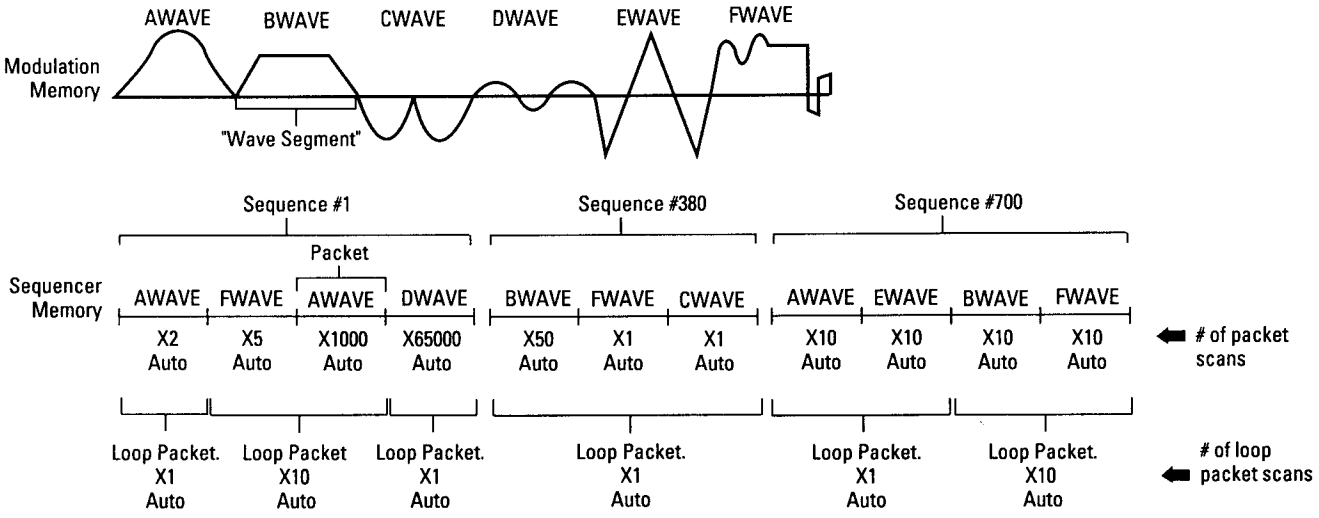


Figure 4-7. HP FASS memory sequencing in Models 7/11/21.

FM Adder and Digital Signature Analysis (DSA)

The FM Adder circuitry in the MDS adds the 30-bit data word from the FM memory to the 30-bit data word from the ACS Frequency Field of the FREQ memory. (See figure 4-1.) The resulting 30-bit data word represents the instantaneous IF frequency to be generated by the ACS. This data is passed to the ACS every 29.8 ns.

In Models 7/11/21, the FM Adder also includes *phase-coherent correction circuitry*, as shown in figure 2-4. This feature allows the HP FASS to switch frequencies in either a phase-continuous *or* a phase-coherent fashion, depending on the application. A thorough discussion of this subject is deferred until section 8 (page 51), as a general understanding of the sine computer circuitry in the ACS is first required.

The DSA capability is used during self-test to verify the operation of the MDS and by the system diagnostics to isolate faults to a field replaceable unit (FRU).

MDS Clocks

CLK/4 (29.8 ns) and CLK/8 (59.6 ns) signals are supplied to the MDS from the Agile Carrier Synthesizer. The CLK/4 signal is used to clock the address generators in each sequencer and to latch AM/PM, PM, and FREQUENCY data from the MDS into the ACS. The CLK/8 signal is used to latch data from the AUC Frequency Field and the AUC Attenuator Field of the FREQ memory from the MDS into the AUC.

The CLK/8 signal in the MDS is also used to latch any external triggers which come into the HP FASS system. This subject is covered separately in section 9, *Triggering and Synchronization of HP FASS.*

Direct Memory Access (DMA)

The DMA interface in the Modulation Data Source allows high-speed transfer of digital signal data from the Math Accelerator Board in the Smart Interface to the modulation memories in the MDS.

HP-IB and Microprocessor

The HP-IB and microprocessor board provides communication with the Smart Interface and controls the operation of the MDS.

The Agile Carrier Synthesizer (ACS) uses digital modulation data provided by the MDS to generate an IF carrier signal with the specified modulation characteristics. For Models 10/11/21, this signal should be bandlimited to a frequency range of 13.5 to 58 MHz, as this is the bandpass range of the SAW filter in the Agile Upconverter. As shown in figure 5-1, the ACS consists of the following:

- Sine Computer & DAC
- System Clocks and Digital Signature Analysis (DSA)
- HP-IB and Microprocessor

Note: The block diagram of figure 5-1 is modified slightly for Model 7. See appendix A for a complete description of the Model 7 configuration.

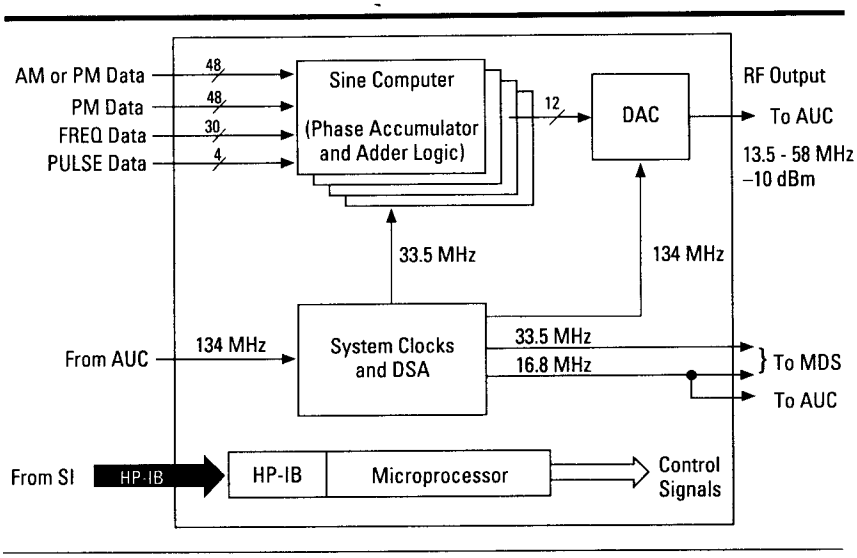


Figure 5-1. HP 86791A Agile Carrier Synthesizer block diagram.

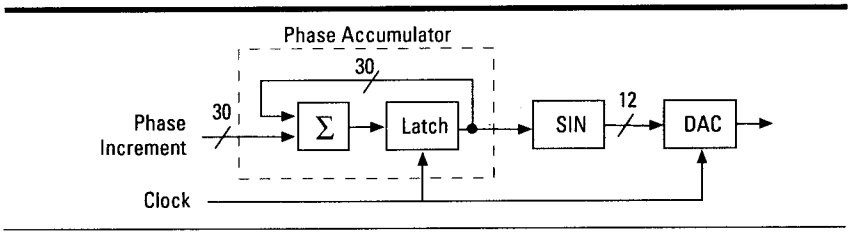


Figure 5-2. Phase accumulator in the Agile Carrier Synthesizer.

Sine Computer & DAC

The sine computer digitally combines the AM/PM, PM, PULSE, and instantaneous carrier frequency data from the MDS to produce a 12-bit binary data stream. This digital data stream is then passed through the DAC to produce an analog IF signal. The next paragraph briefly describes the digital synthesis process. After that, the process will be described in detail.

The heart of the sine computer is a digital phase accumulator (integrator) which computes the phase angle of the carrier signal on a point-by-point basis using the carrier frequency and FM data. The rate of phase accumulation varies in proportion to the desired output frequency, with higher frequencies accumulating phase faster than lower ones. Phase modulation is added by summing the accumulator output with the PM data stream. The SIN of this instantaneous phase is then found to give an instantaneous signal amplitude, which is further modulated by the AM data stream. Finally, the PULSE data determines whether the signal will be ON or OFF at any given instant in time.

To better understand the block diagram of the sine computer, we begin simply with those blocks which are required to generate a CW signal. Additional blocks will then be added as we successively add frequency, phase, amplitude and pulse modulation to the signal.

CW Signal Generation

Figure 5-2 shows the basic block diagram of the phase accumulator. As shown, the input to the phase accumulator is a phase increment. This number represents the amount by which the phase of the signal needs to be advanced during the next clock cycle. The signal phase from the previous clock cycle is latched, fed back, and added to this phase increment to give the next signal phase. For instance, assuming an initial accumulator value of 0° and a constant phase increment of 45°, the phase values 45°, 90°, 135°, 180°, 225°, 270°, 315°, 0°, etc. will be output.

Given the instantaneous phase of our signal, the instantaneous amplitude is found by taking the SIN of that phase value. (The phase data is applied to a sine look-up table stored in ROM.) The DAC then converts this amplitude to an analog voltage level.

For a constant phase increment, the frequency of the resulting output signal from the ACS is given by

ACS Carrier Frequency = Clock Frequency ÷ (360° ÷ Phase Increment)

For a given output frequency, the required phase increment is given by

*Phase Increment = (ACS Carrier Freq ÷ Clock Freq) *360°*

(Note that data coming from the MDS into the phase accumulator is actually frequency data. This data stream is automatically converted to phase increment data by the system. As this process is transparent to the user, it is not shown on the sine computer block diagrams that follow.)

Figure 5-3 shows a 16.8-MHz and a 27.92-MHz signal generated using constant phase increments of 45° and 75°, respectively.

Two points should be noted here regarding phase accumulation. First, there is no requirement that the phase increment be constant over time. The rate of accumulation can be changed simply by changing the phase increment. This is in fact how frequency modulation is achieved.

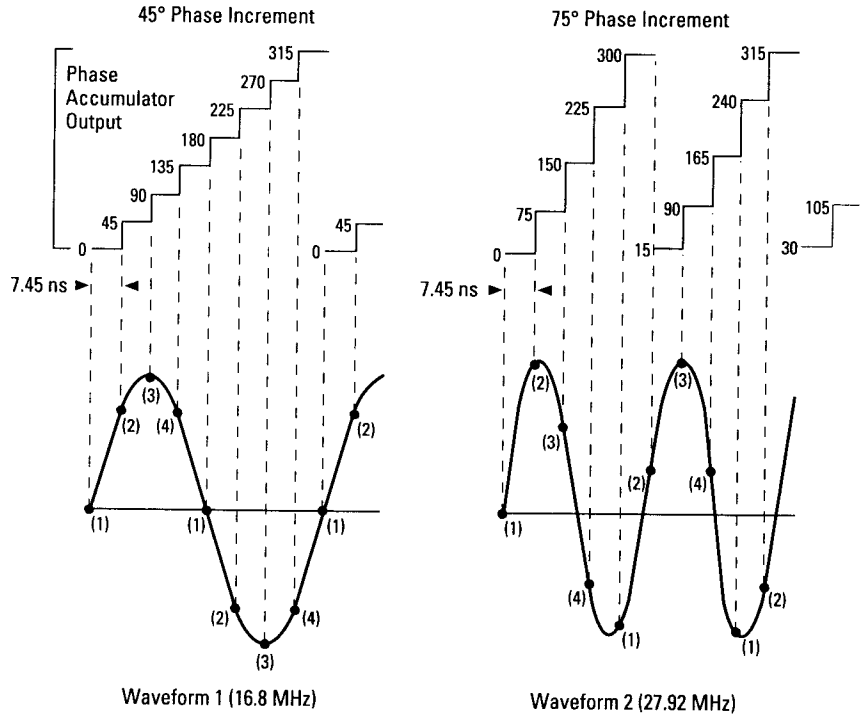


Figure 5-3. Phase accumulator output.

Secondly, phase accumulation is an integration process. This implies that any change in frequency at IF with ACS is done in a *phase-continuous* manner, whether that change be continuous (as in slowly-varying FM) or abrupt (as in frequency hopping).

In Models 7/11/21, correction circuitry in the FM Adder of the MDS can be used to fool the phase accumulator into a *phase-coherent* mode; the user has a choice of either phase-continuous *or* phase-coherent frequency switching at IF. The various frequency switching capabilities of the HP FASS systems are explained in detail in section 8 (page 51).

Frequency Resolution of HP FASS

As explained in the previous section, frequency data is specified by a 30-bit field in the Modulation Data Source. These 30 bits are carried throughout the phase accumulation process in ACS, resulting in an overall system frequency resolution of 0.125 Hz when using the internal 134 MHz clock ($2^{27} / 2^{30} = 0.125$ Hz).

In general, frequency resolution of an N-bit phase accumulator is calculated using the following equation:

Freq Resolution = Clock Freq ÷ Phase Accumulator Modulus

Note that this resolution is determined solely by the digital circuitry of the HP FASS system and is not dependent on any analog circuitry.

Frequency Modulation (FM)

The addition of frequency modulation to our signal is done using the FM Adder in the MDS. A 30-bit data word from the FM memory is added to a 30-bit word from the ACS Frequency Field of the FREQ memory. Again, this is done on a point-by-point basis. The data at the output of the FM Adder represents the instantaneous IF carrier frequency, and it is this data which is routed to the sine computer in ACS.

Phase Modulation (PM)

As shown in figure 5-4, the addition of phase modulation is a straightforward process; the PM data stream is simply added to the output of the phase accumulator.

Amplitude Modulation (AM)

The addition of amplitude modulation to our signal is conceptually a little more difficult to understand. Vector signal diagrams will be used to explain the underlying theory.

Figure 5-5 shows the vector representation of an AM signal which is specified by the general equation $x(t) = A(t)sin(\omega t)$. At any instant in time the signal has a certain amplitude $A(t)$, which is given by the length of the vector, and a certain phase, which is given by the angle ωt. The rate at which this vector rotates determines the carrier frequency of the signal, and the rate at which the length of the vector changes determines the AM rate.

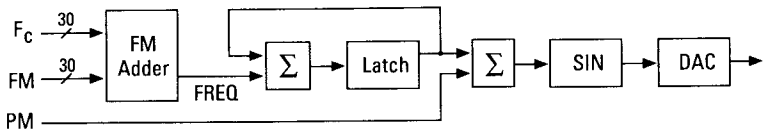


Figure 5-4. Phase Accumulator with FM and PM added.

As the following derivation shows, we can also represent this signal as the summation of two vectors:

$x(t) = A(t)sin(wt)$

Let $B(t) = arccos[A(t)]$
Or $A(t) = cos[B(t)]$

Then $x(t) = cos[B(t)]sin(wt)$
$= 0.5sin[wt+B(t)] + 0.5sin[wt - B(t)]$

As shown in figure 5-6, a signal vector with phase ωt is found by the addition of two other vectors, V1 and V2, with phase angles of $\omega t + B(t)$ and $\omega(t) - B(t)$, where $B(t)$ is the ARCCOS of the AM function $A(t)$. As the angle $B(t)$ changes, the amplitude of the signal vector changes. Thus, the AM rate of the signal is given by the rate at which the angle $B(t)$ changes. The carrier frequency is still determined by the rotational rate of the signal vector.

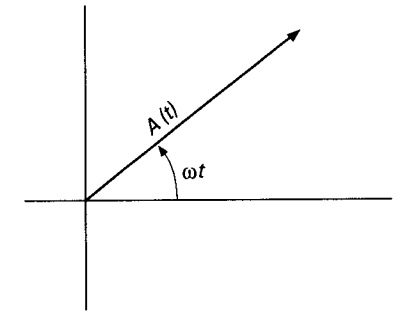


Figure 5-5. Vector representation of an AM signal.

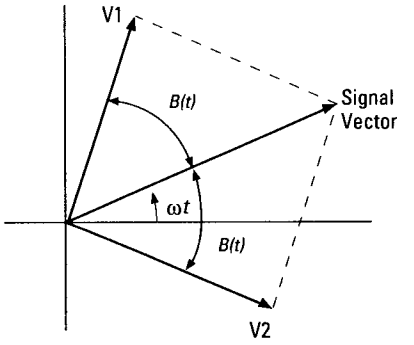


Figure 5-6. Creating an AM signal using vector addition.

Figure 5-7 shows the actual hardware implementation of this AM technique in HP FASS. The AM data stream is first passed through an ARCCOS function to create a *B(t)* data stream. This data is then split into two paths, one for each vector (V1 and V2) in figure 5-6. In accordance with the final equation above, these two data streams are added to and subtracted from the ωt data stream, passed through a SIN function, then added to give the final digital signal.

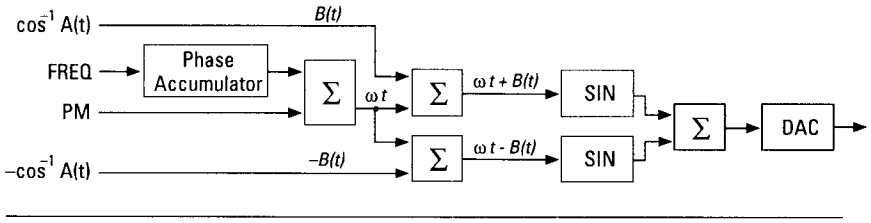


Figure 5-7. Hardware implementation of AM in HP FASS.

It should be noted that the ARCCOS function is actually applied to the AM data stream *during download*, that is, the data that is stored in the AM/PM memory of the MDS is the ARCCOS of the data that was originally sent to the system.

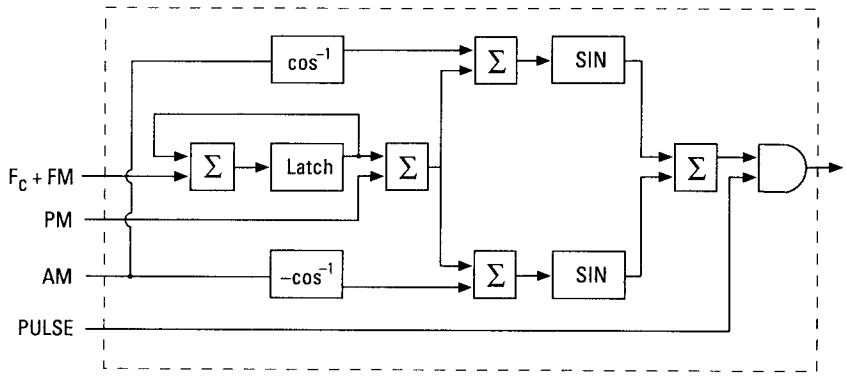


Figure 5-8. Conceptual block diagram of the sine computer in HP FASS. The ARCCOS function is actually applied to the AM data stream during download, before it is stored in the AM/PM modulation RAM.

NOTE: The above discussion only applies when the AM/PM modulation memory in the MDS is being used in AM mode. When this memory is being used in PM mode, the data stored is not passed through an ARCCOS function and the data stream is simply summed at the output of the phase accumulator as if it came from the PM memory.

The complete block diagram of the sine computer in ACS is shown in figure 5-8. Note that the output of the sine computer is turned on and off in accordance with the PULSE data stream.

Data Multiplexing in ACS

As mentioned in the previous section, data from the MDS is clocked at a CLK/4 (33.55 MHz) rate. However, through data multiplexing in the ACS an effective system clock rate of 134 MHz (2^{27} Hz) is achieved. For illustrative purposes, we'll trace the signal flow of AM data through the system to see how this multiplexing scheme is implemented.

Referring back to figure 5-1, we see that 48 bits of AM data are passed to the ACS during each CLK/4 cycle. These 48 bits actually contain four consecutive 12-bit AM data points. Also note from figure 5-1 that there are four sine computer channels, each operating as previously described.

Figure 5-9 shows how the 48 bits of AM data are mapped into the four sine computer channels. Remember that only the AM data streams are being shown here. Each sine computer actually has four inputs: AM/PM, PM, FREQUENCY, and PULSE. Also shown is the method by which those four channels are multiplexed to give a single output.

The sine computers accept, process, and output four data points in parallel every 29.8 ns (CLK/4). Two multiplexers, operating at the full clock rate of 134 MHz, serialize these points into two data streams, one stream containing the data from channels 1 and 3 and the other containing data from channels 2 and 4. These two data streams are then merged using a data latch, resulting in a new 12-bit data point every 7.45 ns.

(Referring back to figure 5-3, notice that each point of the output signal is numbered. This number indicates which sine computer channel that particular data point originates from.)

Note that the Modulation Data Source also routes four PM data points (48 bits) and four PULSE data points (4 bits) to the ACS during each CLK/4 cycle. This data is similarly multiplexed. Therefore, like AM, the effective update rate of phase and pulse modulation is also 134 MHz; the amplitude, phase, and on/off condition of the signal can be changed every 7.45 ns.

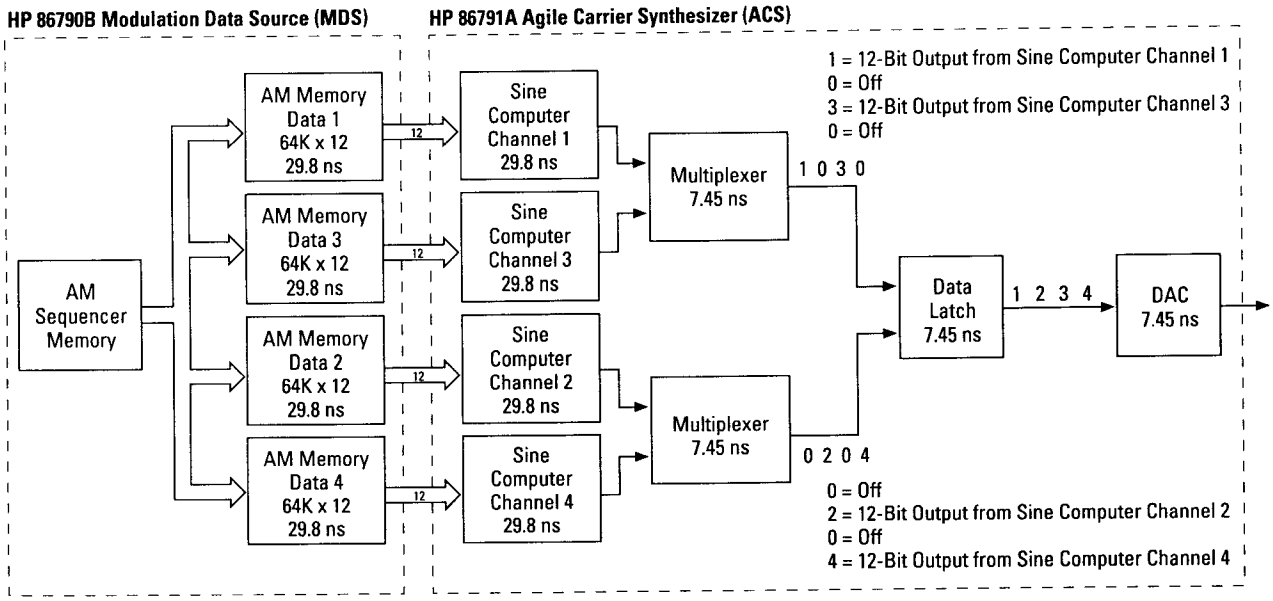


Figure 5-9. Sine computer channel multiplexing.

With FREQUENCY data, however, only one 30-bit data point is passed to the ACS during each CLK/4 cycle. Consequently, that one data point is fed to all four sine computer channels simultaneously. As a result, the instantaneous frequency of the signal can only be changed every 29.8 ns.

System Clocks and Digital Signature Analysis (DSA)

A 134 MHz (2^{27} Hz) clock is supplied to the ACS from the Agile Upconverter. (See figure 5-1.) This is the internal system clock and is used by the ACS to clock the multiplexers and the DAC. In ACS, this clock is also divided by 4 to produce a 33.55 MHz clock (CLK/4) and by 8 to produce a 16.8 MHz clock (CLK/8). The CLK/4 signal is used internally to clock the sine computers and is also passed on for use in the MDS. The CLK/8 signal is routed to both the MDS and the AUC.

The DSA capability is used during self-test to verify the operation of the ACS and by the system diagnostics to isolate faults to a field replaceable unit (FRU).

HP-IB and Microprocessor

The HP-IB and microprocessor board provides communication with the Smart Interface and controls the operation of the ACS.

The Agile Upconverter (AUC) of Models 10/11/12 takes the modulated IF signal from the ACS and places it anywhere in a 10-to-3000 MHz range in under 100 ns, typical. Due to filtering during the upconversion process, the frequency content of the input signal should be bandlimited to the 13.5-to-58 MHz range.

Figure 6-1 shows the general upconversion scheme used by the AUC. The signal is first mixed against two fixed LO signals of 268 MHz and 1728 MHz, respectively. After each upconversion one sideband of the resultant signal is filtered and the other sideband is passed on. A third upconversion places the signal in the 7.7-8.2 GHz range. Unlike the previous upconversions, however, the LO used here is agile, with a frequency resolution of 4.2 MHz (2^{22} Hz). After filtering, the signal is then downconverted with another agile LO hopping in 537 MHz (2^{29} Hz) steps, resulting in a final signal frequency in the 10-to-3000 MHz range.

As shown in figure 6-2, the AUC consists of the following:

- 537 MHz Reference Generator
- RF Reference
- Microwave Reference and Switch
- Direct Synthesizer
- Linear Upconverter and Fast Attenuator
- Downconverter and Slow Attenuator
- Digital Data Delay
- HP-IB and Microprocessor

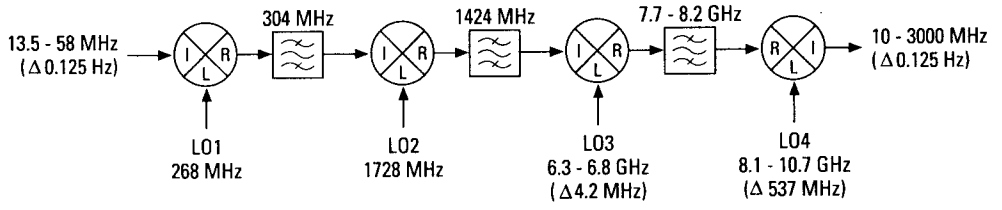


Figure 6-1. The Agile Upconverter uses a four-stage mixing chain, consisting of three upconversions and one downconversion.

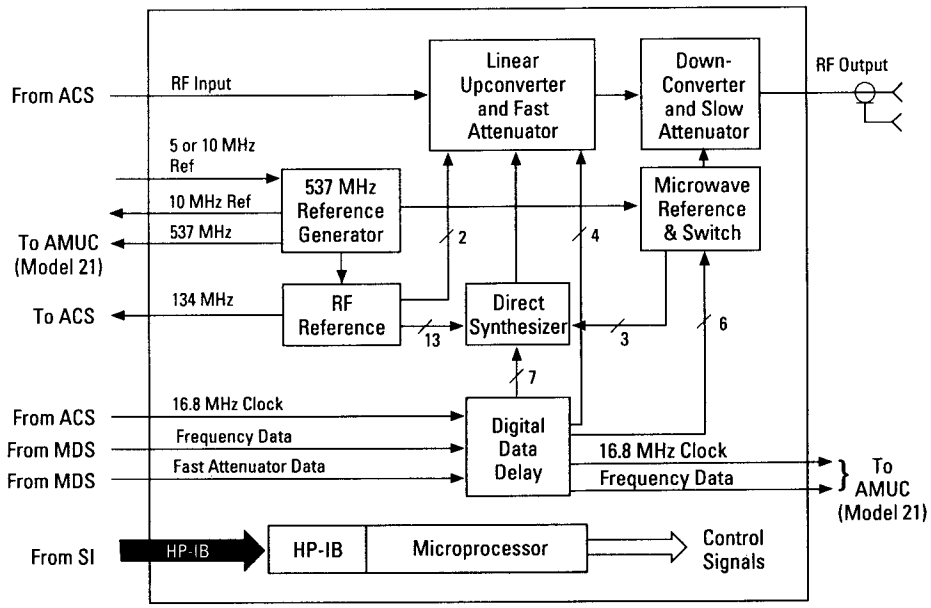


Figure 6-2. HP 86792A Agile Upconverter block diagram.

537 MHz Reference Generator

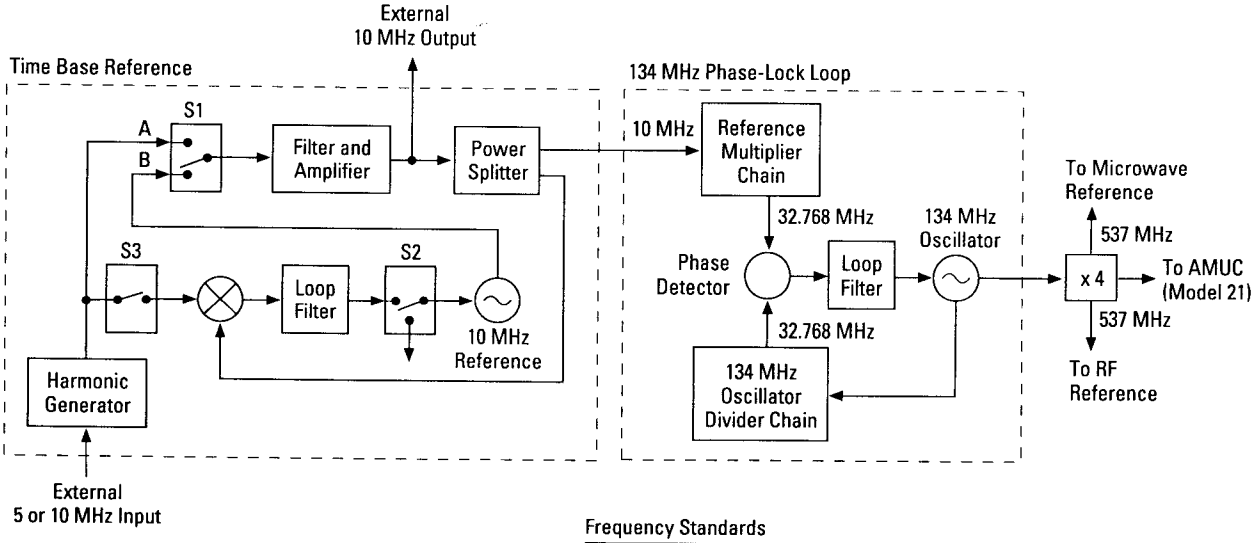
The starting block for any synthesizer is its reference source (figure 6-3). The 537 MHz generation circuitry phase-locks a 134.217728 MHz (2^{27} Hz) oscillator to a 10 MHz reference signal to produce a stable, low phase noise signal at 536.870912 MHz (2^{29} Hz). The 537 MHz output signal is then split and routed to the RF Reference and Microwave Reference circuitry. In Model 21, this signal is also passed on to the Agile Microwave Upconverter. All RF and microwave references in the HP FASS system are derived from this one signal.

The internal 10 MHz reference is also routed to a BNC connector on the rear panel of the AUC and has a level of between 7 and 10 dBm (typically 8.5 dBm). Output impedance is 50 Ω nominal. This signal can be used to supply a phase-locked reference to external equipment.

If desired, an external 5 or 10 MHz reference can be used instead of the internal 10 MHz reference. (The ultimate close-in phase noise of the HP FASS system is dependent on the reference signal used.) The choice of frequency standard is made via the FREQUENCY STANDARD switch on the rear panel of the AUC. There are three options available:

- INTERNAL—Internal 10 MHz reference. Phase noise is determined by the internal 10 MHz reference oscillator.

- EXT ±0.05 PPM—Internal 10 MHz reference phase-locked to an external 5 or 10 MHz reference. External source should be within 0.05 ppm of its nominal frequency or else the phase-locked loop will not lock. Phase noise is determined by the internal 10 MHz reference oscillator. This switch setting is intended for use with a house standard or other cesium or rubidium standard.



Frequency Standards

	S1	S2	S3
(1) Internal Standard	B	OFF	-
(2) Internal Standard Locked to External Std (0.05 ppm)	B	ON	ON
(3) External Standard (5 ppm)	A	-	OFF

Figure 6-3. Agile Upconverter 537 MHz Reference Generator.

• EXT ± 5 PPM—External 5 or 10 MHz reference. The internal 134 MHz oscillator is phase-locked directly to the external source. External source should be within 5 ppm of its nominal frequency or else the phase-locked loop will not lock. Phase noise at offsets less than 100 Hz is determined by the external reference oscillator. This switch setting is intended for use with another instrument that has similar or superior phase noise and frequency stability specifications.

RF Reference

The RF Reference circuitry (figure 6-4) takes the 537 MHz reference signal and generates 15 spurious-free RF reference signals. Two of these signals are the 268 MHz and 1728 MHz fixed LO signals used to drive the first two upconversion mixers. The other 13 signals are fed to the switches in the Direct Synthesizer circuitry.

In addition, the 537 MHz reference is divided to produce the 134 MHz clock signal used throughout the HP FASS system. This signal is routed to the rear panel of the AUC.

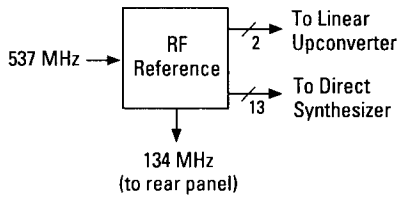


Figure 6-4. RF Reference circuitry in the AUC.

Microwave Reference & Switch

Like the RF Reference section, the Microwave Reference and Switch block uses the 537 MHz reference signal to generate additional spurious-free reference signals (figure 6-5). Three of these signals are fixed in frequency (1074 MHz, 1074 MHz, and 4295 MHz) and are fed to the Direct Synthesizer. A fourth signal serves as the agile LO for downconversion in the output section of the AUC. This LO comes from a comb of frequencies ranging from 8.1 to 10.7 GHz in 537 MHz steps generated with a step-recovery diode. Control lines from the Digital Data Delay block are then used to select one of the six possible frequencies for the LO signal.

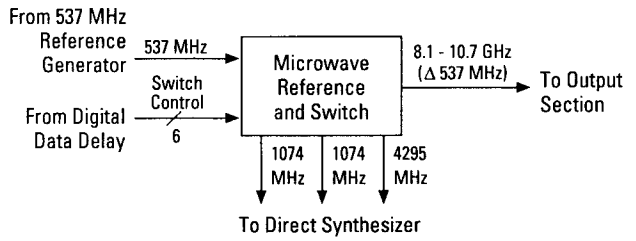


Figure 6-5. Microwave Reference and Switch circuitry in the AUC.

Direct Synthesizer

The Direct Synthesizer provides the high-speed frequency switching capability of the HP FASS system. Through a series of switches and mixers, an agile LO signal in the 6.3-6.8 GHz range is generated in 4.2 MHz (2^{22} Hz) steps. This signal drives the third mixer in the Linear Upconversion path. Good spurious performance is maintained through proper selection of LO signal frequencies.

As shown in figure 6-6, reference signals from the RF Reference and Microwave Reference blocks are routed to the various switches and mixers. Control lines from the Digital Data Delay circuitry drive these switches to select the appropriate reference signals needed to produce a given LO signal.

Note that at the output of each mixer there is a discrete number of possible frequencies. The result is a total number of 128 possible LO signals from the Direct Synthesizer.

It is also important to note that the RF and microwave reference signals are present at all times. They can be thought of as free-running oscillators that are switched in and out as needed. As a result, frequency hopping using the Agile Upconverter is a *phase-coherent* process. See section 8 for a more complete discussion of this subject.

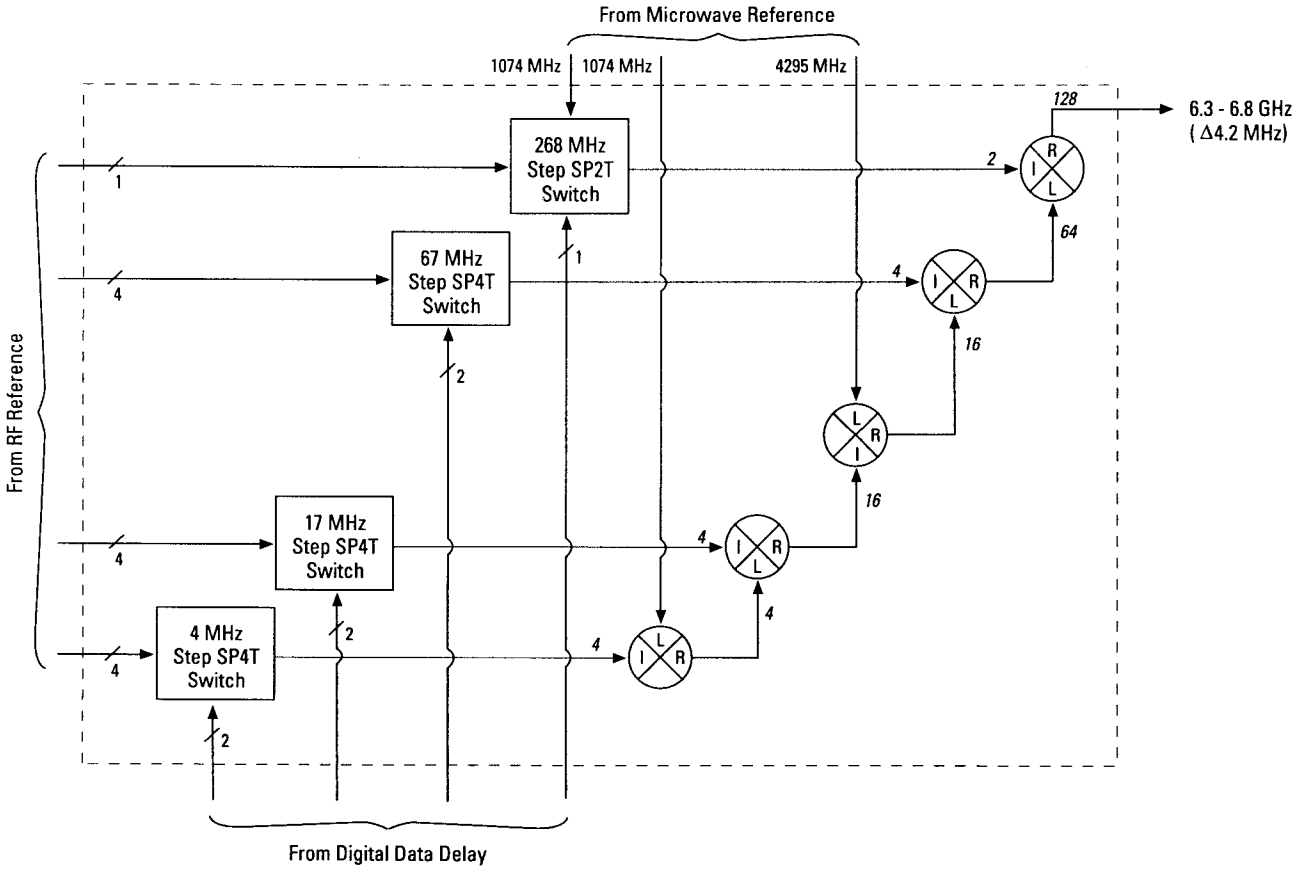


Figure 6-6. Direct Synthesizer in the Agile Upconverter. Numbers in italics indicate the number of possible frequencies available at each point in the diagram.

Linear Upconverter and Fast Attenuator

Figure 6-7 shows a block diagram for the Linear Upconversion path in the AUC. As mentioned previously, upconversion is done in three steps, with the LO signals for the two fixed upconversions being provided by the RF Reference block and the LO for the agile upconversion being provided by the Direct Synthesizer. The signal is appropriately filtered after each mixing process.

Of particular significance is the bandpass SAW filter used after the first upconversion. By filtering the upconverted signal rather than the IF input, improved spectral purity of the final output signal is assured. This HP-proprietary filter was designed to have excellent phase linearity and extremely sharp rolloff characteristics*. Figure 6-8 shows the amplitude transfer function of this filter. As this is a SAW device, it is important to note that there is approximately a 1 µs analog delay through the filter.

Following the SAW filter is a Fast Attenuator, also known as the Fast Level Control (FLC). This diode-switched attenuator switches from 0 to 90 dB in 6.02 dB steps in under 250 ns. The Digital Data Delay block provides appropriate control lines for the FLC.

*See "Development of an Ultra-Flat SAW Filter Module and Its Application to HP FASS", 1989 IEEE Ultrasonics Symposium, by T.L. Bragwell, C.A. Johnson, R.C. Bray, and S. Carp.

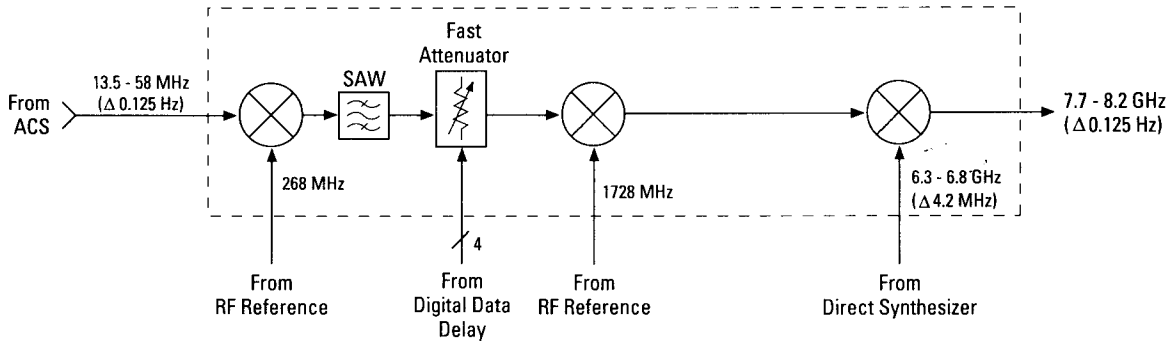


Figure 6-7. Linear Upconversion path in the AUC.

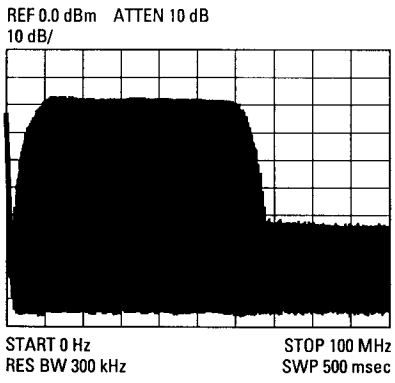


Figure 6-8. Amplitude transfer function of the bandpass SAW filter in AUC (shown at IF).

Downconverter and Slow Attenuator

As shown in figure 6-9, the output section of the AUC contains a downconverter, amplifier, and slow attenuator. The downconverter mixes the output of the Linear Upconverter section against the agile LO provided by the Microwave Reference block in order to generate a signal in the final 10-to-3000 MHz frequency range. After filtering, an output amplifier then boosts the final output power level to a maximum specified level of +10 dBm.

In addition, a slow-switching output attenuator can be set anywhere from 0 to 70 dB in 10 dB steps. Controlled from the microprocessor, this attenuator is used to optimally position the 90 dB range provided by the FLC in the Linear Upconversion path.

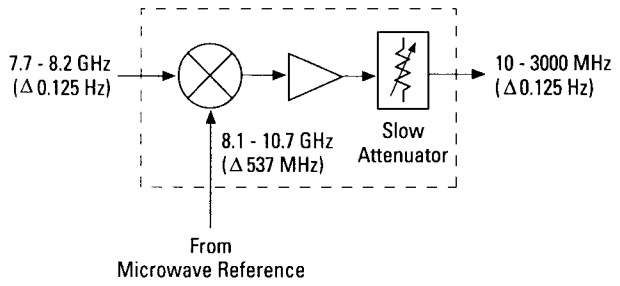


Figure 6-9. Output section of the Agile Upconverter.

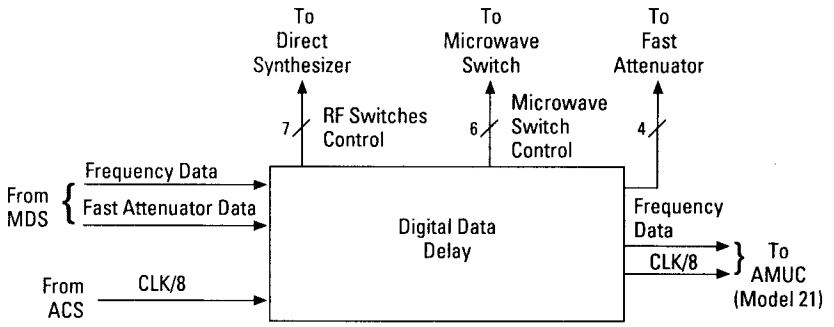


Figure 6-10. Digital Data Delay in the AUC.

Digital Data Delay

The Digital Data Delay (figure 6-10) receives data from the AUC Frequency Field and the AUC Attenuator Field in the MDS and uses it to control the RF switches, microwave switch, and fast attenuator in the Agile Upconverter. This data is digitally delayed to compensate for analog delays through the Linear Upconversion path, thereby assuring that all frequency and amplitude switching is synchronous.

The delay circuitry uses the CLK/8 signal from the ACS. Data from the AUC Frequency Field and the AUC Attenuator Field of the FREQ modulation memory is therefore latched into the AUC every 59.6 ns.

Note: In Model 21, upconversion is done with both the AUC and the Agile Microwave Upconverter. Although data loaded into the AUC Frequency Field is still sent to the AUC, only the lower-order bits are actually used by the AUC. The most significant bits are stripped off and passed on to the AMUC to set its upconversion band. This process is transparent to the user. In addition, the digital data delay is modified in Model 21 to support calibrated output levelling. This feature is described in detail on page 40.

HP-IB and Microprocessor

The HP-IB and Microprocessor board provides communication with the Smart Interface and controls the operation of the AUC.

Detailed Block Diagram

Figure 6-11 shows a complete block diagram for the signal generation portion of the AUC. As previously mentioned, the Direct Synthesizer provides an LO signal with 128 possible frequencies, and the Microwave Reference circuitry provides an LO signal with 6 possible frequencies. As a result, the Agile Upconverter as a whole performs agile upconversion using one of 768 possible LO signals.

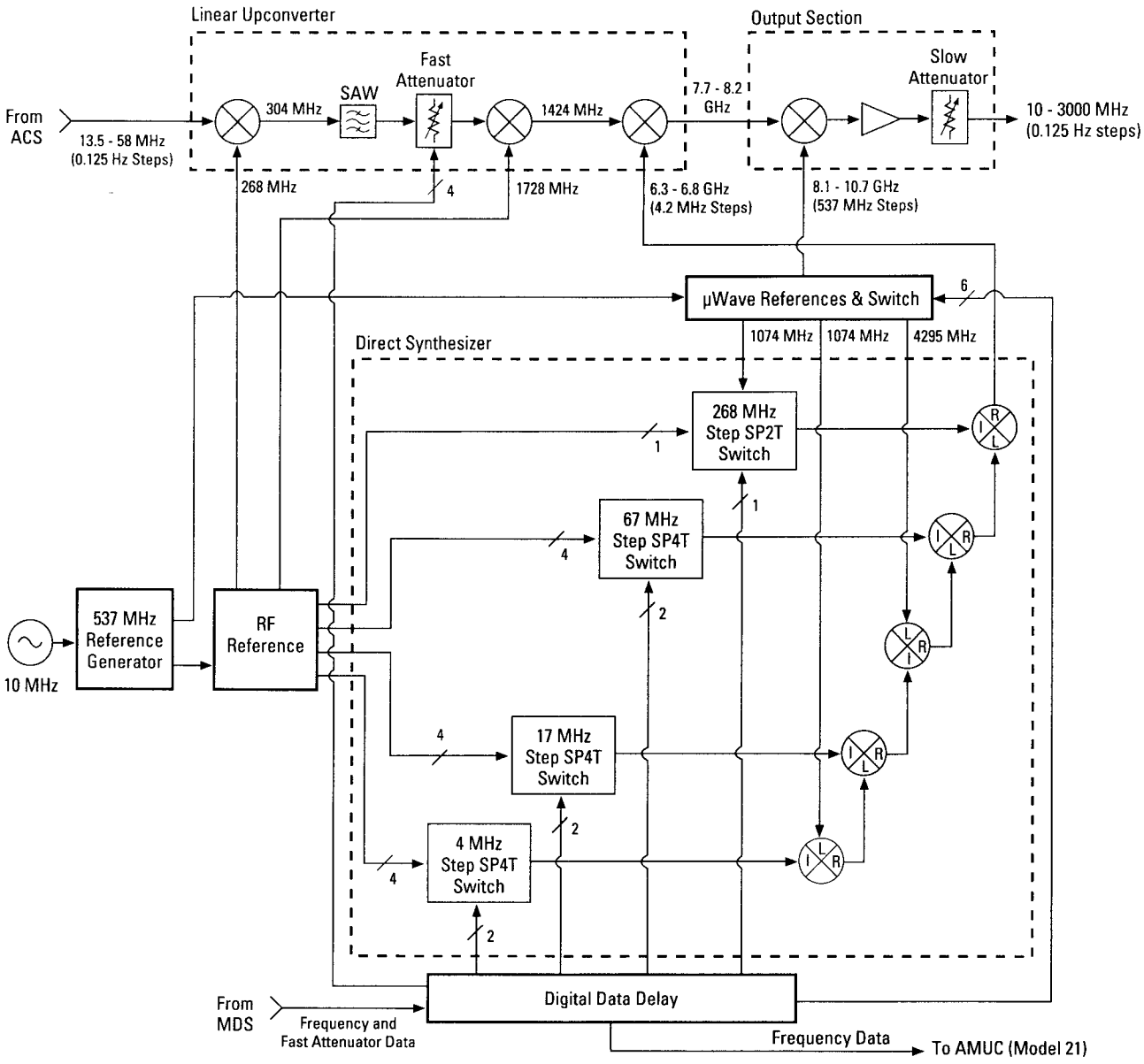


Figure 6-11. Agile Upconverter Block Diagram.

Level Calibration in Model 21

As the frequency range of the Model 21 system is extended to 18 GHz with a second upconverter, it becomes more difficult to maintain a reasonable output power flatness over that entire range. For this reason, the AUC in the Model 21 system has additional circuitry which, when combined with a detector in the Agile Microwave Upconverter and control software in the Smart Interface, provides a mechanism for producing a calibrated output level from the system. This additional circuitry is shown in figure 6-12.

During system calibration, a closed loop is established whereby the RF signal from AMUC is passed through a diode detector and its output level is measured. Using the results of this measurement, internal software algorithms determine how a GaAs FET attenuator in the AUC upconversion chain should be adjusted to give a specified level at the system output. A binary search is used to find the proper attenuator setting. This setting, along with the corresponding carrier frequency information, is recorded in a level calibration table within the Digital Data Delay block of the AUC. This entire procedure is repeated across the frequency range of interest.

During normal system operation, the level calibration table is continually accessed using the frequency data coming into the AUC from the MDS. The calibration data is used to control the attenuator in real-time. (This attenuator is continuously variable over a 20 dB range in less than 100 ns.) Through this fine-level adjustment, the output power from the system remains flat to within ±2 dB across all frequencies.

Note: For increased accuracy, it is possible to bypass the internal detector in the AMUC and use an external power meter for calibration measurements. This method is useful for calibrating the effects of flatness error caused by external cabling and other components.

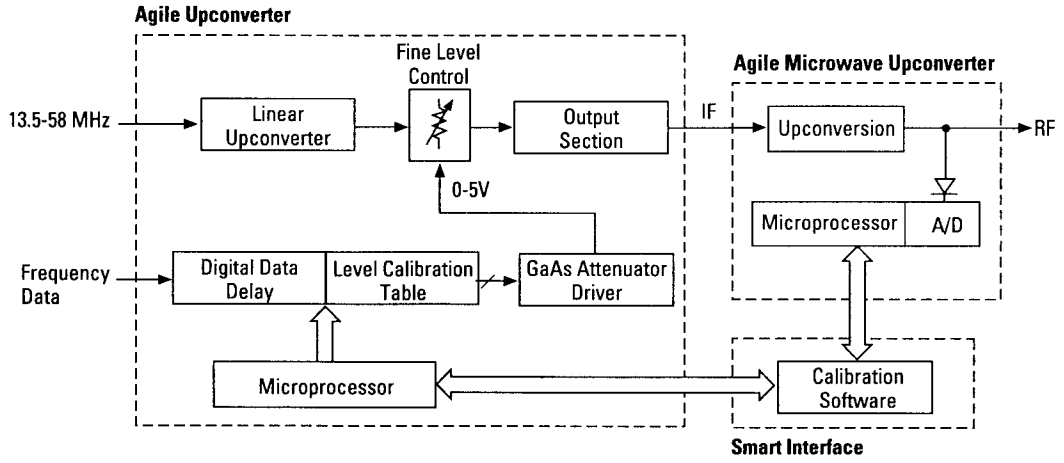


Figure 6-12. Level calibration circuitry in Model 21.

The Agile Microwave Upconverter (AMUC) of Model 21 takes a modulated RF signal from the AUC and places it anywhere in a .05-to-18 GHz range while maintaining 0.125 Hz frequency resolution and 100 ns typical switching speed. The full range is covered by two outputs, 50 to 500 MHz and 0.5 to 18 GHz, with agile switching between them.

Figure 7-1 shows the general upconversion scheme used by the AMUC. The input signal is first split into two paths. A low-pass filter in the first path allows frequencies in the 50-to-500 MHz range to pass directly to the first output. Signals in the 1.61-to-2.95 GHz range are upconverted or downconverted to the 0.5-18 GHz range using an agile LO and passed to the second output. Input signals which are between 500 MHz and 1.61 GHz are ultimately filtered out in both paths and thus are not used.

As shown in figure 7-2, the AMUC consists of the following:

- Input Section
- RF Output Section
- Agile LO Section
- 0.5-12.4 GHz Linear Upconverter
- 12.4-18 GHz Linear Upconverter
- Microwave Output Section
- Digital Frequency Control
- HP-IB and Microprocessor

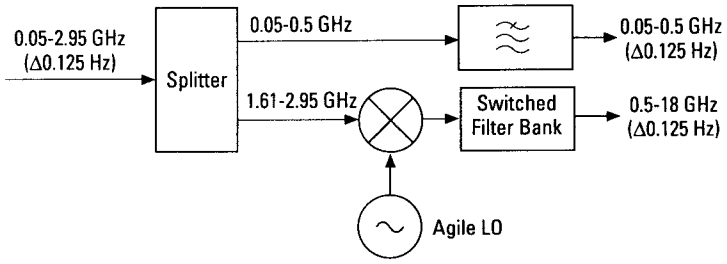


Figure 7-1. General upconversion scheme of the Agile Microwave Upconverter.

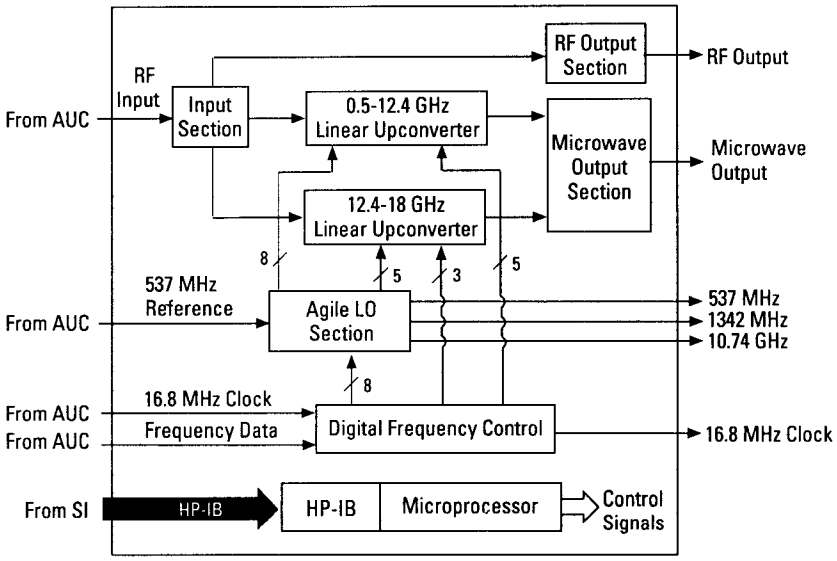


Figure 7-2. HP 86793A Agile Microwave Upconverter block diagram.

Input Section

As shown in figure 7-3, the input section of the AMUC consists of a slow-switching input attenuator and an RF splitter. The step attenuator can be set anywhere from 0 to 11 dB in 1 dB steps. Controlled from the microprocessor, this attenuator is used to optimize the power level into the upconversion path.

The splitter takes the RF input signal from AUC and splits it into three separate signal paths. One of these paths is fed directly into the RF Output Section. The other two signals are sent to the 0.5-12.4 GHz and 12.4-18 GHz Linear Upconverter blocks, respectively. These two paths will eventually be recombined in the Microwave Output Section.

Again, input signals which are between 500 MHz and 1.61 GHz are ultimately filtered out in both the RF and microwave paths and thus are not used.

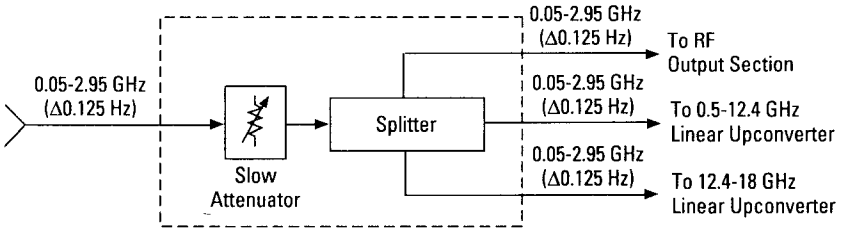


Figure 7-3. Input section of the Agile Microwave Upconverter. Input signals in the 0.5-1.61 GHz range are ultimately filtered and therefore not used.

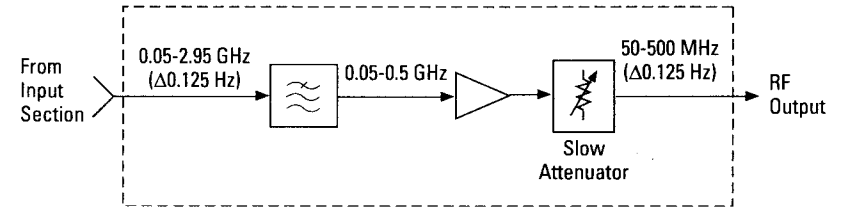


Figure 7-4. RF Output section of the AMUC.

RF Output Section

Figure 7-4 shows the RF Output Section of the AMUC. A low-pass filter is first used to eliminate all frequency components above 500 MHz. After filtering, an output amplifier boosts the final output power level to a maximum specified level of +10 dBm.

In addition, a slow-switching output attenuator can be set anywhere from 0 to 110 dB in 10 dB steps. Controlled from the microprocessor, this attenuator is used to optimally position the dynamic range of the input signal.

Agile LO Section

The Agile LO section, shown in figure 7-5, is the heart of the upconverter. Using a step-recovery diode, the Microwave Reference Generator takes a 537 MHz reference signal from the AUC and generates a comb of frequencies ranging from 10.7 to 22.8 GHz in 1342 MHz steps. This frequency comb is appropriately filtered to provide 13 spurious-free reference signals, which are distributed to microwave switches within the Agile LO section. Control lines from the Digital Frequency Control block drive these switches in real-time to select the signals to be used as LOs for the 0.5-12.4 GHz and 12.4-18 GHz Linear Upconverter blocks. Good spurious performance is maintained at the AMUC output through proper selection of these LO signal frequencies.

In addition to the LO signals, the Microwave Reference Generator also provides 537 MHz, 1342 MHz, and 10.74 GHz reference signals to the rear panel of the AMUC.

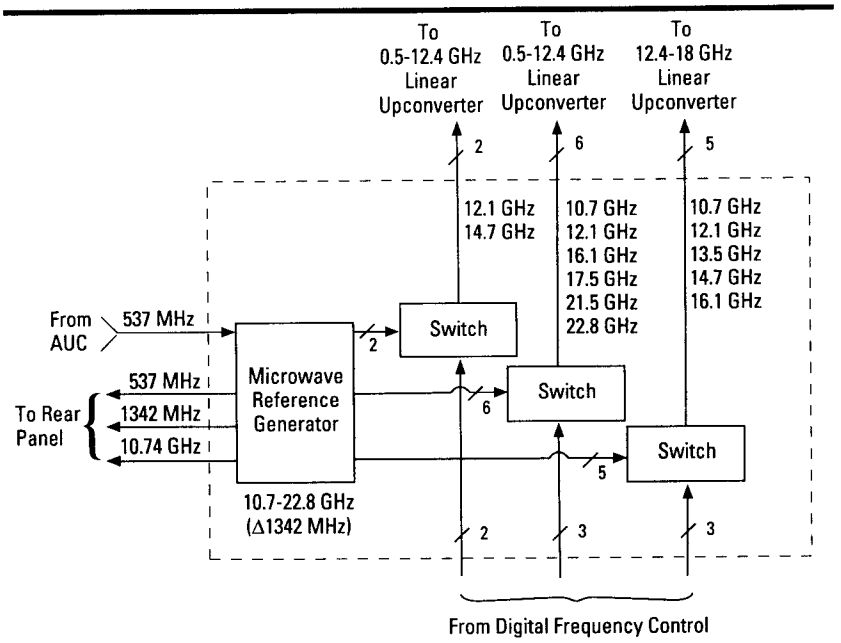


Figure 7-5. Agile LO section of the AMUC.

0.5-12.4 GHz Linear Upconverter

Upconversion to the microwave frequency range is done in two separate Linear Upconverter sections. The first of these sections places the input signal in the 0.5-12.4 GHz band. As shown in figure 7-6, frequency translation is actually done in two stages, with the LO signals for each mixing process coming from the Agile LO section. Switched filter banks are used to eliminate the upper sideband and LO feedthrough after each of the mixers and are driven with control lines from the Digital Frequency Control block. For output frequencies outside the 0.5-12.4 GHz band, this upconversion path is switched off.

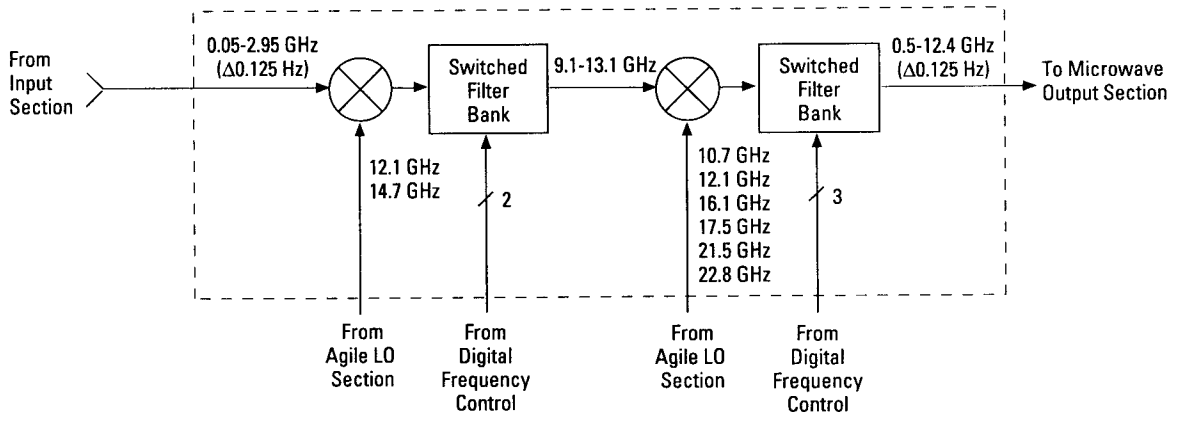


Figure 7-6. 0.5-12.4 GHz Linear Upconverter section in the AMUC.

12.4-18 GHz Linear Upconverter

The second Linear Upconverter section places the input signal in the 12.4-18 GHz frequency range. (See figure 7-7.) Again, the local oscillator for the mixer comes from the Agile LO Section and control signals from the Digital Frequency Control block drive a switched filter bank. In this case, the lower sideband and LO feedthrough are filtered out after the mixing process. For output frequencies outside the 12.4-18 GHz band, this upconversion path is switched off.

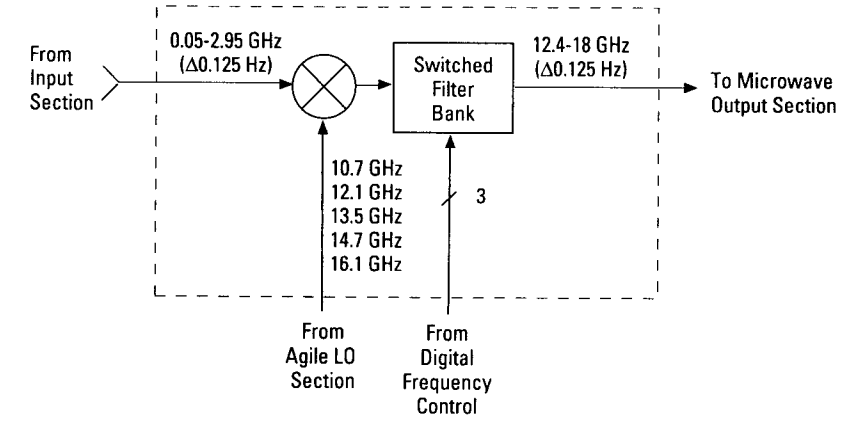


Figure 7-7. 12.4-18 GHz Linear Upconverter section in the AMUC.

Microwave Output Section

The Microwave Output section of the AMUC is shown in figure 7-8. Input signals from the two Linear Upconverter sections are first combined to produce a single signal path. A wideband amplifier then boosts the final output power level to a maximum specified level of +10 dBm. Similar to the RF Output section, a slow-switching output attenuator can then be set anywhere from 0 to 110 dB in 10 dB steps.

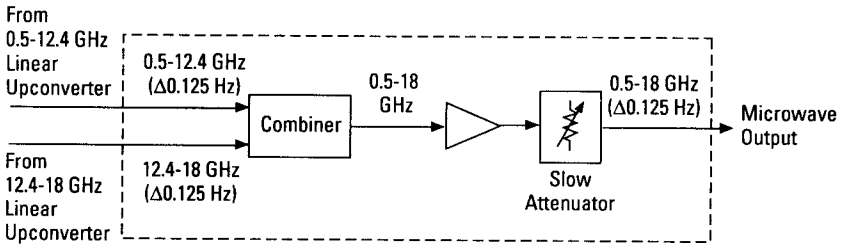


Figure 7-8. Microwave Output section of the AMUC.

Digital Frequency Control

The Digital Frequency Control (figure 7-9) receives frequency data from the Agile Upconverter and uses it to control the microwave switches in the Agile LO section and the switched filter banks in the two Linear Upconverter sections of the AMUC. This data is digitally delayed to compensate for small analog delays through the microwave upconversion path.

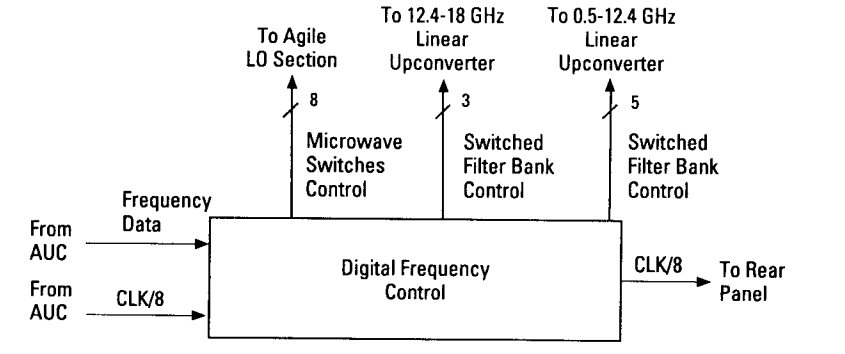


Figure 7-9. Digital Frequency Control in the AMUC.

The control circuitry uses the CLK/8 signal from the AUC. Frequency data from the AUC is therefore latched into the AMUC every 59.6 ns.

HP-IB and Microprocessor

The HP-IB and Microprocessor board provides communication with the Smart Interface and controls the operation of the AMUC.

Detailed Block Diagram

Figure 7-10 shows a complete block diagram of the signal generation portion of the AMUC. Again, the full frequency range of the AMUC is covered by two outputs, 50-500 MHz and 0.5-18 GHz, with agile switching between them.

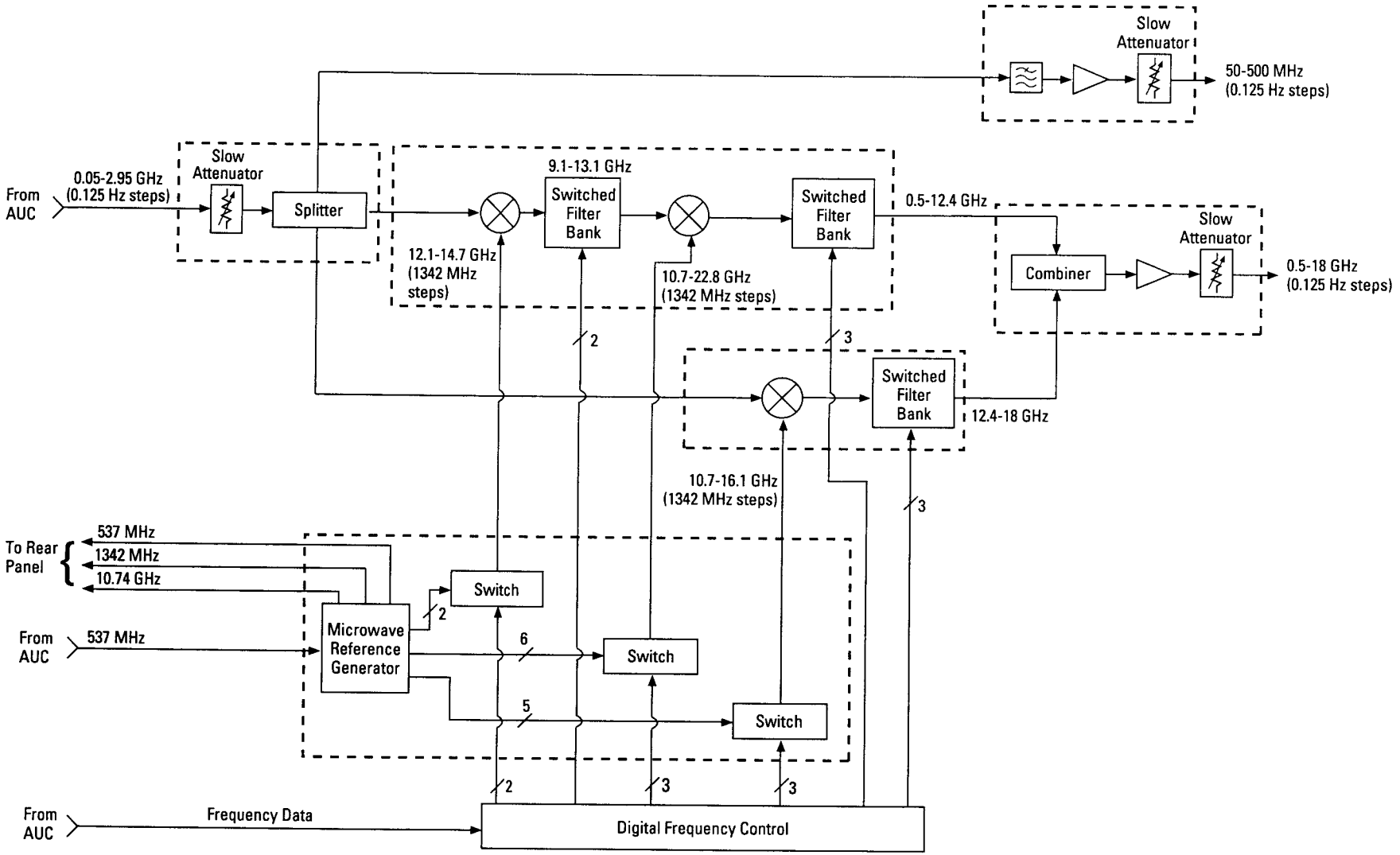


Figure 7-10. Agile Microwave Upconverter block diagram.

Given a firm understanding of the internal architecture of HP FASS, it is important to now look at some system-level issues. It is the system level at which all users must interface.

The following subjects are covered in this section:

- System Clocks
- System Markers
- System Bandwidth
- System Output Power
- Frequency Resolution
- Phase Resolution
- Amplitude Resolution
- Phase-Coherent Switching vs. Phase-Continuous Switching
- Frequency Switching Speed
- System Data Security

System Clocks

Figure 8-1 shows the distribution of clock signals throughout the HP FASS system. As explained previously, the main 134 MHz system clock is generated within the Agile Upconverter. This signal is then routed to the Agile Carrier Synthesizer, where it is divided down to produce CLK/4 and CLK/8 signals. The CLK, CLK/4, and CLK/8 signals are used to clock all digital circuitry in the HP FASS system.

It is also possible to clock HP FASS using an external source rather than the internal one. It should be noted, however, that *the analog circuitry in the AUC always uses the internal clock*, even if the rest of the system is being clocked externally. For further details, refer to Product Note 8791-5, *Tips on External Clock Operation with HP FASS.*

Note: There is no Agile Upconverter in the Model 7 system. A 134 MHz oscillator and a 10 MHz timebase reference are instead located in the Agile Carrier Synthesizer.

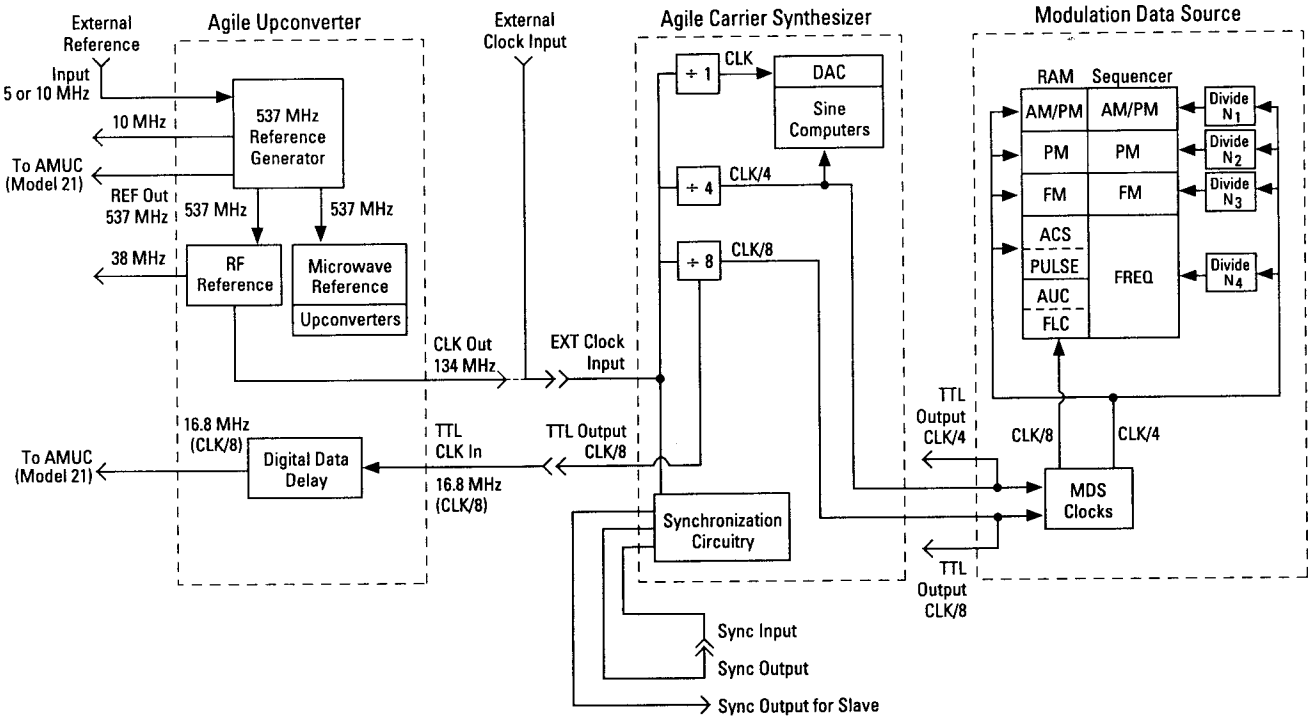


Figure 8-1. HP FASS clock distribution.

System Markers (Model 10)

The Model 10 system provides a unique set of rear-panel marker outputs. Each output generates a TTL-level pulse which is synchronous with a specific sequencer event in the Modulation Data Source. Refer to page 22 for a complete operational description of these sequencer events.

There are 16 possible marker signals available from the Model 10 system, four each from the four sequencers in the MDS. The four markers are:

- *Address Equals.* A pulse is generated whenever a specified RAM address is generated by the sequencer. This marker is programmable.
- *Sequence Start.* A pulse is generated at the beginning of each sequence repetition.
- *Packet Start.* A pulse is generated at the beginning of each packet.
- *Scan Start.* A pulse is generated at the beginning of each scan within a packet.

While there are four markers available from each sequencer, only two of them are actually brought out to the rear panel of the MDS. When shipped from the factory, these are the Sequence Start marker (labeled as Event Marker 1) and the Address Equals marker (labeled as Event Marker 2). See figure 8-2. The user can reconfigure the system so that any two of the four markers for each sequencer are available at the rear panel. Consult section 2-8, *Configuring the Event Markers*, in the *HP FASS Model 10 System Service Manual* for the proper procedure.

It is important to note that while these markers are synchronous with sequencer events in the MDS, they are not synchronous with the RF output of the system. This is due to the digital and analog delay of signal data through the system. Consequently, there is a fixed latency period of approximately 2.4 µs from the time when a marker is generated to the time when the corresponding RF signal arrives at the system RF output.

System Markers (Models 7/11/21)

The Model 7/11/21 systems provide a unique set of rear-panel marker outputs. Each output generates a TTL-level pulse which is synchronous with a specific sequencer event in the Modulation Data Source. Refer to page 24 for a complete operational description of these sequencer events.

There are 32 possible marker signals available from the Model 7/11/21 systems, eight each from the four sequencers in the MDS. The eight markers are:

- *Address Equals.* A pulse is generated whenever a specified RAM address is generated by the sequencer.
- *Sequence Start.* A pulse is generated at the beginning of each sequence repetition.
- *Packet Start.* A pulse is generated at the beginning of each regular packet.
- *Scan Start.* A pulse is generated at the beginning of each scan within a regular packet.
- *Packet ID Start.* A pulse is generated at the beginning of each marked regular packet.
- *Packet ID.* A pulse is generated and remains high during the entire duration of a marked regular packet.
- *Loop Start.* A pulse is generated at the start of each loop packet.
- *None.* The marker output is disabled.

While there are eight markers available from each sequencer, only two of them are actually brought out to the rear panel of the MDS. These two markers are referred to as Event Marker 1 and Event Marker 2. (See figure 8-2.) Through software, the user can reconfigure which two of the eight markers for each sequencer are to be generated.

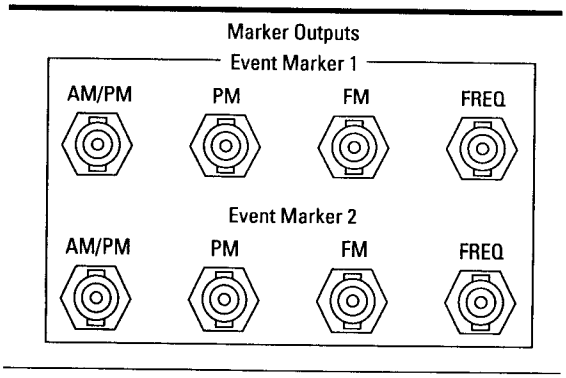


Figure 8-2. HP FASS System Markers.

System Bandwidth

(Note: The following discussion pertains only to HP FASS Models 10/11/21. Refer to Appendix A for a discussion of system bandwidth in the Model 7 Baseband FASS.)

The instantaneous modulation bandwidth of HP FASS is specified at 40 MHz. In general, the bandwidth of the output signal will be equal to the bandwidth of the IF signal coming from the ACS. (The Agile Upconverter only translates that bandwidth over the frequency range of the system). Remember, however, that this signal can contain frequencies anywhere from 13.5 MHz to 58 MHz, as this is the effective passband of the SAW filter in the AUC. That's a range of 44.5 MHz. Why, then, is the specification set at 40 MHz?

Figure 8-3 shows the situation at hand. Assuming a symmetrical spectrum, it is only possible to achieve a bandwidth of 44 MHz if the center frequency of our IF signal is set to about 36 MHz. However, in order to precisely set the carrier frequency of our overall output signal it is usually necessary to fine-tune the ACS IF carrier frequency over a 4.2 MHz range about this ideal center frequency of 36 MHz. (4.2 MHz is the frequency resolution of the Agile Upconverter.) As a result, it is possible to have an IF carrier frequency as low as 33.55 MHz (2^{25} Hz) and as high as 37.75 MHz ($22^{25} + 2^{22}$ Hz). In each case, the maximum bandwidth is then limited to about 40 MHz.

System Output Power

(Note: The following discussion pertains only to HP FASS Models 10/11/21. Refer to Appendix A for a discussion of output power in the Model 7 Baseband FASS system.)

In Models 10/11, the overall output power from the HP FASS system is determined by four factors:

(1) The amplitude values loaded into the AM/PM memory of the Modulation Data Source.

(2) The signal gain through the Agile Upconverter.

(3) The setting of the Fast Level Control (FLC) in the Agile Upconverter (0-90 dB, 6.02 dB steps).

(4) The setting of the output attenuator in the Agile Upconverter (0-70 dB, 10 dB steps).

In Model 21, three other factors also contribute to the overall output power from the system:

(5) The setting of the input attenuator in the Agile Microwave Upconverter (0-11 dB, 1 dB steps).

(6) The signal gain through the Agile Microwave Upconverter.

(7) The setting of the output attenuator in the Agile Microwave Upconverter (0-110 dB, 10 dB steps).

The AM values loaded into the MDS determine the output power from the ACS into the AUC. With all ones loaded (full amplitude), ACS puts out about -10 dBm. With 0.5 loaded (half voltage), the power decreases by 6 dB to −16 dBm.

As one might expect, the actual gain through the Agile Upconverter and the Agile Microwave Upconverter varies with frequency. However, by measuring the output power of the system as a function of frequency, it is possible to generate a calibration table of correction factors which can be used to provide a flat output signal across all frequencies. This is in fact the function of the LEVEL CAL utility in the System Instrument-on-a-Disk (SID) software. (See the *HP FASS System Operating Manual* for complete details.)

In Models 10/11, the correction factors generated by the LEVEL CAL must be applied to the AM data that is downloaded to the system. In Model 21, the correction factors are automatically applied to the signal with special built-in auto-levelling circuitry. (For more complete details, see discussion on page 40.)

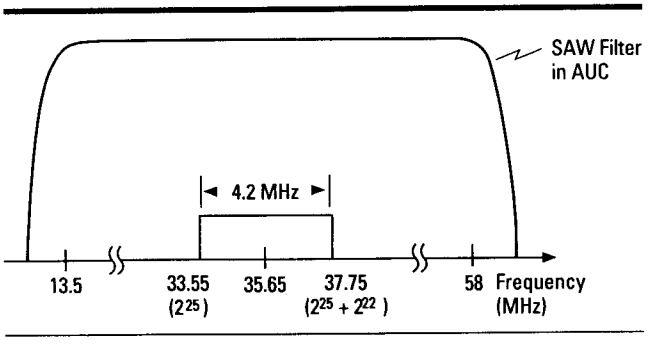


Figure 8-3. HP FASS bandwidth limitations.

For a calibrated output, we can now think of the AUC and the AMUC as having constant gains through them. As a figure of merit, these gains are about 22 dBm for Models 10/11 and 16 dBm for Model 21.

In general, the following equation should be used to calculate the system output power from Models 10/11:

*Output Level = 22 dBm + 20*LOG(AM Data with Level Cal Factor) – FLC Setting – AUC Output Attenuator Setting*

For Model 21, the output power is given by

*Output Level = 16 dBm + 20*LOG(AM Data) – FLC Setting – AUC Output Attenuator Setting – AMUC Input Attenuator Setting – AMUC Output Attenuator Setting*

For example, suppose the following parameters are being used in a Model 11 system:

AM Value = 0.4 (includes level calibration factor)
FLC Setting = 12 dB
AUC Output Attenuator = 10 dB

The output power is then calculated as

*Output Level = 22 + 20*LOG(0.4) –12 –10 = –7.95 dB*

Note that it is generally a good idea to have the FLC set to at least 12 dB, as this reduces the power into the output amplifier in the AUC and minimizes harmonic distortion at the output of the AUC.

The output power from Models 10/11 is specified to be –107 dBm to +10 dBm, while the output power from Model 21 is specified to be –100 dBm to +10 dBm. (See figure 8-4).

Frequency Resolution

As explained in section 5, the frequency resolution of the HP FASS system is 0.125 Hz when using the internal 134 MHz clock.

Phase Resolution

As mentioned previously in section 4, PM data is specified using 12-bit words in the Modulation Data Source. Consequently, there are 4096 possible phase states over 360°. The phase resolution of the system is therefore 360°/4096 0.088° = 0.0015 radians.

Amplitude Resolution

As was the case with PM data, AM data is also specified using 12-bit words. However, one of these bits is used as a sign bit (AM data range is ±1), and approximately one bit is lost due to the ARCCOS function applied to the data. As a result, there are only 10 effective bits available, giving approximately 56 dB of dynamic range.

With a digital system, it is important to realize that the effective amplitude resolution in dB changes as a function of amplitude level; the resolution of low-level signals is coarser than that of higher-level signals.

The graph in figure 8-5 shows this effect for the HP FASS system. At an AM attenuation level of 0 dB (corresponding to a value of 1.0 loaded into the AM/PM memory),

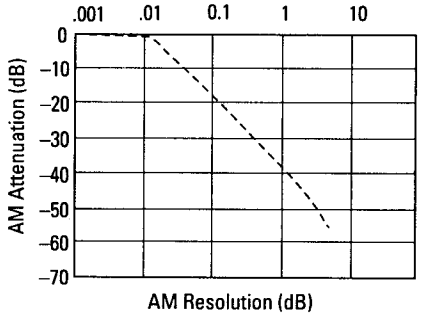


Figure 8-5. Effective amplitude resolution as a function of AM attenuation level for HP FASS.

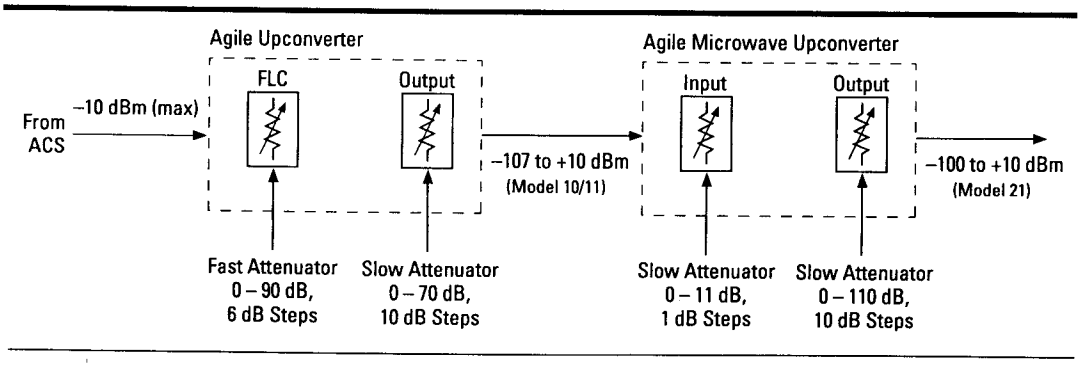


Figure 8-4. HP FASS System Output Power.

the effective resolution is about 0.002 dB. For 56 dB of attenuation (corresponding to 0.0016 loaded into the AM/PM memory), the effective resolution is changed to 6 dB. This phenomenon should be considered when generating amplitude-modulated signals with HP FASS.

Figure 8-6 shows an antenna scan signal for which a sin(x)/x amplitude profile was loaded into the AM/PM memory. At the higher amplitude levels of the main lobe and first few sidelobes the effects of quantization are barely noticeable. However, as the sidelobe levels get smaller and smaller the amplitude resolution gets coarser. Figure 8-7 shows the amplitude profile for these sidelobes.

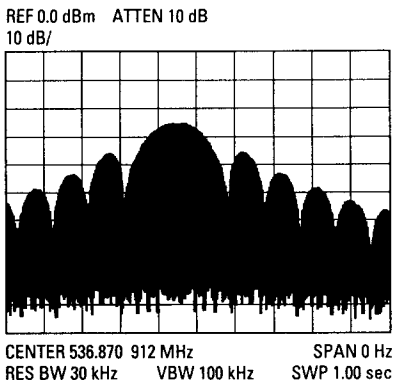


Figure 8-6. Amplitude profile of an antenna scan signal generated with HP FASS.

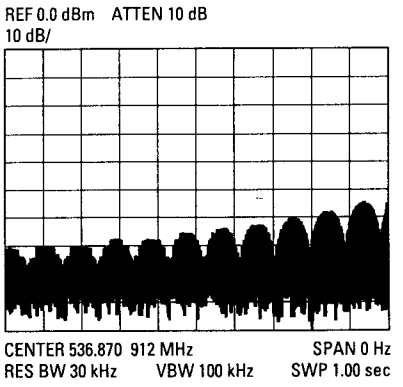


Figure 8-7. Low-level sidelobes of antenna scan signal.

As an alternative, it is possible to use the Fast Attenuator (FLC) in the AUC to generate low-level signals while maintaining good amplitude resolution with the AM data.

Phase-Coherent Switching vs. Phase-Continuous Switching

The HP FASS system supports both phase-continuous frequency switching and phase-coherent frequency switching. Figure 8-8 depicts a phase-continuous frequency change. As the frequency changes from F1 to F2 and back to F1 again, the instantaneous phase of the carrier signal varies in a continuous, smooth fashion; the phase trajectory of the signal (shown as a solid line) has no discontinuities. (Note: For simplicity, the phase trajectories of F1 and F2 are each drawn starting with a zero phase offset. In practice, each frequency can have a random or defined starting phase.)

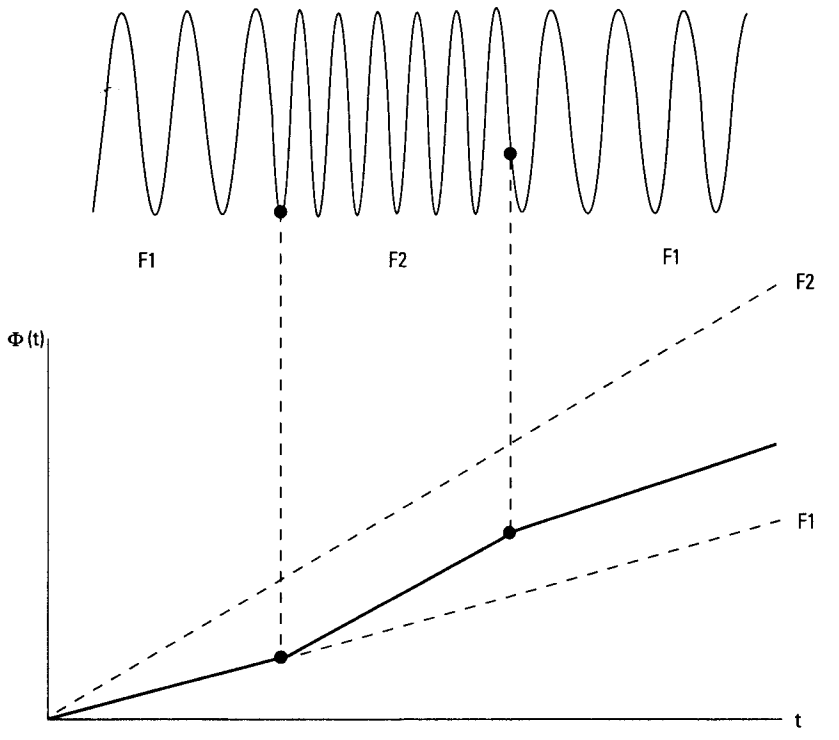


Figure 8-8. A phase-continuous signal has no phase discontinuities at the switching points.

In HP FASS (all models), the digital phase accumulator in the Agile Carrier Synthesizer (ACS) automatically generates a phase-continuous carrier signal. (See pages 27-28 for a complete discussion of the phase accumulator.) The rate of phase accumulation varies in proportion to the input frequency (figure 8-9), with higher frequencies accumulating phase faster than lower ones. As the phase accumulation process is essentially a digital integration, any change in frequency is done in a phase-continuous manner, whether that change be continuous (as in slowly-varying FM) or abrupt (as in frequency hopping).

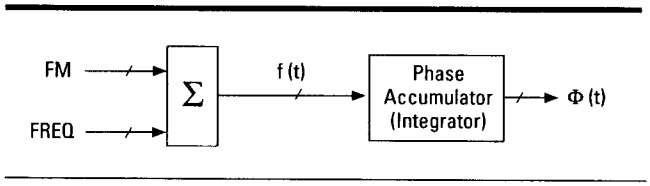


Figure 8-9. The phase accumulator in HP FASS produces a continuous phase function over time.

Conversely, with phase-coherent frequency switching the signal must appear as if each frequency is being generated by a separate, continuously-running oscillator being switched in and out as needed. Whenever the simulator returns to a specific frequency, the phase of the output signal must be as if the signal has always been at that frequency. The phase trajectory of such a signal is shown in figure 8-10.

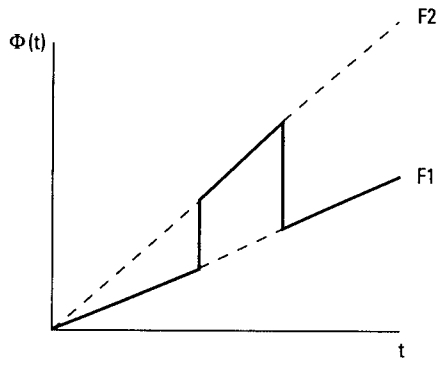


Figure 8-10. Phase-coherent frequency switching.

Phase-coherent frequency switching is automatically provided by the AUC of Models 10/11/21 and the AMUC of Model 21. In each case, the agile direct synthesizer effectively switches between continuously-running local oscillators.

In Models 7/11/21, it is also possible to perform phase-coherent frequency switching at baseband with the ACS. This function is performed with special phase-coherent correction circuitry which is present in these systems. (See figure 2-4.)

As the phase accumulator in HP FASS inherently produces a phase-continuous signal, it is necessary to "trick" it into a phase-coherent mode by introducing a precise phase jump at each frequency transition point. This jump in phase occurs over a single sample clock interval. Referring to figure 8-11

$\Phi(t) = 2\pi F_1 t$ Φ at time t

$\Phi(t+1) = 2\pi F_2 (t+1)$ Desired Φ at time t+1

$$\begin{aligned}\text{Phase Jump} &= \Phi(t+1) - \Phi(t) \\ &= 2\pi F_2 (t+1) - 2\pi F_1 t \\ &= 2\pi [F_2 t - F_1 t + F_2] \\ &= 2\pi [\Delta F\, t + F_2]\end{aligned}$$

Therefore,

Frequency at time (t+1) = $\Delta F\, t + F_2$

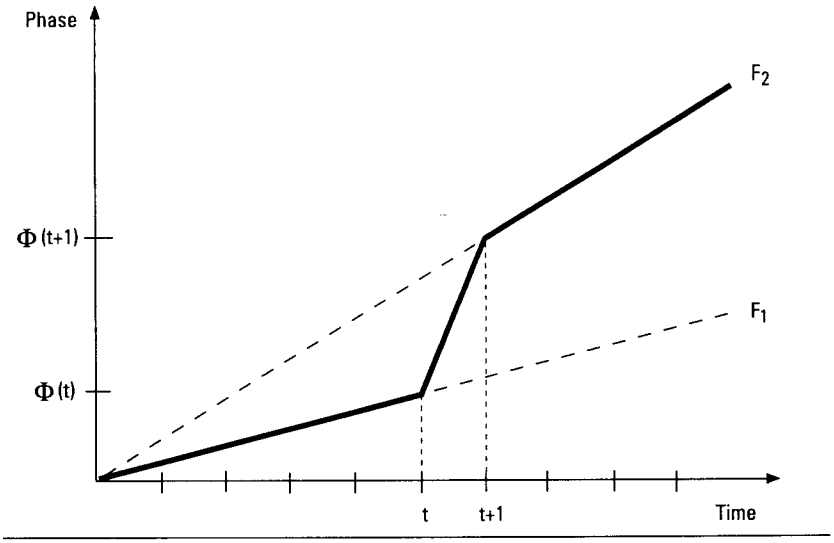


Figure 8-11. An instaneous phase bump is required to fool the phase accumulator into a phase-coherent mode.

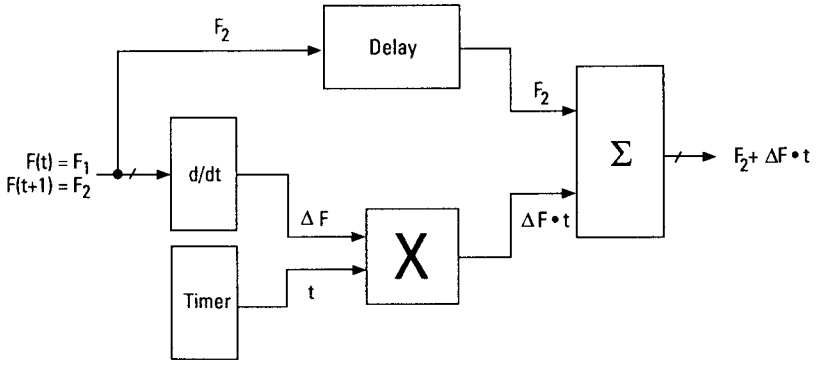


Figure 8-12. Phase-coherent correction circuitry in Models 7/11/21.

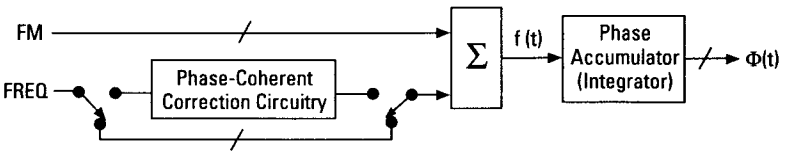


Figure 8-13. Phase-coherent correction can be switched in or out depending on the application. FM can also be added prior to correction.

A shapshot of the frequency correction circuitry in HP FASS at time t+1 is shown in figure 8-12. The differentiator detects a change in frequency; at all other time its output is zero. For one clock cycle, the output of this circuit will be ΔFt + F2. Figure 8-13 shows how the choice between frequency switching modes is made in Models 7/11/21. An alternative mode is also available whereby phase-coherent correction is done after the FM data has been added to the carrier data.

While this discussion has focussed on hopping between just two frequencies, the analysis holds true for multiple frequencies without limitation.

To summarize:

(1) Frequency hopping at baseband with the ACS is inherently a phase-continuous process by viture of the phase accumulation technique used to generate the carrier.

(2) In Models 7/11/21, the user can activate a phase-coherent correction mode to provide phase-coherent frequency switching at baseband with the ACS.

(3) Frequency hopping at IF and RF with the AUC (Models 10/11/21) and/or the AMUC (Model 21) is always phase-coherent.

Frequency Switching Speed

(Note: The following discussion pertains only to HP FASS Models 10/11/21. Refer to Appendix A for a discussion of frequency switching speed in the Model 7 Baseband FASS system.)

Figure 8-14 shows the phase plot for a 914 MHz to 373 MHz frequency hop. As shown, phase settles to within 5.7 degrees (0.1 radian) of its final value in 37 ns, while in just under 80 ns the phase has settled to within 0.57 degrees (0.01 radian). Although specified performance over the operating temperature range of HP FASS is a conservative 250 ns, typical performance across the full frequency band is consistently better than 100 ns for all frequency combinations.*

Note that the above discussion refers only to frequency switching using the Agile Upconverter and/or the Agile Microwave Upconverter. For applications in which the hop bandwidth is less than 40 MHz, upconversion is typically fixed and hopping is done at IF using the ACS. In this case, switching speed is limited by the update rate of frequency information to the phase accumulator. This rate is given by CLK/4, which is 33.55 MHz (29.8 ns) when using the internal system clock.

*See "Frequency Switching Time Measurement Using Digital Demodulation", Bruce G. Anderson, EEEE Transactions on Instrumentation and Measurement, Vol 39, No. 2, April 1990.

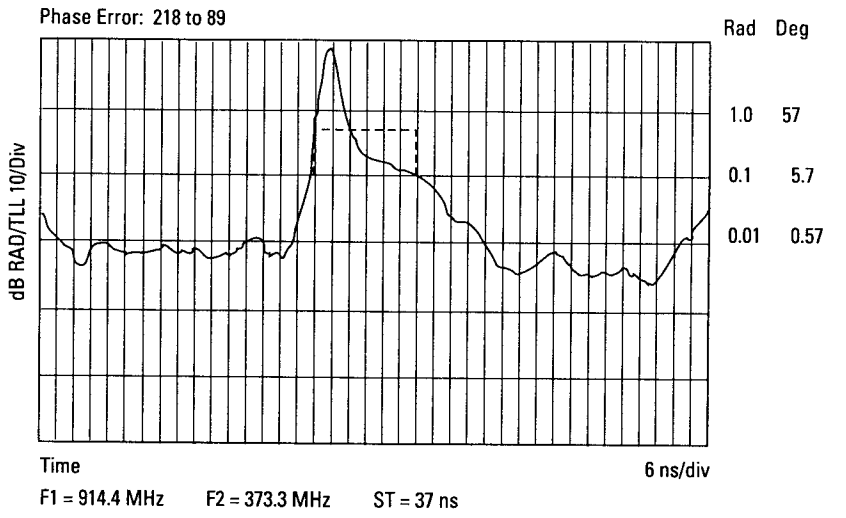


Figure 8-14. Signal phase vs. time for a 914 MHz to 373 MHz frequency hop.

System Data Security

This subsection discusses the various memory systems used in HP FASS and the procedures necessary to secure any data the user may deem classified.

Each of the instruments in HP FASS — the Smart Interface, the Modulation Data Source, the Agile Carrier Synthesizer, the Agile Upconverter, and the Agile Microwave Upconverter — uses some form of semiconductor memory. The memory in the MDS is used to store data describing the signal being generated. Some instrument configuration data is also stored in the MDS memory. The memories in the ACS, the AUC, and the AMUC store only instrument configuration data. In all four of these boxes, an exhaustive memory test is done as the instrument is powered on, overwriting any existing data and configuration information.

Although none of the instruments will retain data when powered off, one may ensure that no data is retained by cycling the power to run the memory tests. It is advisable to leave the power on for at least one minute to allow the RAM tests to fully complete.

The memories in the Smart Interface differ somewhat from those in the other instruments. There are basically four areas of RAM memory to be concerned with:

(1) Array processor RAM
(2) 68000 coprocessor RAM
(3) PC RAM
(4) Configuration RAM

The array processor RAM is completely cleared on power-up by a self-executing diagnostic test. The coprocessor RAM and PC RAM are standard DRAM technology used in most personal computers. Although it is not assertively cleared by any routine, no data is retained by the DRAM once power has been removed. The configuration RAM in the SI is saved via a battery back-up circuit. The information in the configuration RAM is not related to the signal being generated by the HP FASS; it only contains information for the operating system, such as the type of display and disk drive being used. Erasing this data will make HP FASS system bootup impossible.

In addition, the removable Bernoulli cartridge used with the Sl may also contain data which pertains to the signal being generated. If you are concerned about the security of data on the cartridge you should store it in a secure area. Data saved on floppy disks should be protected in a similar manner.

In summary, follow these procedures to ensure security of classified HP FASS data:

1. Reset the system via the front-panel RESET key in local mode or via the *RST command in remote mode.

2. Remove the Bernoulli cartridge and lock it in a secure area.

3. Cycle power on the Smart Interface.

4. Cycle power on the Modulation Data Source, Agile Carrier Synthesizer, Agile Upconverter, and Agile Microwave Upconverter. Wait at least one minute while the instruments run their internal self-tests.

5. Power all instruments off.

Triggering Overview

In many applications, it is necessary to synchronize signals from HP FASS to a trigger from an external source. In radar target simulation, for example, a PRF trigger from the radar system under test might be used to precisely control the timing of the simulated target returns. The HP FASS system must be capable of responding to these triggers in a known, repeatable fashion so that timing ambiguities are avoided.

There are three types of triggering available in the HP FASS system:

(1) Start/Stop System Triggering

(2) Packet Advance Triggering

(3) Dynamic Sequence Triggering (Models 7/11/21 only)

Each of these trigger types is discussed separately in the following sections.

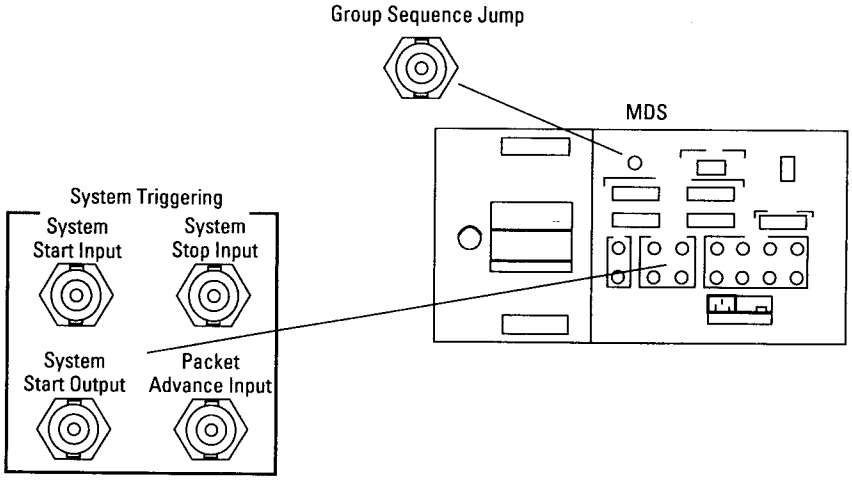


Figure 9-1. HP FASS System Triggering.

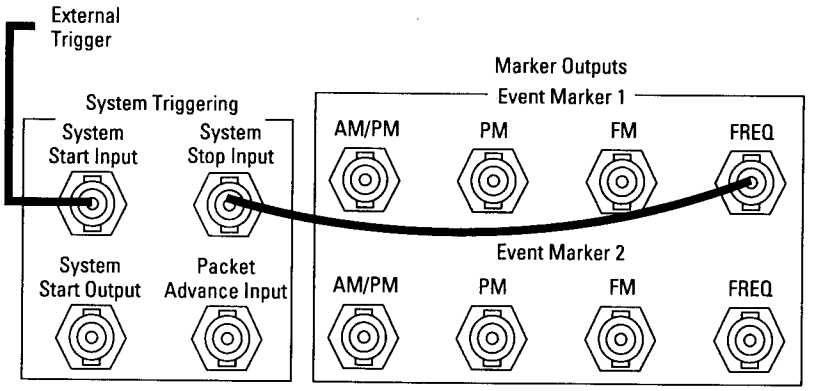


Figure 9-2. For single-shot triggering, one of the EVENT MARKER outputs can be jumpered to the SYSTEM STOP INPUT.

Start/Stop System Triggering

With start/stop triggering, signal generation from the HP FASS system is controlled with START and STOP trigger signals. These signals can be either HP-IB software triggers or TTL hardware triggers.

There are three modes of start/stop triggering available:

1. Free Run. Signal generation is initiated from the front panel or over HP-IB with a START command. The system runs continuously until a STOP command is issued, which stops and resets the sequencers in the Modulation Data Source.

2. External Continuous (ECON). Signal generation is initiated via an external TTL trigger into the SYSTEM START INPUT (figure 9-1), or with a "trigger start" command from the front panel or over HP-IB. Once started, the system runs continuously until a STOP command is issued.

3. External Single (ESIN). Signal generation is initiated via an external TTL trigger into the SYSTEM START INPUT and paused via an external TTL trigger into the SYSTEM STOP INPUT. Both of these triggers can be supplied by the user. However, by connecting a jumper cable from one of the EVENT MARKER outputs to the SYS-

TEM STOP INPUT (figure 9-2) it is possible to automatically pause the system after each repetition of the signal, thereby providing a single-shot capability. Execution is resumed with each new trigger into the SYSTEM START INPUT.

Packet Advance Triggering

Another type of triggering available with the HP FASS system is packet advance triggering. As explained in section 4, the sequencers in the Modulation Data Source serve as address generators for accessing signal data from the modulation RAMs. The addressing information is specified in the form of packets. For each packet, the user must specify where in RAM the wave segment is located, the number of scans through that wave segment before advancing to the next packet, and the method of advancing to the next packet.

In Model 10 there are three packet advance modes available:

1. Auto. The sequencer automatically advances to the next packet after completing the specified number of scans.

2. Bus. The sequencer advances to the next packet after receiving an HP-IB software trigger. The current scan finishes before the sequence advances.

3. Group. All sequencers set to this mode advance to the next packet after receiving a packet advance trigger. This trigger can be either a software HP-IB trigger or an external TTL trigger coming into the PACKET ADVANCE INPUT of HP FASS. (See figure 9-1.) The current scan finishes before the sequence advances.

In Models 7/11/21, there are two additional packet advance modes available:

1. Bus Immediate. The sequencer *immediately* advances to the next packet after receiving an HP-IB software trigger.

2. Group Immediate. All sequencers set to this mode *immediately* advance to the next packet after receiving a packet advance trigger. This trigger can be either a software HP-IB trigger or an external TTL trigger coming into the PACKET ADVANCE INPUT of HP FASS.

It is important to note the timing ambiguities that arise when supplying an external trigger into the PACKET ADVANCE INPUT for the GROUP packet advance mode. As mentioned, it is necessary for the current scan of a wave segment to be completed before a sequence can advance to the next packet. The time from when a trigger comes into the system to the time when the sequence is advanced is therefore variable; the trigger can arrive anytime during the current scan. Consequently, this method of triggering should only be used when timing accuracy is not critical.

Dynamic Sequence Triggering

The final type of triggering available in the HP FASS is referred to as dynamic sequence or sequence jump triggering. This feature is limited to the Model 7/11/21 systems.

Dynamic sequencing is a real-time capability which allows the user to randomly select a signal on-the-fly based on some external event. The user pre-programs a set of signal sequences, each with its own unique sequence identification number. In real-time, the user then selects a signal sequence by providing a sequence number to the HP FASS system, either over HP-IB or with digital data into a 25-pin I/O port on the back panel of the MDS. In addition, the user must also provide a trigger to initiate a jump to the new signal sequence. This trigger can be either a software HP-IB trigger, a TTL trigger into the GROUP SEQUENCE JUMP trigger input on the back panel of the MDS (figure 9-1), or a TTL trigger into one of the 25-pin I/O ports on the back panel of the MDS.

For more complete details on this dynamic sequencing capability, please refer to Product Note 8791-1, *Real-time Control of HP FASS.*

Synchronous vs. Asynchronous Triggering

Repetitive triggering of the HP FASS system can be done using either start/stop triggering, packet advance triggering, or dynamic sequence triggering. Depending on the user requirements for pulse-to-pulse jitter, this triggering can be done either synchronously or asynchronously. As an example, we will look at a typical implementation of start/stop triggering to explain the difference between these two modes of operation.

Repetitive triggering using start/stop trigger signals is done in the EXTERNAL SINGLE mode. Once a TTL trigger is received at the SYSTEM START INPUT, signal data from the Modulation Data Source is latched at the next rising edge of CLK/8.

The timing relationship between the CLK/8 signal and an asynchronous external trigger is shown in figure 9-3. As shown, the time Δ from when a trigger arrives to the time it is recognized by the system can vary with each trigger pulse. This variation translates into jitter of the RF output in relation to the incoming trigger signal. When using the internal 134-MHz system clock, this jitter can be as large as 59.6 ns.

Figure 9-4 shows an example of asynchronous triggering from a radar system. In this configuration, simulated target returns can have a timing ambiguity of up to 59.6 ns, corresponding to a range ambiguity of about 30 feet (9.14 meters).

In cases where pulse-to-pulse jitter must be minimized, synchronous triggering should be used. As shown in figure 9-5, this is achieved by driving the external trigger source and the HP FASS system with a common clock. (In this case, the radar provides the clock and 10 MHz reference for the two systems.) In addition, the divider used to generate the PRF trigger should be a multiple of eight so that the PRF trigger is consistently phased to CLK/8.

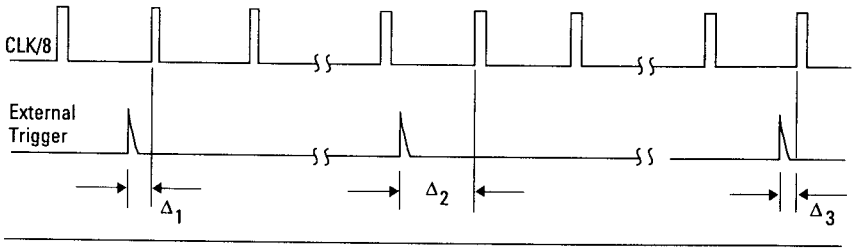


Figure 9-3. Timing jitter as a result of asynchronous triggering.

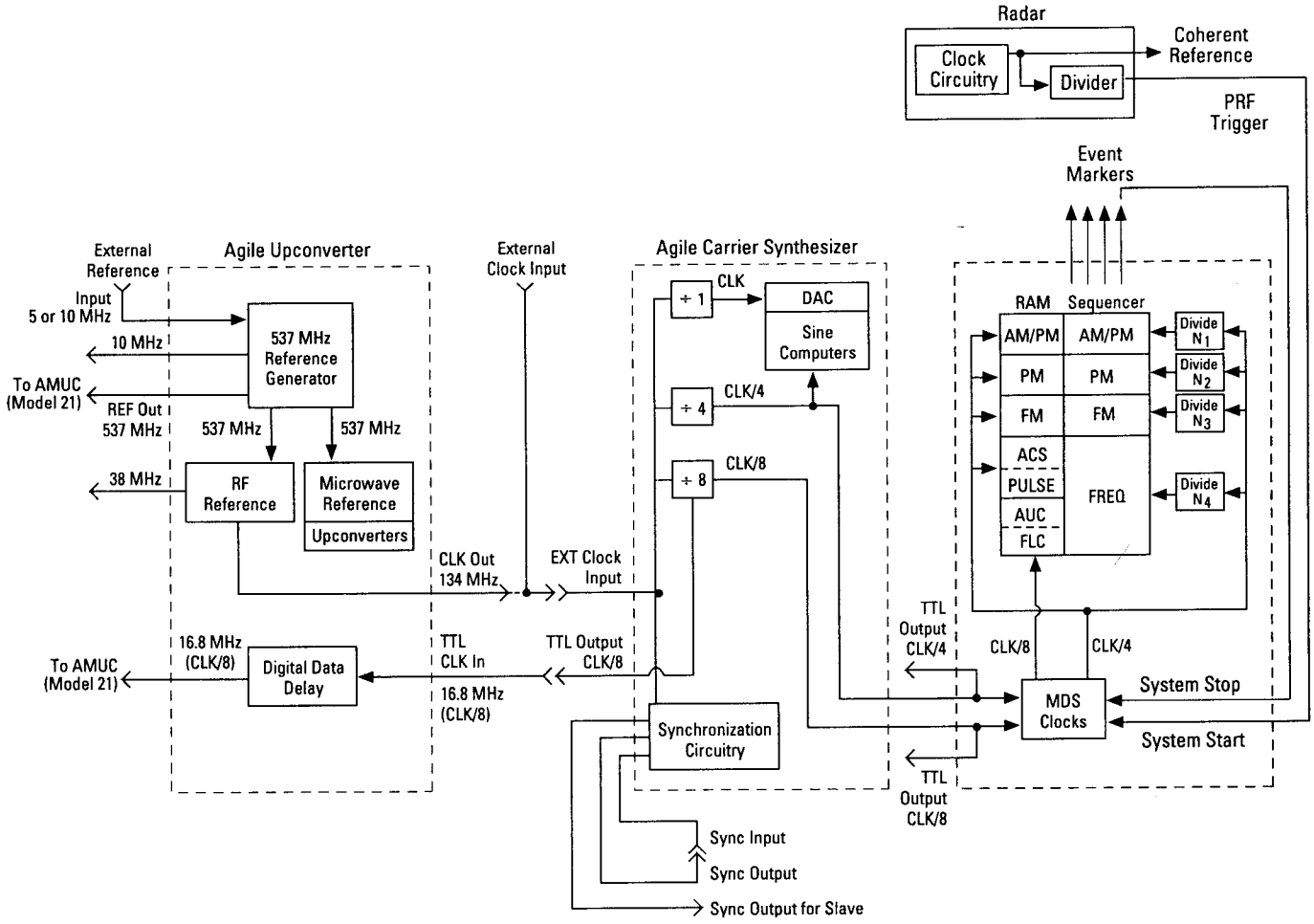


Figure 9-4. Asynchronous start/stop triggering of HP FASS from a radar.

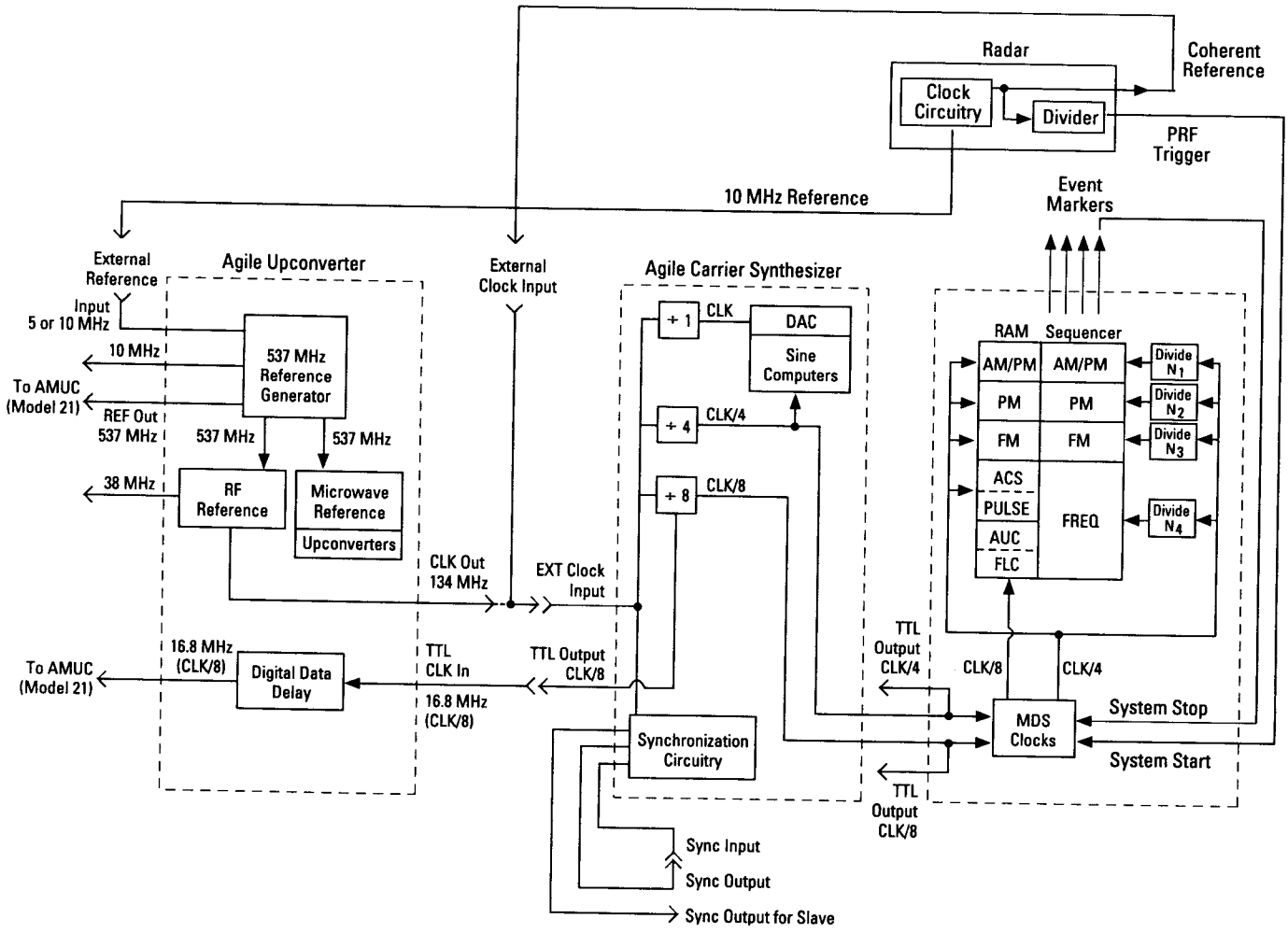


Figure 9-5. Synchronous start/ stop triggering of HP FASS from a radar.

Figure 9-6 shows the timing relationship for synchronous operation. The time difference Δ is now fixed.

It is important to note that an external trigger does not produce an immediate RF output from the system. Due to digital and analog signal delays through the system, there is an approximate 2.6 µs (Models 7/10) or 3.6 µs (Models 11/21) latency from the time a trigger is recognized to the time the associated signal arrives at the RF output. However, this delay is fixed for a given HP FASS system and does not contribute to timing ambiguities.

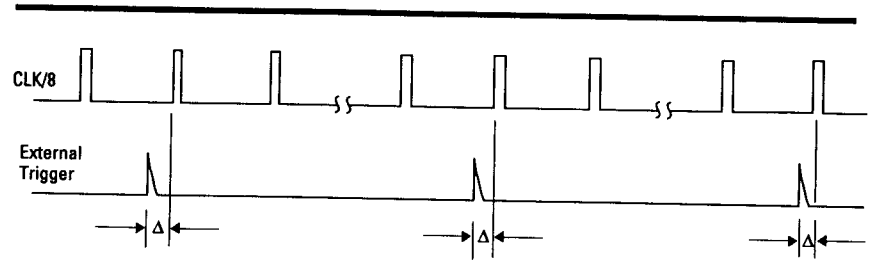


Figure 9-6. Timing stability as a result of synchronous triggering.

Synchronizing Multiple HP FASS Systems

Synchronization of multiple HP FASS systems is accomplished by locking each system to the same clock. The HP FASS system that provides this common clock is referred to as the MASTER. All other units in the setup are designated as SLAVES. Figure 9-7 shows the cabling required when synchronizing two HP FASS systems. (Note that the FREQUENCY STANDARD switch on the back panel of the SLAVE's Agile Upconverter must be set to EXT ±0.05 ppm.)

NOTE: There is only one SYNC OUTPUT FOR SLAVE provided by the MASTER unit. When synchronizing more than two HP FASS systems, an external ECL buffer is required for this output in order to provide proper fan-out to all SLAVE units. (See figure 9-8.) In addition, an external buffer may be required for the SYSTEM START OUTPUT of the Modulation Data Source in the MASTER. Refer to Section B, *Rear Panel Connectors*, of the *HP FASS System Operating Manual* for specifications of these two connectors.

Once the proper hardware configuration has been established, each system is individually loaded with the desired signal and sequence data. (Remember, each system must be set to a unique HP-IB address.) Once programmed, system synchronization can be initiated either internally or externally. For internal synchronization, a software trigger is sent to the MASTER unit and all systems immediately start in unison. (There may actually be a fixed start delay from unit to unit due to differences in clock cable lengths.) For external synchronization, the SYSTEM START INPUT of the MASTER unit is enabled to accept an external TTL trigger.

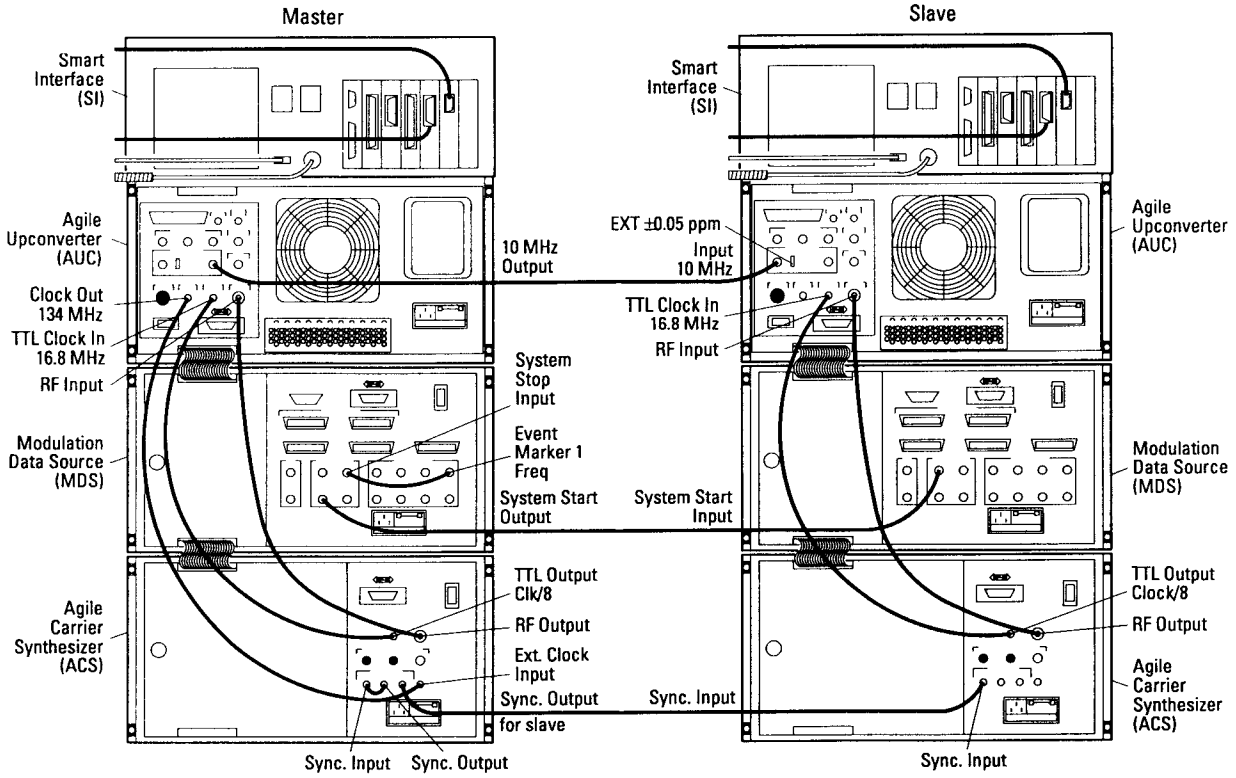


Figure 9-7. Cabling for synchronizing two HP FASS systems.

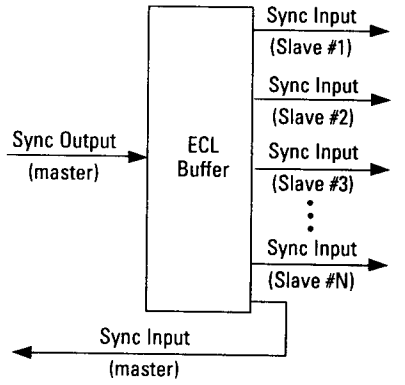


Figure 9-8. An external ECL buffer provides the proper fan-out of the MASTER clock signal to all SLAVE systems.

Note that the above procedure does not guarantee that the RF output signals from multiple HP FASS systems will be in-phase. The following factors all contribute to possible phase skew between systems:

1. Clock cable lengths. As mentioned above, the sequencers in each of the systems will not necessarily start at the same time if the clock cables to each system vary in length.

2. Analog delay. Once a signal exits the Agile Carrier Synthesizer, it must go through an analog upconversion chain. The delay through this chain will vary from system to system, with the SAW filter in the Agile Upconverter being the primary contributor to variations.

3. Independent Oscillators. Although synchronization is achieved through the use of a common clock, that clock only drives the digital circuitry of each HP FASS. The oscillators in the individual Agile Upconverters, while locked to the same 10-MHz reference, are still independent in that their phases are different due to the random power-up state of dividers in each AUC.

It is important to note that any phase skew between systems will remain constant as the systems are stopped and restarted. Therefore, the phase skew can be compensated for by either adjusting clock cable lengths or by programming a constant phase offset in the PM memory of one or more of the HP FASS systems.

Also note that when synchronizing HP FASS systems, losses in the SYNC OUTPUT FOR SLAVE clock cable can result in a degraded clock signal in the SLAVE units. This may subsequently degrade spur performance. Thus, it is best to use short, low-loss cables to optimize spur performance.

(The Model 7 Baseband FASS system does not include an Agile Upconverter. Therefore, analog delay differences between any two systems is minimal. In addition, all oscillators in a synchronized configuration are locked; there are no independent oscillators.)

At the digital level, the Model 7 Baseband FASS system has the same functionality as the Model 11/21 systems. It is at the analog level, however, that these systems differ; there are no upconverters in the Model 7 system. The Model 7 system therefore consists only of the Smart Interface (SI), the Modulation Data Source (MDS), and the Agile Carrier Synthesizer (ACS).

As shown in figure A-1, the ACS of the Model 7 is modified to provide an analog output section. This output section consists of a low-pass anti-aliasing filter, amplifier, and programmable step attenuator. In addition, all Model 7 system clocks are generated within the ACS. System clocks can be based either on the internal 134 MHz oscillator, or on an external clock signal. An internal or external 10 MHz timebase reference is used.

System Bandwidth and Agility

The output frequency range of the Model 7 system is DC to 50 MHz. Therefore, the instantaneous modulation bandwidth is 50 MHz. Since all frequency hopping is done at baseband, the switching speed is limited by the update rate of frequency information to the phase accumulator. This rate is given by CLK/4, which is 33.55 MHz (29.8 ns) when using the internal 134 MHz system clock.

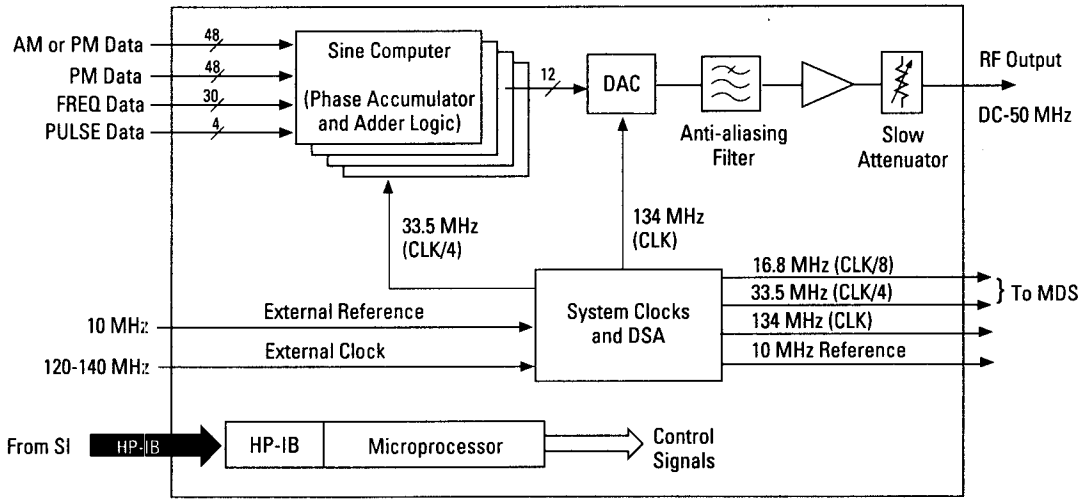


Figure A-1. Block diagram of the Agile Carrier Synthesizer in Model 7.

System Output Power

The output power from Model 7 is determined by three factors:

(1) The amplitude values loaded into the AM/PM memory of the Modulation Data Source.

(2) The gain of the output amplifier in the Agile Carrier Synthesizer.

(3) The setting of the output attenuator in the Agile Carrier Synthesizer (0-70 dB, 10 dB steps).

The AM value loaded into the MDS determines the output power from the DAC. With all ones loaded (full amplitude), the output is about -10 dBm. With 0.5 loaded (half voltage), the power decreases by 6 dB to -16 dBm.

The gain of the output amplifier is about 20 dB.

The slow-switching output attenuator can be set anywhere from 0 to 110 dB in 10 dB steps. This attenuator is controlled from the microprocessor.

In general, the following equation should then be used to calculate the overall system output power from Model 7:

*Output Level = 10 dBm + 20*LOG(AM Data) – Output Attenuator Setting*

For example, suppose the following parameters are being used in a Model 7 system:

AM Value = 0.4
Output Attenuator = 10 dB

The output power is then calculated as

Output Level =
*10 + 20*LOG(0.4) – 10 =*
–7.96 dBm

The output power from Model 7 is specified to be –100 dBm to +10 dBm.

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