Agilent Communications Agile Operation of the 8645A

Product Note 8645-1

Agilent Technologies

Product Note 8645-1

Introduction

This product note explains the frequency agile capabilities of the 8645A Agile Signal Generator, and the control of these capabilities. As the Table of Contents indicates, the focus of this document is on operation rather than on performance.

After reading this product note, the user should know how to operate all of the agile capabilities of the 8645A, and be able to use the signal inputs and outputs related to agile operation to integrate the Agile Signal Generator into a test system.

Table of Contents

Overview

The 8645A is a 1 (or 2) GHz RF signal generator specifically designed to perform the most demanding tests on frequency agile radios and on state of the art communication systems; with its modulation, amplitude control, and sweep functions, the 8645A also performs in and out-of-channel tests on high-performance radios.

Specifically, your frequency agile and communication testing needs are met in the following ways:

1. A frequency range of 251.5 kHz to 2060 MHz (1030-2060 MHz is obtained by ordering Option 002).

2. Modulation formats include AM, FM, and Pulse.

3. Frequency hopping is controlled from the front panel, or by the rear panel GPIB, Sequence, Hop, and Fast Bus connectors.

4. Digitally stepped or phase continuous frequency sweeping.

5. Remote ATE programming through GPIB (Agilents implementation of IEEE Standard 488.2 - 1987).

As shown in Figure 1, frequency hopping is controlled in three ways. Locally from the front panel, remotely from GPIB, and externally from the rear panel. This product note describes how to control frequency hopping locally and remotely; refer to the 8645A Operation Guide part number 08645-90023 if you need information about GPIB control.

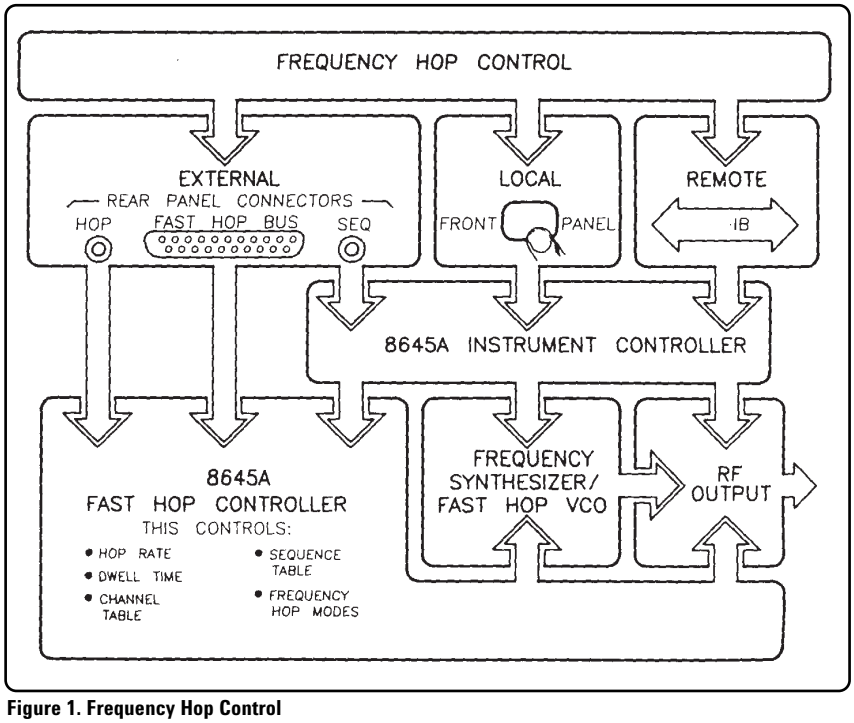


Figure 1. Frequency Hop Control

Whatever your method of controlling the 8645A, there are six basic steps to follow when you frequency hop the 8645A:

1. Put the 8645A into the Fast Hop, Mode 5.

2. Enter frequency and amplitude settings into a channel table, and then arrange the sequence table in a specific order.

3. Enter values for the hop rate and dwell time.

4. Select any one of the nine frequency hop modes.

5. Set up modulation on the RF output.

6. Activate the 8645A to frequency hop.

Channels and Sequences

The 8645A frequency hops between sets of frequency and amplitude parameters. Each set is stored in a unique memory location called a "channel". As you store each set into different channels you create what is called a "channel table".

Entries in the channel table do not contain information about the order in which each channel is output from the Agile Signal Generator. The order is specified in what is called a "sequence table". You determine the organization of the sequence table.

The Channel Table

The channel table consists of 8000 internal memory locations stored in non-volatile memory. Each channel in the table is used to specify a frequency and amplitude to which the 8645A will hop. Channel storage registers start at numeral 0 and go to numeral 7999. An example channel table is as follows:

Channel Number	Channel Frequency	Channel Amplitude
0	100 MHz	10 dBm
1	550 MHz	8 dBm
2	1020 MHz	12 dBm
7999	250 MHz	6 dBm

Table 1. Example Channel Table.

Local Entry Keys for the Channel Table

Three front-panel keys are used to set up a channel table. The keys are accessed by first pressing the blue **SHIFT** key. A description of each key follows the illustration shown below:

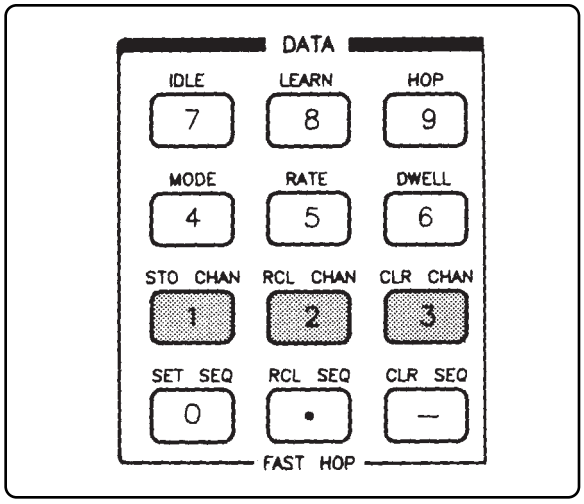


Figure 2. Local Entry Keys for the Channel Table

The **STO CHAN** key is used to store frequency and amplitude settings in a channel, and to overwrite any current channel settings. You must sequentially store each channel starting with storage register 0. If you do not, an error message appears to indicate a Bad fast chan address. The maximum allowed variation for amplitude settings is 20 dB unless you turn on Special Function 203. The error message Amptd range too large appears if you exceed the attenuator's vernier range.

The **RCL CHAN** key is used to recall frequency and amplitude settings for any existing channel from the channel table. You must recall an existing channel number, or else an error message appears to indicate a Bad fast chan address.

The **CLR CHAN** key is used to clear all entries from the channel table. When you re-enter data into the channels after clearing all entries, start again with storage register 0.

Remember

All front-panel keys associated with frequency hopping cannot be accessed unless the **MODE 5, FAST HOP** key is active. If this mode is not active, an error message appears to indicate that the - instrument is Not in Fast Hop Mode. A yellow annunciator above the **MODE 5** key lights up to let you know that it is active.

The Sequence Table

The 8645A has a time saving feature which uses a hop sequence identical to the order in which frequency and amplitude settings were entered into the channel table. That is, if you do not set up the sequence table, the 8645A frequency hops in ascending numerical order starting from channel number 0 and on up to the last channel in which you have stored a set of frequency and amplitude parameters.

However, you may set up the sequence table in a specific order for the frequency hop. The sequence table consists of up to 8000 channel table entries stored in non-volatile memory. The sequence table starts at numeral 0 and can go to numeral 7999. A Channel may be repetitively used in the sequence table. An example of a sequence table is as follows:

Sequence Step #	Channel
0	3
1	0
2	100
3	0
7999	1

Table 2. Example Sequence Table.

Local Entry Keys for the Sequence Table

Three front-panel keys are used to set up a sequence table. The keys are accessed by first pressing the blue SHIFT key. A description of each key follows the illustration shown below:

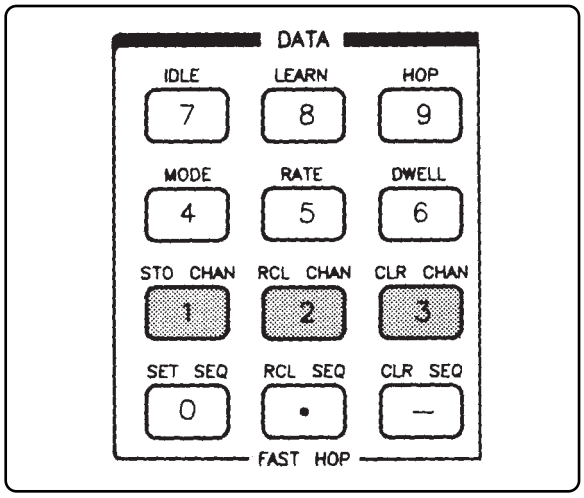


Figure 3. Local Entry Keys for the Sequence Table.

The **SET SEQ** key is used to set up channels in the sequence table. The 8645A automatically increments to the next available sequence location as you enter each channel. The sequence table starts at numeral 0. Channels are entered in any order, and can be entered more than once in the sequence table.

The sequence table cannot be corrected one entry at a time. If modifications to the sequence table are required, the sequence table must first be cleared, and new sequences entered.

The **RCL SEQ** key is used to recall frequency and amplitude settings for any existing channel from the sequence table. You must recall an existing sequence number, or else an error message appears to indicate a Bad fast sequence entry.

The **CLR SEQ** key is used to clear all channels from the sequence table. When you re-enter data into the sequence table after clearing all channels, you will start over with sequence number 0.

Remember

If your sequence table has channel number entries that do not exist in the channel table, and you attempt to frequency hop the instrument, an error message appears to indicate a Bad fast sequence entry. Fix either the channel table or the sequence table.

Rate and Dwell

The 8645A allows you to set the number of hops per second (called the "hop rate"), and the duration of the RF output for each hop (called the "dwell time"). Hop rate and dwell time values are interactive. If the hop rate and dwell time values clash when the 8645A is asked to frequency hop, an error message appears to indicate a Rate and dwell conflict.

The hop rate and dwell time may be set prior to activating the frequency hop, or varied during the frequency hop (as described on page 10) without having to relearn the frequency/amplitude channel settings. Using an external triggering source also allows you to vary the hop rate and/or dwell time while frequency hopping.

Note

For information about using an external triggering source to vary the hop rate and/or dwell time, refer in this product note to the section titled "External Triggering". Specifically, Ext Stepped Ext Dwell and Fast Hop Bus Ext Dwell.

Hop Rate

Hop rate is the number of frequency changes per second expressed in Hertz. The internal hop rate is specified as a fixed frequency over the frequency range of 8 Hz to 50 kHz. However, the maximum allowable hop rate is limited by the frequency range over which the 8645A frequency hops.

For example, the table on the next page indicates that if you were to frequency hop two channels, one at 150 MHz and the other at 100 MHz, the maximum hop rate you can use is 10.9 kHz.

Dwell Time

Dwell time is the duration of the RF output power for any channel at the RF Output connector. The duration covers a time period between two points where RF output power is turned 90% on, and is turned 10% off, as shown below:

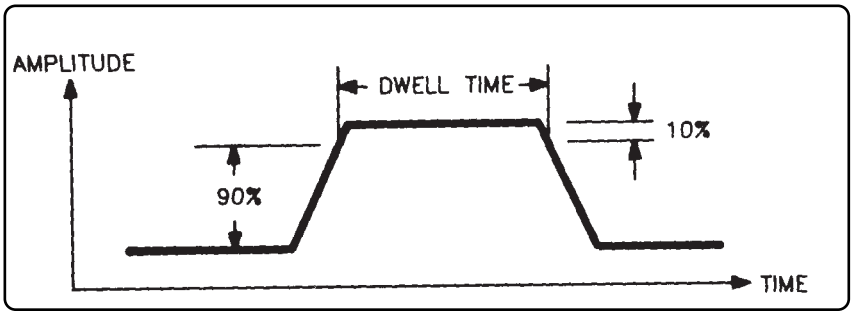


Figure 4. Dwell Time Duration.

The internal dwell time is specified as a fixed duration over the range of 6.4 msec to 99 msec (an external trigger input allows longer and variable dwell times). A fundamental characteristic of dwell time is that it cannot be longer than the period of the hop rate, which is:

$$\text{Hop Period} = \frac{1}{\text{Hop Rate}}$$

In fact, the dwell time must be less than or equal to the Hop Period minus the Switching Time, as follows:

$$\text{Dwell Time} \leq \text{Hop Period} - \text{Switching Time (see Table 3)}$$

Switching time is a function of the frequency range over which the Agile Signal Generator frequency hops. As the hop rate decreases, the switching time proportionally increases.

Switching times for each frequency range, along with the maximum hop rates for each frequency range are shown below:

Frequency Range (MHz)	Closed Loop ALC Switching Time* (msec)	Maximum Hop Rate (kHz)
128-2060	<15	50**-
8-2060	<85	10.9
0.252-2060	<500	1.98

* Add 5 µsec: for Option 002.

** With hop rates above 46.7 kHz, dwell time must be less than 6.4 msec to allow for frequency switching.

Table 3. Switching Times and Maximum Hop Rates.

For example, let's see if it is possible to use a 100 msec dwell time to frequency hop channels over an 8 MHz to 1 GHz frequency range at a 5 kHz hop rate. Note the following calculations:

Dwell Time = 100 µsec
Hop Period = 200 µsec
Switching Time = 85 µsec (worst case)

115 µsec = 200 µsec - 85 µsec

100 msec ≤ 115 µsec

Calculations show that the 100 msec dwell time will work, Switching time, shown in the above calculation, is a "worst case" value derived from the table shown on the previous page.

Local Entry Keys for the Hop Rate and Dwell Time

Two front-panel keys are used to set hop rate and dwell time. The keys are accessed by first pressing the blue **SHIFT** key. A description of each key follows the illustration shown below:

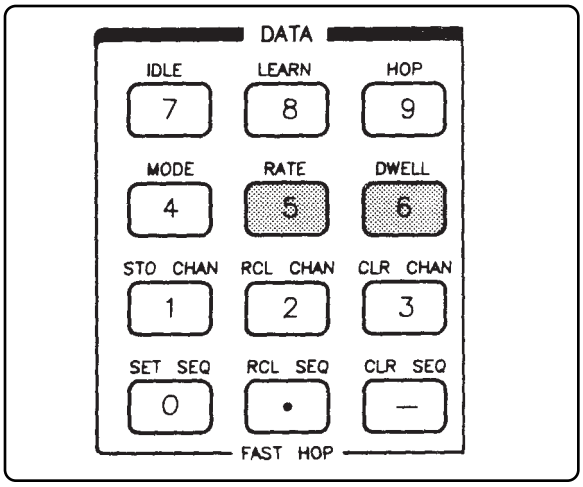


Figure 5. Local Entry Keys for the Hop Rate and Dwell Time.

The **RATE** key is used to set the hop rate. Whenever an instrument preset is done, the hop rate defaults to 250 Hz.

The **DWELL** key is used to set the dwell time. Whenever an instrument preset is done, the dwell time defaults to 2.00 msec.

Remember

If you get a Rate and dwell conflict error message, modify the values for either hop rate or dwell time so that Dwell Time ≤ Hop Period - Switching Time

Hop Rate and Dwell Time Resolution

Dwell time for the RF output can be entered from a minimum of 5 µsec, and up to a maximum of 125 msec; however, 6.4 µsec is the lower limit, and 99 msec is the upper limit specified for internal triggering. Hop rate can be entered from a minimum of 8 Hz, and up to a maximum of 200 kHz; however, 50 kHz is the upper limit specified for internal triggering.

Dwell time resolution is determined as follows:

- Dwell time resolution is limited by 3 significant digits shown on the front-panel display, and can be entered in 200 nsec intervals if the hop rate is greater than or equal to 77 Hz. (For frequency hop modes 1, 2, 4, and 5, refer to Table 4.)

- Dwell time resolution is limited by 3 significant digits shown on the front-panel display, and can be entered in 2 µsec intervals if the hop rate is less than 77 Hz. (For frequency hop modes 1, 2, 4, and 5, refer to Table 4.)

- Dwell time resolution is 200 nsec if the dwell time is less than 13 msec, or 2 µsec if dwell time is greater than or equal to 13 msec. (For frequency hop modes 3, and 6-9, refer to Table 4.)

Hop rate resolution is determined as follows:

- When the hop rate is less than 77 Hz, resolution is limited by 3 sig nificant digits shown on the front-panel display, or by 200 nsec increments in the hop rate period.

- When hop rate is greater than or equal to 77 Hz, resolution is lim ited by 3 significant digits shown on the front-panel display, or by 2 µsec increments in the hop rate period.

Hop rate or dwell time values may be changed while the 8645A is learning or frequency hopping. Select either hop rate or dwell time, and do the following:

- Key in the new hop rate or dwell time value. If the hop rate or dwell time conflict, you will get an error message while learning or hopping (the last valid values will still be active).

- Turn the knob. You may use the INCR/DECR ⇐∇or ⇒∇ keys to change the resolution of the knob. Turning the knob in either direction will set hop rate or dwell time without causing an error during the learning or hopping.

- Press one of the INCR/DECR ⇑ ⇓ keys to change the hop rate in 10 Hz increments, and the dwell time in 100 msec increments. These keys can set hop rate or dwell time without causing an error during the learning or hopping.

Increments for the ⇑ ⇓ keys may be changed in the following way:

1. Press the blue **SHIFT** key, and either the **RATE** or **DWELL** key.
2. Press the **INCR SET** key. The FREQUENCY/STATUS display should show either Rate Incr or Dwell Incr and the currently active incre ment value.
3. Enter the new increment value.

Frequency Hop Modes

The 8645A has nine frequency hop modes (not to be confused with the front-panel **MODE SELECT** keys). Each frequency hop mode determines how the RF output is controlled during the frequency hop. Your testing or operating needs determine which frequency hop mode to use.

Only one frequency hop mode can be active at a time, and as you will see, each frequency hop mode has either an internal or an external triggering mechanism.

Internal triggering allows you to start or control the frequency hop from either the front-panel, or via GPIB. External triggering allows you to start or control the frequency hop with TTL signals either to the rear-panel **HOP** connector, or to the rear-panel **FAST HOP BUS** connector.

For detailed information about internal and external triggering, refer in this product note to the section titled *"External Triggering"*.

How to Access the Frequency Hop Modes

You can view each of the nine frequency hop modes in the FREQUENCY/STATUS display by doing the following:

1. **Press the Mode Select MODE 5, FAST HOP key**. Otherwise, you will get an error message that indicates Not in Fast Hop Mode.

2. **Press the blue SHIFT key, and the MODE key**. You'll notice the currently active frequency hop mode is shown.

3. **Turn the knob, or press one of the ⇑ ⇓ keys**. One at a time the other frequencyhop modes are shown. A frequency hop mode becomes active when it is shown in the FREQUENCY/STATUS display.

4. **To exit, press any front-panel key**. Remember, whichever mode is displayed when you exit is the active mode for subsequent operation.

A Brief Description of Frequency Hop Modes

A brief description of each frequency hop mode is as follows:

Internal Triggering		
Mode	**Frequency Hop Mode**	**Description**
1	Int Repetitive	Continuously cycles through the sequence table.
2	Int Single	Cycles once completely through the sequence table.
3	Int Stepped	Cycles one channel at a time through the sequence table.

External Triggering		
Mode	**Frequency Hop Mode**	**Description**
4	**Ext Repetitive**	**Same as 1, except that frequency hopping is initiated by a TTL signal.**
5	**Ext Single**	**Same as 2, except that frequency hopping is initialized by a TTL signal.**
6	**Ext Stepped Int Dwell**	**Same as 3, except that frequency hopping is controlled by a TTL signal.**
7	**Ext Stepped Ext Dwell**	**Same as 3, except that frequency hopping and dwell time are controlled by a TTL signal.**
8	**Fast Hop Bus Int Dwell**	**Frequency hop in any order to any channel in the sequence table. Dwell time is fixed.**
9	**Fast Hop Bus Ext Dwell**	**Same as 8, except that dwell time is controlled by a TTL signal.**

Table 4. Frequency Hop Modes.

When the 8645A is frequency hopping, a message in the FREQUENCY/STATUS display alerts the user to the status of the frequency hop mode. As shown in Table 5, the message is dependant upon which frequency hop mode is active:

Mode(s)	FREQUENCY/STATUS Message
1	Fast Hop (Free Running)
2,3	Fast Hop (Man/GPIB Trig)
4-9	Fast Hop (External Trig)

Table 5. Status Messages for the Frequency Hop Modes

For Frequency Hop Mode 1

When Fast Hop (Free Running) is displayed, the 8645A continuously cycles through each channel in the sequence table.

For Frequency Hop Modes 2 and 3

When Fast Hop (Man/GPIB Trig) is displayed, the 8645A waits for the user to trigger the frequency hop either manually (from the front panel) or remotely (through GPIB).

For Frequency Hop Modes 4 through 9

When Fast Hop (External Trig) is displayed, the 8645 waits for the user to externally trigger the frequency hop with a TTL signal on either the rear-panel **HOP** connector, or on the Fast Hop Bus HOP line.

Local Entry Key for the Frequency Hop Modes

The **MODE** key is used to change the frequency hop mode. This key is accessed by first pressing the blue **SHIFT** key. A description of the MODE key follows the illustration shown below:

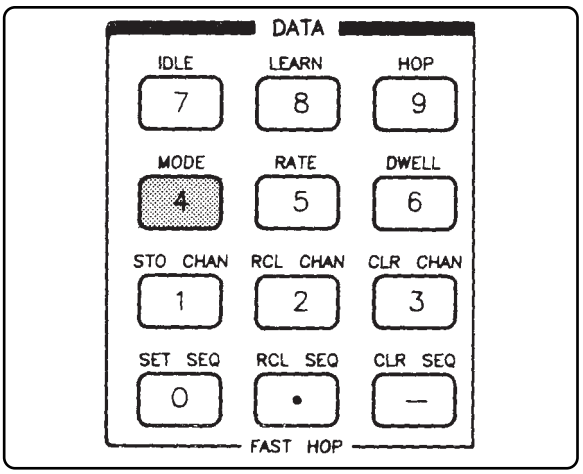


Figure 6. Local Entry Key for the Frequency Hop Modes.

The **MODE** key gives you access to the frequency hop modes. Whenever an instrument preset is done, the frequency hop mode defaults to Int Repetitive.

Remember

A Not in Fast Hop Mode error message indicates that you do not have the instrument in the FAST HOP mode; correct this problem by pressing the MODE SELECT, MODE 5 key.

Timing Control and Synchronization

This section contains essential information about timing control and synchronization for the frequency hop.

Timing control refers to implementation of the nine frequency hop modes discussed in the previous four pages. There are two types of triggering mechanisms for timing control, internal and external. Both Internal Triggering and External Triggering are described in detail later on in this section.

Synchronization refers to the arrangement in time of events that must take place for the frequency hop to occur. A timing diagram for each frequency hop mode explains the synchronization for both Internal Triggering and External Triggering.

To fully understand the timing diagrams shown with the Internal Triggering and External Triggering descriptions, you should read about the Fast Hop Bus.

Before investigating the details of timing control and synchronization, understand that you can put the 8645A into one of three conditions after pressing the Mode Select **MODE 5**, **FAST HOP** key:

1. The Idle State
2. The Learn State
3. The Hop State

Continue reading for a description of these three conditions.

The Idle State

When the 8645A is in the Idle State, it accepts entries or modifications to the channel table, sequence table, hop rate, dwell time, and frequency hop modes.

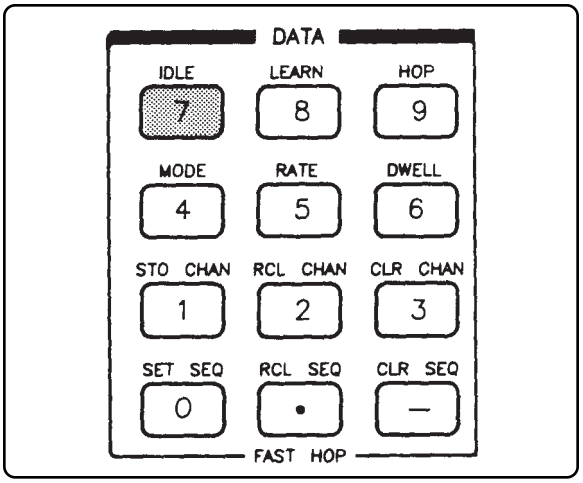


Figure 7. Local Entry Key for the Idle State.

The **IDLE** key, shown above, is accessed by first pressing the blue **SHIFT** key. There are two ways the Idle State can occur:

1. Whenever you change to the **MODE 5**, **FAST HOP** position from **AUTO** or any of the other Mode Select positions.
2. Whenever you press the **IDLE** key.

The 8645A goes from the Idle State to the Learn State upon request.

The Learn State

In the Learn State, the 8645A calibrates its internal circuitry to quickly switch from one channel to another with specified accuracy. It takes at least 10 seconds to complete the learn operation; additional time depends upon the number of channels set up in the sequence table.

Since the frequency accuracy of the RF output is temperature dependant, the Learn State should be kept active when not frequency hopping, or re-initiated if the ambient temperature has changed significantly since the last completed learn operation. This ensures the most accurate RF output while frequency hopping.

Note

If the ALC loop is closed (refer to the section in this product note titled "Amplitude Control"), the RF output is shut off during the Learn State. This prevents the output of undesired signals prior to frequency hopping. However, if the ALC loop is open, the RF output will be on during the Learn State.

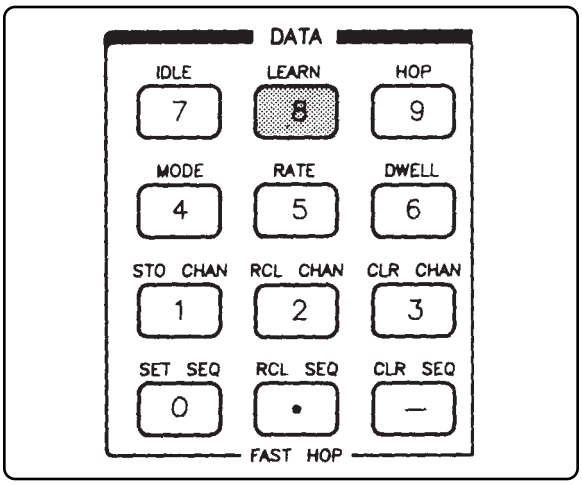


Figure 8. Local Entry Key for the Learn State.

The **LEARN** key, shown above, is accessed by first pressing the blue **SHIFT** key. There are three ways the Learn State can occur:

1. Whenever you press the LEARN key.
2. Whenever you press the HOP key to start the frequency hop. A Learn State occurs prior to the frequency hop even if the sequence table or channel table have not been changed.
3. The TTL level at the rear-panel SEQ (sequence) connector determines if the 8645A is in the Learn State. A TTL high keeps the 8645A in the Hop State; a TTL low puts the 8645A into the Learn State.

The 8645A can go from the Learn State to either the Idle State, or the Hop State.

The Hop State

Frequency hopping occurs in the Hop State.

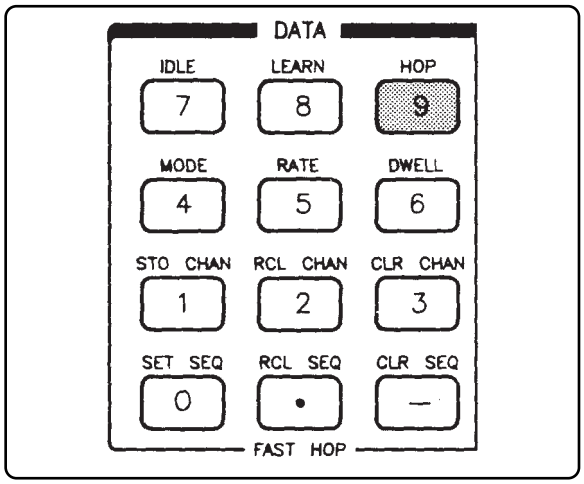


Figure 9. Local Entry Key for the Hop State.

The **HOP** key, shown above, is accessed by first pressing the blue **SHIFT** key. Going from the Learn State to the Hop State happens in one of two ways:

1. If the 8645A is internally triggered, the transition to the Hop State occurs immediately after pressing the **HOP** key (assuming that the learn operation first occurs).
2. If the 8645A is externally triggered, specific timing control and synchronization conditions must be met.

The Fast Hop Bus

The Fast Hop Bus is a DB-25 pin connector located on the rear-panel of the 8645A. Its purpose is to provide a means of external control and synchronization for the frequency hop sequence. Specific control and synchronization information on the Fast Hop Bus is found in the timing diagrams for Internal Triggering and External Triggering.

- When the 8645A is configured to operate with one of the three **internal** frequency hop modes, the Fast Hop Bus is used to trigger external control circuitry.

- When the 8645A is configured to operate with one of the six **external** frequency hop modes, the Fast Hop Bus is used to control the frequency hop.

The Fast Hop Bus connector is illustrated in Figure 10; a description of each line on the Fast Hop Bus starts on the next page:

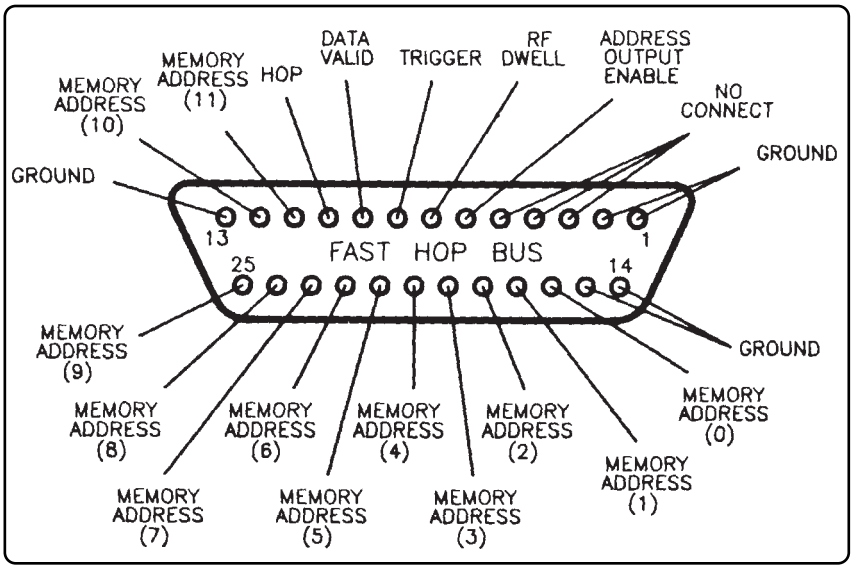


Figure 10. Rear-Panel, Fast Hop Bus Connector.

Ground and No Connection

The *Ground* connections for the Fast Hop Bus are found on J1 pins 1, 2, 13, 14, and 15.

There are no connections on the Fast Hop Bus for J1 pins 3, 4, and 5.

Address Output Enable

The *Address Output Enable* line on J1 pin 6 determines whether the *Memory Address* lines are to be used as inputs or outputs.

If the *Address Output Enable* line is at a TTL high or is floated, then the *Memory Address* lines are available as inputs. A binary address can then be synchronized on the *Memory Address* lines to indicate the desired position in the sequence table.

If the *Address Output Enable* line is grounded, then the *Memory Address* lines output the current sequence position during the frequency hop.

RF Dwell

The *RF Dwell* line on J1 pin 7 outputs a TTL signal to indicate the on/off state of the RIF output. A TTL high on the *RF Dwell* line indicates that the RF output is on; a TTL low on the *RF Dwell* line indicates that the RIF output is off.

The *RF Dwell* line is filtered to reduce RF emissions. As a result of the filtering, there is up to a 1 µsec delay from the time the RF output starts changing states from a low to a high, to when this transition appears at the rear-panel Fast Hop Bus connector.

Trigger

The *Trigger* line on J1 pin 8 outputs a TTL signal that goes from low to high to indicate when the 8645A has hopped to the next frequency in the sequence table. The transition back to a TTL low occurs when the RF output is turned off. No synchronization information is included with the *Trigger* line to indicate when the RF output is turned on.

The low to high transition of the Trigger line tracks the low to high transition of the **HOP** line (J1 pin 10) but is delayed by up to 200 nsec.

The *Trigger* line is not filtered, so there are only a few nanoseconds of delay for transitions to appear at the rear-panel Fast Hop Bus connector.

Data Valid

The *Data Valid* line on J1 pin 9 allows you to input a TTL signal to indicate that the *Memory Address* lines have set up a valid address on the Fast Hop Bus. A TTL high indicates that the valid address is present; a TTL low indicates that a valid address is not present.

In the *External Triggering* timing diagrams for Fast Hop Bus Internal Dwell and for Fast Hop Bus External Dwell, you will see how to synchronize the *Data Valid* line with the other Fast Hop Bus lines. The *Data Valid* line is used for synchronization with only these two frequency hop modes.

Hop

The *Hop* line on J1 pin 10 receives a TTL input signal to control the hop rate. Certain frequency hop modes also allow the *Hop* line to even control the dwell time. To control the Hop line, refer to the detailed descriptions for each frequency hop mode controlled by *External Triggering*.

The *Hop* line on the Fast Hop Bus, and the rear-panel **HOP** connector are internally connected, and consequently have the same synchronization.

Memory Address

The *Memory Address* lines on J1 pins 11, 12, and 16 through 25 receives TTL input signals to set up a desired address in the sequence table. The *Address Output Enable* line must first be enabled before an address can be input. The *Data Valid* line indicates if the input address is valid.

Internal Triggering

There are three internal triggering modes. Timing control and synchronization for each one is described in detail as follows:

Int Repetitive

The *Internal Repetitive* mode causes the 8645A to repetitively frequency hop through the sequence table when the Hop State is activated from the front panel or through GPIB.

Frequency hopping continues until the Learn State or Idle State is invoked. Hop rate and dwell time are fixed at the internally set values when this mode is active.

The following diagram in Figure 11 depicts the synchronization that occurs when the 8645A frequency hops in the Internal Repetitive mode:

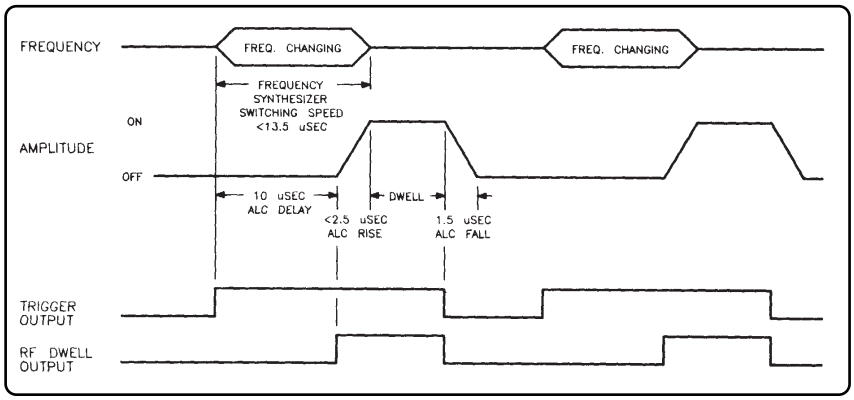


Figure 11. Internal Repetitive Synchronization.

Int Single

The *Internal Single* mode allows the 8645A to frequency hop once through the sequence table when the Hop State is activated from the front panel or through GPIB. At the completion of the Internal Single sequence, the 8645A remains in the Hop State with the RF output turned off and waits for another Hop command.

Hop rate and dwell time are fixed at the internally set values when this mode is active, To cycle through the sequence table again, re-activate the Hop State.

The following diagram in Figure 12 depicts the synchronization that occurs when the 8645A frequency hops in the Internal Single mode:

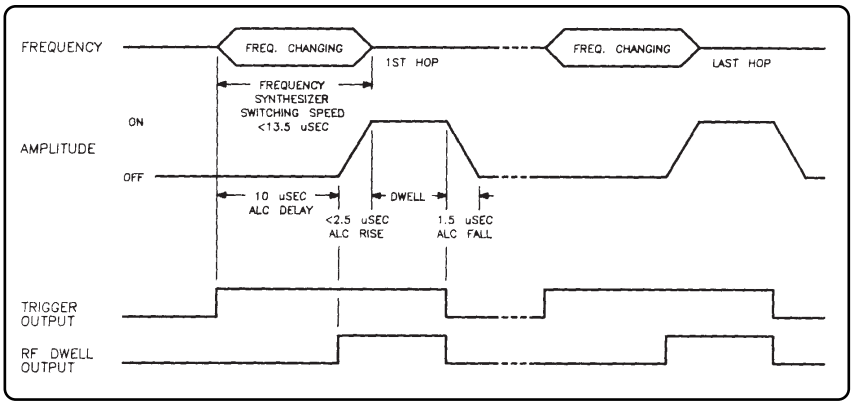


Figure 12. Internal Single Synchronization.

Int Stepped

The *Internal Stepped* mode allows the 8645A to cycle through the sequence table one channel at a time. In this mode, the user controls the hop rate either from the front panel, or from the rear-panel GPIB connector. Dwell time is fixed at the internally set value.

When this mode is active, a frequency hop occurs only when the ⇑ key is pressed, the knob is rotated, or the frequency hop is invoked through GPIB.

The following diagram in Figure 13 depicts the synchronization that occurs when the 8645A frequency hops in the Internal Stepped mode:

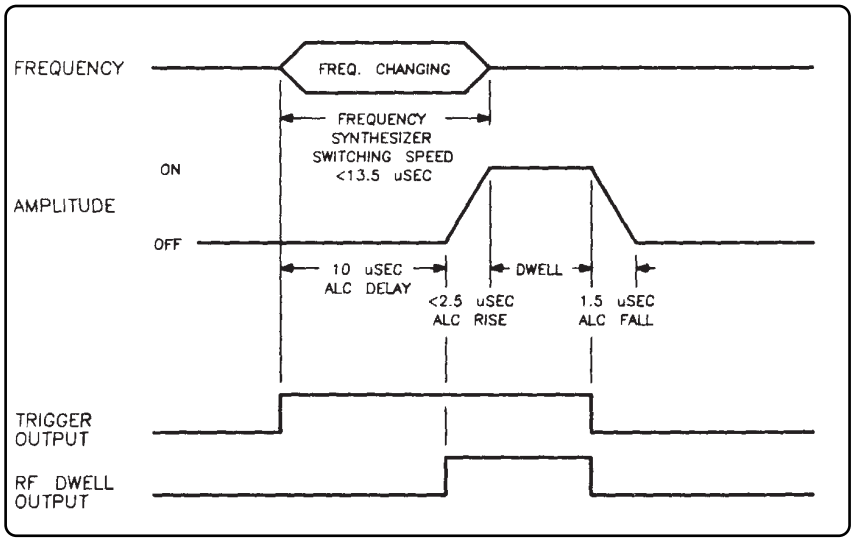


Figure 13. Internal Stepped Synchronization.

External Triggering

There are six external triggering modes. Tin-dng control and synchronization for each one is described in detail as follows:

Ext Repetitive

The *External Repetitive* mode causes the 8645A to repetitively frequency hop through the sequence table when the Hop State is activated. In this mode, the Hop State is activated by keeping a TTL high signal either on the rear-panel **HOP** connector, or on the Fast Hop *Bus HOP* line. When the TTL signal is dropped to a low state, frequency hopping is suspended.

The following diagram in Figure 14 depicts the synchronization that occurs when the 8645A frequency hops in the External Repetitive mode:

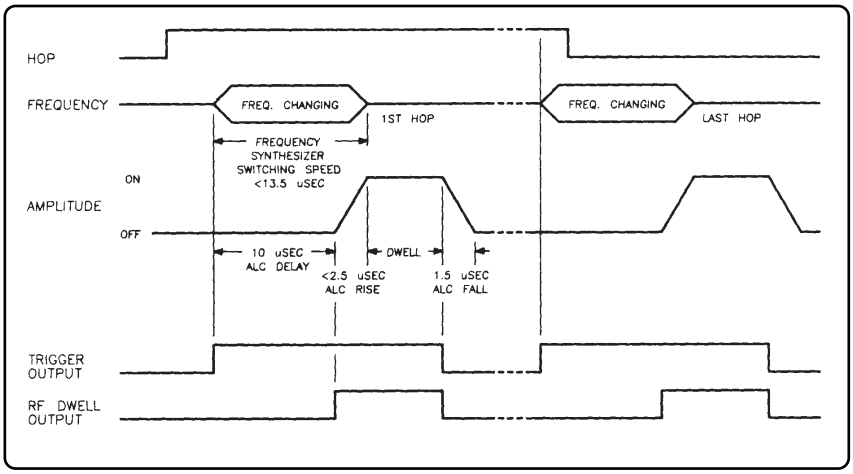


Figure 14. External Repetitive Synchronization.

Ext Single

The *External Single* mode allows the 8645A to frequency hop once through the sequence table when the Hop State is activated. In this mode, the Hop State is activated by an external TTL signal. At the completion of the External Single sequence, the 8645A remains in the Hop State with the RF output turned off and waits for another Hop command.

The rising edge from a TTL signal, input to the rear-panel **HOP** connector, or on the Fast Hop Bus *HOP* line, causes the 8645A to cycle once through the sequence table after completing a learn operation. Hop rate and dwell time are fixed at the internally set values.

To cycle through the sequence table again, the 8645A must re-enter the Learn State by a low TTL signal input pulse to the rear-panel **SEQ** connector. Then, the rising edge of the next TTL signal input to the rear-panel **HOP** connector will activate the Hop State for another External Single sequence.

The following diagram in Figure 15 depicts the synchronization that occurs when the 8645A frequency hops in the External Single mode:

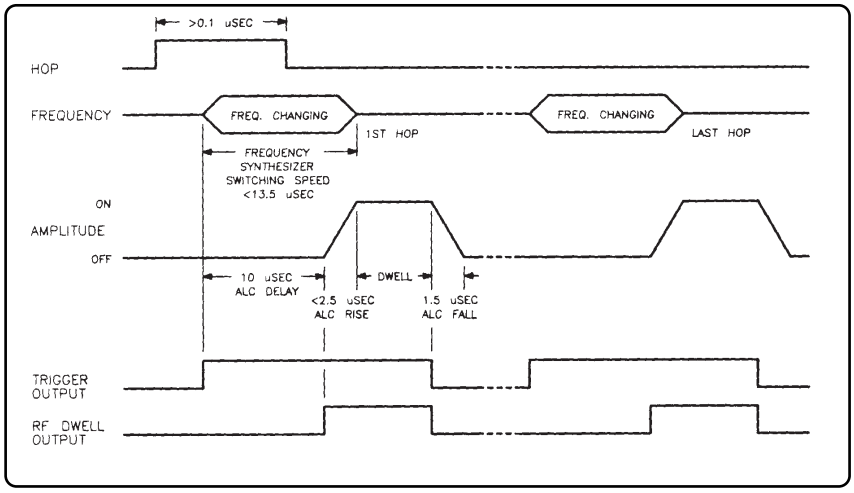


Figure 15. External Single Synchronization.

Ext Stepped Int Dwell

The *External Stepped Internal Dwell* mode allows the 8645A to cycle through the sequence table one channel at a time. In this mode, the user externally controls the hop rate; dwell time is fixed at the internally set value.

When this mode is active, the rising edge from a TTL signal, input to the rear-panel **HOP** connector, or on the Fast Hop Bus HOP line, causes the 8645A to change to the next channel in the sequence table. The RF output remains on for the duration of the dwell time.

The following diagram in Figure 16 depicts the synchronization that occurs when the 8645A frequency hops in the External Stepped Internal Dwell mode:

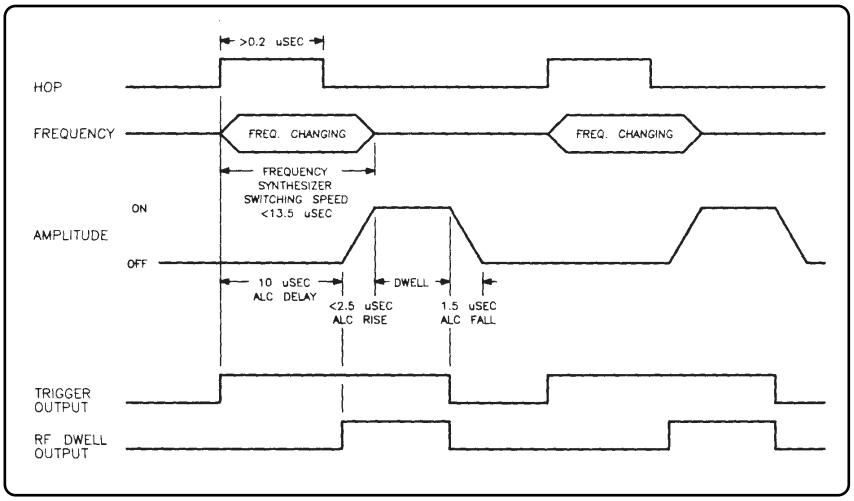


Figure 16. External Stepped Internal Dwell Synchronization.

Ext Stepped Ext Dwell

The *External Stepped External Dwell* mode allows the 8645A to cycle through the sequence table one channel at a time. In this mode, the user externally controls the hop rate and dwell time. The dwell time and hop rate can be varied for each channel in the sequence table while the 8645A is frequency hopping.

When this mode is active, a TTL signal input to the rear-panel **HOP** connector, or on the Fast Hop *Bus HOP* line, controls the hop rate and dwell time. The 8645A changes to the next channel in the sequence table on each rising edge of the TTL signal.

Keeping the TTL signal in a "high state" causes the RF output to remain on. Returning the TTL signal to a "low state" causes the RF output to shut off. The TTL signal must be in a low state for at least the ALC fall time between frequency hops.

The following diagram in Figure 17 depicts the synchronization that occurs when the 8645A frequency hops in the External Stepped External Dwell mode:

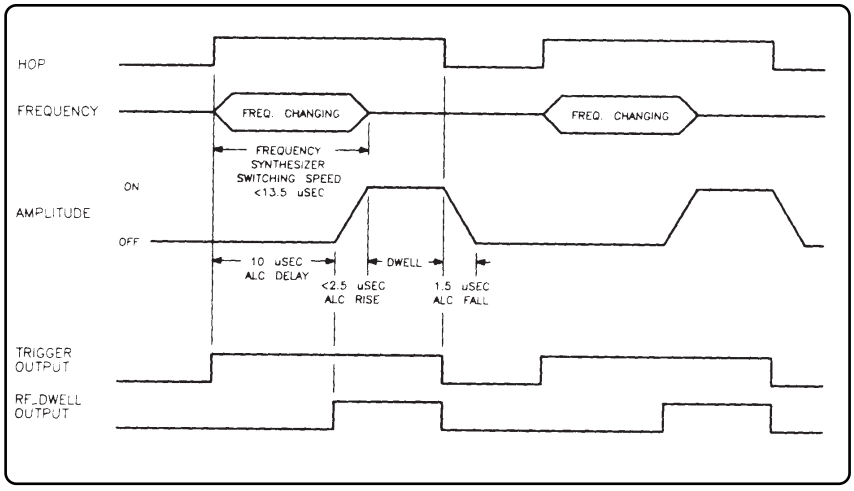


Figure 17. External Stepped External Dwell Synchronization.

Fast Hop Bus Int Dwell

The *Fast Hop Bus Internal Dwell* mode allows the 8645A to frequency hop in any order to any channel in the sequence table. In this mode, the dwell time is fixed to the internally set value.

This mode and the *Fast Hop Bus External Dwell* mode have the most complicated synchronization, and require more external hardware for control than any of the other seven frequency hop modes.

To frequency hop in this mode, you are required to interface TTL signals to the rear-panel **FAST HOP BUS** connector, **SEQ** (sequence) connector, and **HOP** connector (only if it is used instead of the Hop line on the Fast Hop Bus).

Place a high/low TTL bit pattern on the 12 Memory Address lines to address the sequence table. The address data on the Fast Hop Bus will correspond directly to one of the 4000 positions in the sequence table.

For example, the Memory Address lines shown in Table 6 can be set up to correspond to "Step # 54" in the sequence table by sending specific address data over the Fast Hop Bus (add up the decimal equivalent for each Memory Address Line that is high to arrive at the address position in the sequence table):

$$32 + 16 + 4 + 2 = 54$$

Memory Address Lines (J1 Pin #)	Decimal Equivalent	High/Low TTL Bit Pattern
11	2048	0 (MSB)
12	1024	0
25	512	0
24	256	0
23	128	0
22	64	0
21	32	1
20	16	1
19	8	0
18	4	1
17	2	1
16	1	0 (LSB)

Table 6. Memory Address Lines for the Fast Hop Bus.

Note

The sequence table contains up to 4000 channel table entries from address position 0 to 3999. However, if you add up the decimal equivalent for each Memory Address Line shown in Table 6, the result would indicate that positions greater than 3999 could be addressed. All address positions greater than 3999 are invalid.

Synchronize the Data Valid line to toggle to a TTL high when the address data is valid.

To frequency hop to a new channel in the sequence table, input the rising edge of a TTL signal to the Hop line on the Fast Hop Bus (or to the HOP connector).

Remember

The TTL level at the SEQ (sequence) connector determines if the 8645A is in the Learn State. A TTL high keeps the 8645A in the Hop State; a TTL low puts the 8645A into the Learn State.

In normal operation, the 8645A allows for a faster switching speed by buffering the position addressed in the sequence table. This results in a synchronization delay of one frequency hop over the Fast Hop Bus.

If you do not want a one frequency hop delay, and are willing to accept a 7 µsec slower frequency switching time, you can turn off the buffered Fast Hop Bus with Special Function 201. This special function only works with the Fast Hop Bus Internal Dwell mode. Also, if you turn the buffering off, the Hop line must be held at a TTL high for 3 msec or less.

The diagrams in Figures 18 and 19 depict the synchronization that occurs when the 8645A frequency hops in the Fast Hop Bus Internal Dwell mode with and without the buffering.

Note

If you use the Fast Hop Bus Internal Dwell with the Buffering off, you will notice in Figure 3-19 that there is an overlap between when the frequency is changing and when the output amplitude comes on.

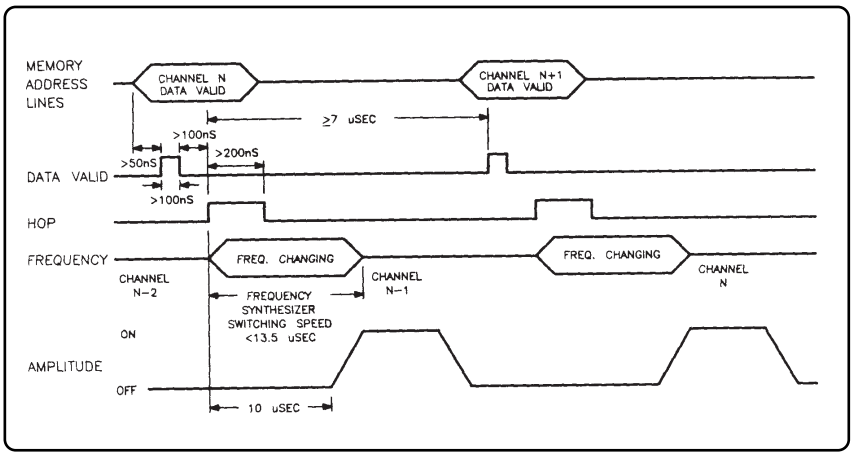


Figure 18. Fast Hop Bus Internal Dwell Synchronization, Buffering On.

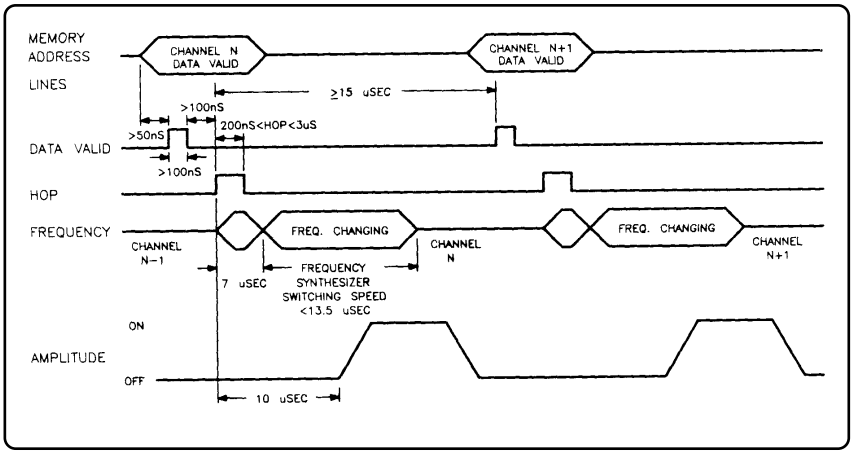


Figure 19. Fast Hop Bus Internal Dwell Synchronization, Buffering Off.

Fast Hop Bus Ext Dwell

The *Fast Hop Bus External Dwell* mode allows the 8645A to frequency hop in any order to any channel in the sequence table. In this mode, dwell time is controlled by the duration of the TTL signal on the Hop line.

This mode and the *Fast Hop Bus Internal Dwell* mode have the most complicated synchronization, and require more external hardware for control than any of the other seven frequency hop modes.

To frequency hop in this mode, you are required to interface TTL signals to the rear-panel **FAST HOP BUS** connector, **SEQ** (sequence) connector, and **HOP** connector (only if it is used instead of the Hop line on the Fast Hop Bus).

The variable dwell time in this mode allows you to have the RF output on for different amounts of time for each channel in the sequence table. As long as the TTL signal on the Hop line is high, the RF output is turned on; whenever the TTL signal on the Hop line is low, the RF output is turned off.

Place a high/low TTL bit pattern on the 12 Memory Address lines to address the sequence table. Address data on the Fast Hop Bus corresponds directly to one of the 4000 sequence table positions.

For example, the Memory Address lines shown in Table 7 can be set up to correspond to "Step # 342" in the sequence table by sending specific address data over the Fast Hop Bus (add up the decimal equivalent for each Memory Address Line that is high to arrive at the address position in the sequence table):

$$256 + 64 + 16 + 4 + 2 = 342$$

Memory Address Lines (J1 Pin #)	Decimal Equivalent	High/Low TTL Bit Pattern
11	2048	0 (MSB)
12	1024	0
25	512	0
24	256	1
23	128	0
22	64	1
21	32	0
20	16	1
19	8	0
18	4	1
17	2	1
16	1	0 (LSB)

Table 7. Memory Address Lines for the Fast Hop Bus

Note

The sequence table contains up to 4000 channel table entries from address position 0 to 3999. However, if you add up the decimal equivalent for each Memory Address Line shown in Table 7, the result would indicate that positions greater than 3999 could be addressed. All address positions greater than 3999 are invalid.

Synchronize the *Data Valid* line to toggle to a TTL high when the address data is valid.

To frequency hop to a new channel in the sequence table, input the rising edge of a TTL signal to the Hop line on the Fast Hop Bus (or to the **HOP** connector).

Remember

Remember

The TTL level at the SEQ (sequence) connector determines if the 8645A is in the Learn State. A TTL high keeps the 8645A in the Hop State; a TTL low puts the 8645A into the Learn State.

In normal operation, the 8645A allows for a faster switching speed by buffering the position addressed in the sequence table. This results in a synchronization delay of one frequency hop over the Fast Hop Bus.

If you do not want a one frequency hop delay, and are willing to accept a 7 msec slower frequency switching time, you can un-buffer the Fast Hop Bus by means of an external hop generating circuit. An example circuit shown in Figure 20 indicates that the **External Control Line** pulse must originate from a timing source that you provide.

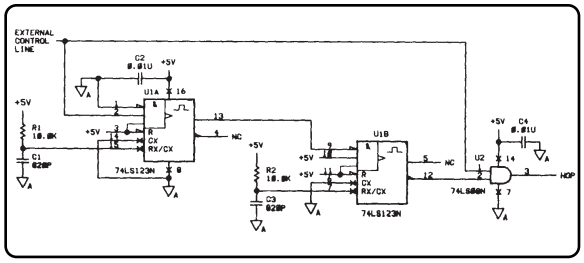


Figure 20. Sample Circuit to Control the Frequency Hop.

The following diagrams in Figures 21 and 22 depict the synchronization that occurs when the 8645A frequency hops in the Fast Hop Bus External Dwell mode with and without the buffering:

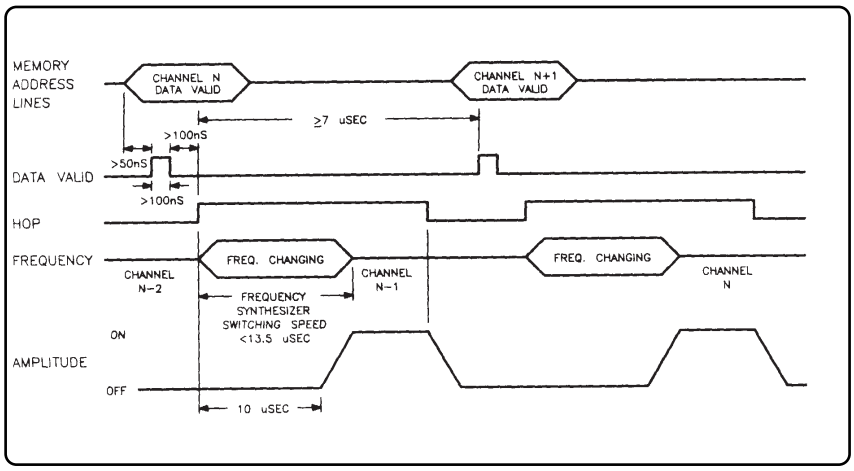


Figure 21. Fast Hop Bus External Dwell Synchronization, Buffering On.

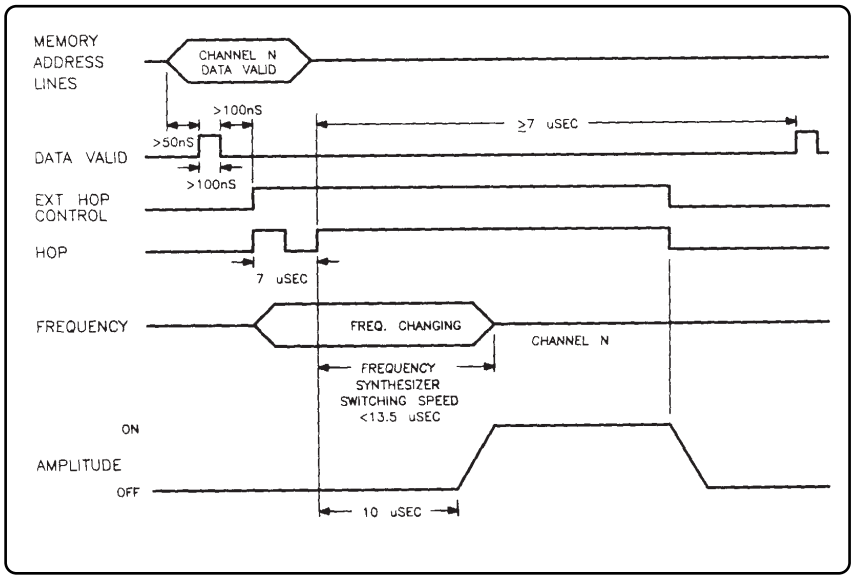


Figure 22. Fast Hop Bus External Dwell Synchronization, Buffering Off.

Amplitude Control

A maximum amplitude level variation of 20 dB is allowed between any two channels entered into the channel table. You can extend the amplitude level variation of the RF output by -15 dB during the Hop State without causing the 8645A to enter the Learn State by using special function 203.

Note

When Special Function 203 is envoked, the Fast Hop Operation, Amplitude accuracy specification, and the Amplitude Modulation, AM indicator accuracy specification will be degraded.

Amplitude level is controlled in one of two ways: Open, or Closed Loop ALC (Automatic Level Control). Each method has its advantages and disadvantages. You must decide which method best meets your needs.

Closed Loop ALC is the default method. Open loop ALC is selected by Special Function 202. If Pulse modulation is selected, Open Loop ALC is automatically turned on during the Learn State. Continue reading for a detailed discussion of both Open, and Closed Loop ALC.

Closed Loop ALC

Closed Loop ALC operation quickly turns on the RF output by 40 dB, and then exponentially ramps up to the desired level. In the same manner, the RF output exponentially ramps down to turn off. After this initial power drop, the RF output is quickly shut off by an additional 40 dB. Refer to figure 23.

The main disadvantage of operating with Closed Loop ALC is:

1. A longer switching time between frequency hops.

There are six main advantages of operating with Closed Loop ALC as follows:

1. Less spectral splatter.
2. Better linear AM control of the RF output level.
3. Better isolation between frequency hops.
4. Better level accuracy.
5. Power is off during the Learn State.
6. Shorter Learn State time.

During the Learn State with Closed Loop ALC operation, the RF output is turned off by about 70 dB while the 8645A learns all of the electronic settings for each channel in the sequence table. This prevents the output of undesired signals prior to the frequency hop.

The following diagram in Figure 23 depict Closed Loop ALC operation during the frequency hop:

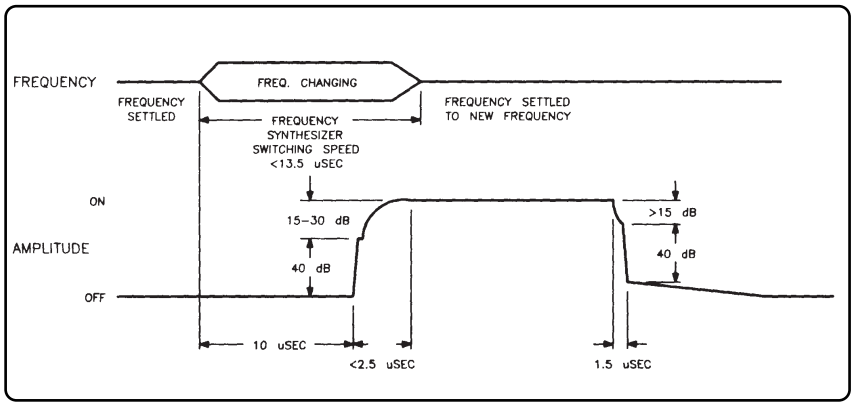


Figure 23. Closed Loop ALC Amplitude Control.

Open Loop ALC

Open Loop ALC operation turns on the RF output by quickly ramping up the amplitude level to 40 dB in less than 100 nsec. In the same manner, the RF output quickly turns off as it ramps down 40 dB in less than 100 nsec. Refer to Figure 24.

The main advantage of operating with Open Loop ALC is:

1. A quicker switching time between frequency hops.
There are six main disadvantages of operating with Open Loop ALC as follows:

1. More spectral splatter.
2. Less linear AM control of the RF output level.
3. Less isolation between frequency hops.
4. Less level accuracy.
5. Power is on during the Learn State.
6. Longer Learn State time.

During the Learn State with Open Loop ALC operation, the RF output is turned on and off while the 8645A learns all of the electronic settings for each channel in the sequence table. This increases the Learn State time by about 3 msec for each channel.

The following diagram in Figure 24 depict Open Loop ALC operation during the frequency hop:

Note

There is an overlap between when the frequency is changing and when the output amplitude comes on

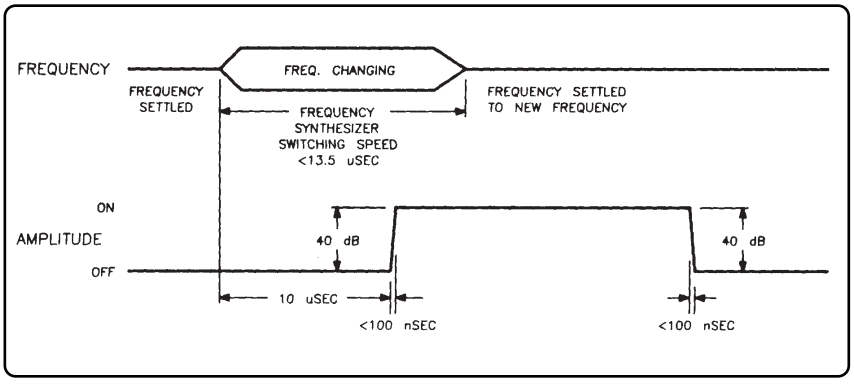


Figure 24. Open Loop ALC Amplitude Control.

Frequency Hop Example

The following exercise is made up of two procedures. The first procedure demonstrates how to frequency hop the 8645A in the Int Single mode. The second procedure demonstrates how to frequency hop the 8645A in the Ext Stepped Int Dwell mode. Each procedure takes about 10 minutes to complete.

Equipment Needed

Both procedures require use of the following equipment:

Equipment	Recommended Model Numbers
Spectrum Analyzer	8562A/B, or 8566B, or 8568B
Function Generator	3312A, or 3314A, or 8111A, 8116A, or 8904A

Procedure # 1 - Internal Single Mode

Procedure # 1 starts with step 1 shown on the next page. A review of the six major steps in the procedure are as follows:

- Set up and adjust the Spectrum Analyzer.
- Set up six frequency hop channels.
- Enter the hop rate and dwell time.
- Set up the sequence table.
- Activate the Internal Single mode.
- Enable the Fast Hop State.

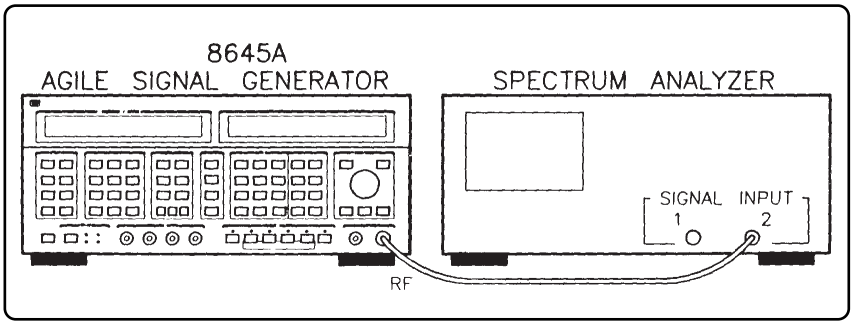


Figure 25. Equipment Setup for Internal Single Procedure #1.

Set Up and Adjust the Spectrum Analyzer

1. **Connect the 8645A to the Spectrum Analyzer as shown in Figure 25.** Turn on the equipment and make the following adjustments to the Spectrum Analyzer:

   Center Frequency .....100 MHz
   Frequency Span .....100 MHz
   Reference Level .....10 dBm

Set Up Five Frequency Hop Channels

2. **Press the green INSTR PRESET key.** Doing so presets the 8645A to a known state for the following steps.

3. **Press the MODE 5, FAST HOP key.** The yellow annunciator above this key lights up. The 8645A is now in the Idle State and is ready to accept modifications to the channel table, sequence table, hop rate and dwell time, and frequency hop modes.

4. **Set up the 8645A with the correct frequency and amplitude settings for channel 0, as shown in Table 8. Press the blue SHIFT key, and then press the ENTER key.** Repeat this step for channels 1-5 in Table 8.

Channel Number	Channel Frequency	Channel Amplitude
0	70 MHz	0 dBm
1	80 MHz	0 dBm
2	90 MHz	0 dBm
3	100 MHz	0 dBm
4	110 MHz	0 dBm
5	120 MHz	0 dBm

Table 8. Channel Table for the Internal Single Mode Procedure.

Enter the Hop Rate and Dwell Time

5. **Enter a hop rate of 8 Hz, and a dwell time of 100 msec.** Once again, the hop rate is slow and the dwell time long; this allows you to clearly see the results on the spectrum analyzer.

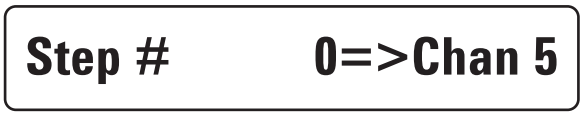
Set Up the Sequence Table

6. **Press the blue SHIFT key, and the SET SEQ** key. The 8645A is now ready for sequence table entries. You will see the following in the FREQUENCY/STATUS display:

Note

If a Step # other than "0" appears in the FREQUENCY/STATUS display, a sequence table has already been set up. If this is the case, clear the sequence table with the CLR SEQ key.

7. **Press the numeral 5 key.** This step sets up channel 5 for the first position (Step # 0) in the sequence table. You will see the following in the FREQUENCY/STATUS display:



8.**Press the ENTER key to put channel number 5 into sequence position Step #0**. Notice how the Step # increments up to the next sequence position, namely Step # 1.

9.**Continue to set up the sequence table with the pattern shown in Table 9. When you reach Step # 6, press the blue SHIFT key and the EXIT key to terminate entries into the sequence table.** When you are done with this step, a channel pattern of 5, 0, 4, 1, 3, 2 is ready for the frequency hop.

Sequence Step #	Channel
0	5
1	0
2	4
3	1
4	3
5	2

Table 9. Example Sequence Table.

Activate the Internal Single Mode

10. **Press the blue SHIFT key, and the MODE key.** You will see the fol lowing in the FREQUENCY/STATUS display:

Int Repetitive

11. **Turn the knob, or press one of the ⇑ ⇓ keys until "Int Single" is shown in the FREQUENCY/STATUS display.** The Internal Single mode is now activated.

12. P**ress the blue SHIFT key, and the EXIT key to get out of the frequency hop mode selection area.**

Enable the Fast Hop State

13. **Activate the Maximum Hold function on the Spectrum Analyzer.** The Maximum Hold function allows the Spectrum Analyzer to display all the channels as the 8645A frequency hops to them. If your Spectrum Analyzer does not have a Maximum Hold function, that's okay, just proceed to the next step.

14. **Press the blue SHIFT key, and the HOP key.** The AMPLITUDE dis plays shows Learning for about 10 seconds, and then the 8645A frequency hops once through the sequence table one Step # at a time. The following display should appear on the Spectrum Analyzer:

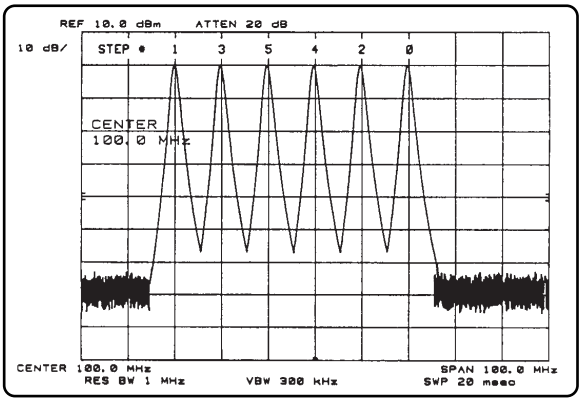


Figure 26. Amplitude Display

15. **Remove the Maximum Hold function from the Spectrum Analyzer. Press the blue SHIFT key, and the HOP key again.** You'll notice on the Spectrum Analyzer that the 8645A cycles through the sequence table once again. Every time the Hop State is activated in the Internal Single mode, the 8645A cycles once through the sequence table.

Procedure #2 - External Stepped Internal Dwell Mode

Procedure #2 starts with step 16 shown below; Procedure # 2 is a continuation of Procedure # 1. A review of the four major steps in the procedure is as follows:

- Set up and adjust the Function Generator.
- Activate the External Stepped mode.
- Enable the Fast Hop State.
- Modify the Results.

16. **Connect the 8645A to the Spectrum Analyzer and Function Generator as shown in Figure 27.** Keep the Spectrum Analyzer set to the adjustments made in Procedure # 1. Turn on the Function Generator and make the following adjustments:

    On the Function Generator

    Frequency .....1 Hz
    Amplitude .....1.5 Vpk
    Waveform .....Square

Activate the External Stepped mode

17. **Press the blue SHIFT key, and the IDLE key.** The 8645A must be in an Idle State before changing the frequency hop mode.

18. **Change the frequency hop mode from Int Single to Ext Stepped Int Dwell, and then exit.** The following should be shown in the FREQUENCY/STATUS display before you exit:

Ext Stepped Int Dwell

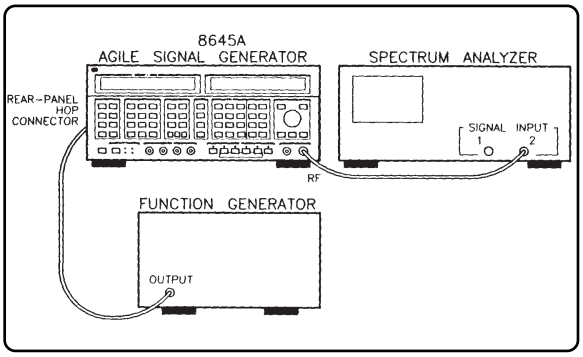


Figure 27. Equipment Setup for External Stepped Internal Dwell Procedure # 2.

Enable the Fast Hop State

19. **With the Function Generator's output active, press the blue SHIFT key, and the HOP key.** Once again, the Learn State is invoked for about 10 seconds. Notice on the Spectrum Analyzer that the 8645A frequency hops from one channel in the sequence table to the next at a 1 Hz rate.

Modify the Results

20. **Slowly increase the rate of the Function Generator's output.** Notice on the Spectrum Analyzer that the 8645A frequency hops at a faster rate which is proportional to the increased rate of the Function Generator.

Frequency Hop Example-Things to Remember

The following list is a summary of the most important points previously discussed in the Frequency Hop Example:

- Channel and sequence table entries are made with the 8645A in the Idle State.
- Any channel may be used more than once in the sequence table.
- Activate any of the nine frequency hop modes by showing your selection in the FREQUENCY/STATUS display.
- The Learn State is invoked before the Hop State to ensure the most accurate RF output while frequency hopping.

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Product specifications and descriptions in this document subject to change without notice.

Printed in USA November 13, 2001
5951-6711

Agilent Technologies