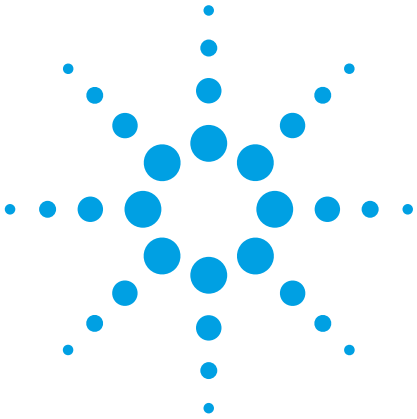
PLL and Jitter Spectrum Analysis using the 86100C Digital Communications Analyzer

Product Note 86100C-2



- **Flexible and accurate technique for PLL bandwidth/jitter transfer analysis**
- **Identification of the root causes of jitter**
- **Jitter spectrum and phase noise analysis on both clock and data**
- **Large dynamic range**
- **Emulate system response through virtual PLL's**
- **Accurate measurements made in seconds**

Agilent Technologies

Introduction

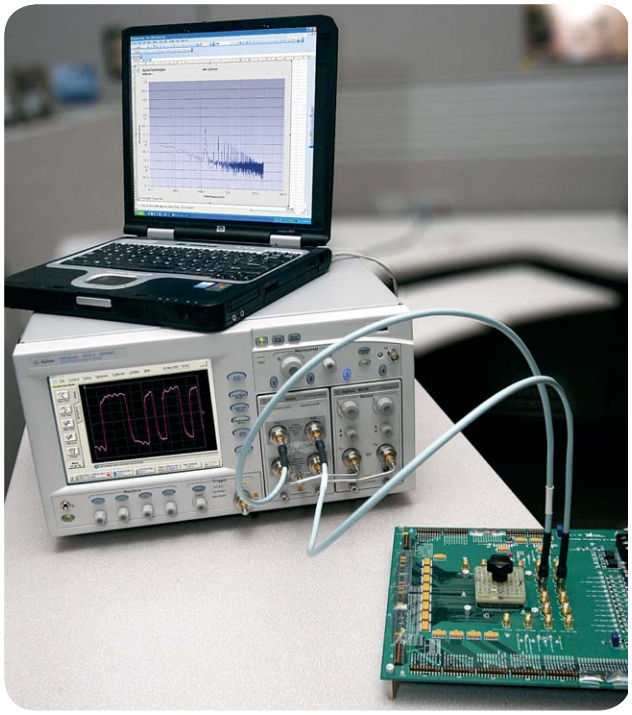
The 86100C Infiniium DCA-J Digital Communications Analyzer is well known for its speed, accuracy, and ease-of-use as a jitter measurement tool. (See Agilent Technologies Product Note 86100C-1). With a simple press of a button, the jitter of a signal is broken down into its various components including random, periodic, duty cycle distortion, and inter-symbol interference. Precision estimates can then be provided for aggregate deterministic and total jitter.

Further insight into jitter properties is achieved by observing the spectral (frequency domain) components of jitter. The DCA-J can isolate and display periodic jitter frequencies and amplitudes to help identify sources of jitter. The sources of random jitter can also be spectrally resolved, but has not been part of the DCA-J solution. This has traditionally been achieved with a spectrum analyzer/phase noise analysis system to display the noise spectrum of an oscillator (clock) signal. However, data signals can also be viewed in the phase noise "domain". With the addition of the 86108A Precision Waveform Analyzer or 83496B Clock Recovery Module and an external PC running control software, the DCA-J is able to provide jitter analysis similar to a spectrum analyzer based phase noise test system. The key benefits of the new system are:

- Provides an accurate and flexible technique to measure PLL bandwidth and jitter transfer
- Jitter spectrum, transfer and phase noise analysis on data as well as clock signals
- Insight into the root causes of jitter and how they can be controlled
- High dynamic range to simultaneously view large periodic jitter and low level noise
- Jitter spectrum from > 10 ns to < 1 fs
- Phase noise to < –106 dBc/Hz at 10 kHz offset
- Emulate PLL responses to observe system level effects
- Display phase noise (dBc/Hz), or jitter in seconds in the jitter frequency domain

The 86100C with the 86108A or 83496B technique provides these results through internally monitoring the phase detector output of the 86108A or 83496B clock recovery system. Jitter is not obtained from edge position analysis on a long waveform data record. Instead the phase detector of the clock recovery system effectively acts as a jitter demodulator, providing an analog signal that is representative of the jitter on the incoming clock or data signal. The measurement technique provides some important advantages over other oscilloscope based techniques:

- PLL bandwidth and jitter transfer can be measured on a variety of devices with any combination of data or clock inputs and data or clock outputs. For example, measure the PLL bandwidth of a transmitter with a 100 MHz reference clock input and a 2.5, 5 or 8 Gb/s output
- Input or output data rates from 50 Mb/s to 13.5 Gb/s or clock rates from 25 MHz to 6.75 GHz
- Measurement frequency span is independent of oscilloscope waveform record length
- Does not require acquisition of a long waveform record resulting in fast measurement times and simpler post-processing
- Simultaneously observe jitter spectrum results and the time domain waveform



For a detailed explanation on making these measurements using the 86100C/83496B or 86108A system, including specifics on setup and operation, go to ***www.agilent.com/find/jtf*** *for the 86100C-400 Measurement and Compliance Suite Users Guide (part number 86100-90110).*

A system level look at jitter

An in-depth discussion on jitter definitions and the benefits of jitter analysis through observation of phase noise are found in "Using Clock Jitter Analysis to Reduce BER in Serial Data Applications, Agilent Literature number 5989-5718EN". (Phase noise analysis using the 86100C/86108A or 83496B system was not available at the time this document was written.). While the above mentioned document is mainly devoted to the analysis of clock signals, the basic theory can also be extended to data signals, as the jitter present on clocks often translates onto a data stream.

Jitter can come from a variety of sources. It is useful to examine the basic architecture of a generic serial data system and discuss the mechanisms that create jitter within each element. Just as important is understanding how jitter from one element can affect the jitter performance of another element. The basic system consists of a transmitter, a channel, a receiver, and a reference clock. Phase-locked Loops (PLL's) are commonly used to manage or create timing across the system and can have a significant impact on overall jitter performance. The system is intended to be generic and include distributed, forward, and embedded clock architectures.

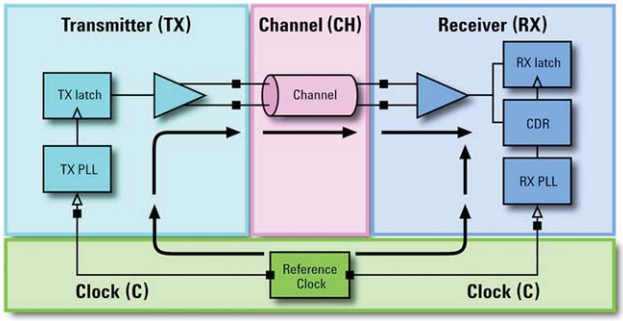


Figure 1. Generic serial bus communications system

Reference clocks:

The reference clock determines the data rate of the serial bus system. If the reference clock fluctuates in frequency, the data rate of the system will also fluctuate (jitter!). Jitter mechanisms in the reference clock include random jitter from noise mechanisms within the oscillator, periodic jitter from spurious oscillator sidebands, and duty cycle distortion from oscillator nonlinearities.

Transmitters:

To produce data, the transmitter derives its timing from a clock source. The transmitter typically multiplies up the reference clock to achieve the desired data rate. The multiplication is usually achieved with some form of PLL. In the process of multiplication, the PLL will add some jitter (typically random jitter from its internal oscillator). The jitter from the reference clock may also be imposed on the multiplied clock. The total jitter at the output of a PLL depends on the jitter spectrum of both the data and the VCO contained within the PLL. The jitter from the reference oscillator is multiplied by the PLL jitter transfer function (PLL loop bandwidth), which filters the high frequency components of the jitter, but preserves the low frequency jitter. The jitter from the VCO is multiplied by the jitter transfer complement (since the VCO is inside the loop), which passes the high frequency components of the VCO jitter while reducing the low frequency components. The loop effectively removes the high frequency jitter on the reference and the low frequency jitter on the VCO. Noise from other components inside the loop such as the amplifiers and phase detectors can be added to the VCO jitter to get a more complete picture of the jitter spectrum. The PLL bandwidth settings can help reduce jitter, as jitter that is within the loop bandwidth is what is transferred to the serial data. Given the effects of PLL loop bandwidth, a frequency domain view of jitter is critical to understanding how jitter propagates and how it can be controlled. An accurate knowledge of the PLL bandwidth provides important insights into the root causes of transmitter jitter.

The transmitter can also have jitter from mechanisms that are not related to the reference clock, including random jitter from thermal effects, inter-symbol interference from limited bandwidth, and periodic jitter due to electromagnetic interference.

Observing the jitter on both the transmitter data and the reference clock is an essential element to understanding and improving the overall performance of the communications system.

Channels:

The channel can alter the time at which a signal crosses the ideal decision threshold (another way to describe jitter). This is typically due to limited bandwidth and is commonly referred to as inter-symbol interference.

Receivers:

Receivers can also produce jitter as there may be PLLs or other timing elements that are subject to random jitter mechanisms. Typically receiver jitter analysis deals with the ability of a receiver to achieve a good bit-error-ratio in the presence of jitter rather than determining the amount of jitter that is created. However, if a receiver obtains its timing information from a reference clock, the receiver can be subject to the same jitter transfer and amplification issues as the transmitter.

When jitter becomes large enough, it can cause receivers to make mistakes and degrade the BER of a communications system. To minimize the effects of jitter, it can be reduced at the point it is created, or it can be managed at downstream points in the signal path. In either approach, the more that is known about the jitter, the better the chances that it can be dealt with efficiently.

The PLL design can be optimized through knowing the spectrum of the jitter it will encounter and accurate measurement of its jitter transfer performance.

The basics of frequency domain jitter analysis

The ideal reference clock oscillator will produce a simple sinusoid at the desired frequency:

$$v_{ideal}(t) = v_o \sin 2\pi f_c t$$

In the time domain this signal is seen as the basic sine function. In the frequency domain, the signal is seen as a single spectral line.

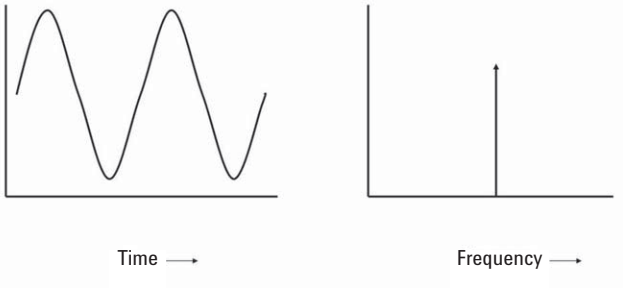


Figure 2. Time and frequency representations of a simple sinusoid

No oscillator is perfect. A real oscillator will produce a signal described by:

$$v_{real}(t) = (v_o + \Delta v(t)) \sin (2\pi f_c t + \varphi(t))$$

Where: $\Delta v(t)$ represents signal fluctuation due to amplitude noise

$\varphi(t)$ represents fluctuations in the phase of the clock signal

In the time domain this signal will fluctuate in amplitude, in addition to the expected sinusoidal variation, and have an inconsistent period. In the frequency domain, the signal is no longer a discrete spectral line. There is now spreading of the spectrum – unintentional amplitude and phase modulation causing spectra both above and below the nominal signal frequency.

To understand how a signal has been degraded by jitter, it is helpful to examine the frequency domain spreading of the signal in detail. The spread of the clock spectrum is typically symmetric. That is the spectrum above the main signal is a mirror image of the spectrum below the main signal. A useful approach is to simply look at the upper modulation alone, in terms of its offset position from the ideal signal ("carrier"). As the spreading of the ideal signal is often dominated by random noise processes, it is useful to determine the sideband energy over a specific spectral width, typically 1 Hz. A phase noise plot is a display of the phase modulation of a signal, plotted as the energy of the signal in a 1 Hz bandwidth compared to the total energy of the signal.

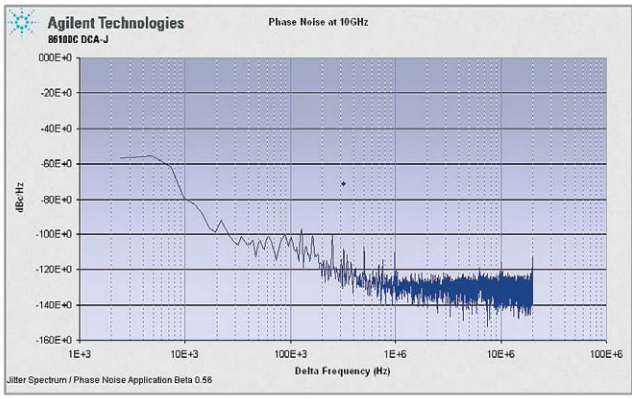


Figure 3. Phase noise plot

The phase noise plot presents some valuable insights into the nature of random jitter. Different noise mechanisms have different profiles.

- Random walk frequency modulation follows a f^{-4} slope
- Flicker FM noise follows a f^{-3} slope
- White FM noise follows a f^{-2} slope
- Flicker phase modulation follows a f^{-1} slope
- White phase noise is flat versus frequency

The jitter spectrum

Phase noise and jitter spectrum plots both provide a view of the spectral purity of a clock signal. Although the two plots both quantify the spectral purity as a function of frequency offset from the carrier, the y-axis is scaled differently for the jitter spectrum compared to the phase noise.

A phase noise measurement is normalized to the clock frequency, the carrier power, and to a 1 Hz resolution bandwidth. The units for the y-axis of a phase noise plot are dBc/Hz. In a frequency division multiplexed system such as cellular telephone the phase noise of the carrier can lead to adjacent channel interference. The level of the interference depends on the receiver bandwidth and the phase noise is simply multiplied by the receiver bandwidth (add 10 times the logarithm of the bandwidth) in Hertz to get the interference level. Discrete frequencies in the phase noise plot cannot be correctly interpreted unless the resolution bandwidth of the actual measurement is known. The phase noise plot is generally preferred by wireless communication system designers since the magnitude is relative to the carrier power and normalized to a 1 Hz system bandwidth allowing a quick calculation of system dynamic range for a given receiver bandwidth at an adjacent channel.

In contrast, the jitter spectrum plots the magnitude in seconds (rms) and the data is not normalized for the measurement resolution. Digital link designers generally prefer this representation since the jitter is absolute allowing direct comparison of sub rate clocks with full rate clocks. The jitter spectrum can preserve phase information so that any deterministic components of the spectrum (such as SSC) can be processed and reconstructed in the time domain. The random noise can also be integrated to get the total root mean square (rms) random jitter. This allows construction of probability density functions required for BER estimation. See figure 11.

Jitter Spectrum and Phase Noise on Data Signals

When digital data are transmitted, the rate at which bits are produced is typically set by some reference clock. The transmitter may multiply a low rate reference clock by an appropriate factor to get the correct data rate. The PLL multiplier both amplifies the jitter on the clock and introduces its own jitter, primarily RJ from the PLL VCO. The performance of the reference clock, whether good or bad, is transferred to the transmitter.

The time domain representation of a jitter-free data stream is intuitively simple. The frequency domain representation is more complicated. The diverse pattern of ones and zeroes with a large variety of times between data edges leads to the line spectra in the frequency domain that follow a sin (x)/x envelope, with spectral nulls at the data rate and its harmonics (NRZ data). For data from a repeating pattern/sequence, the spacing between the line spectra is the pattern repetition frequency.

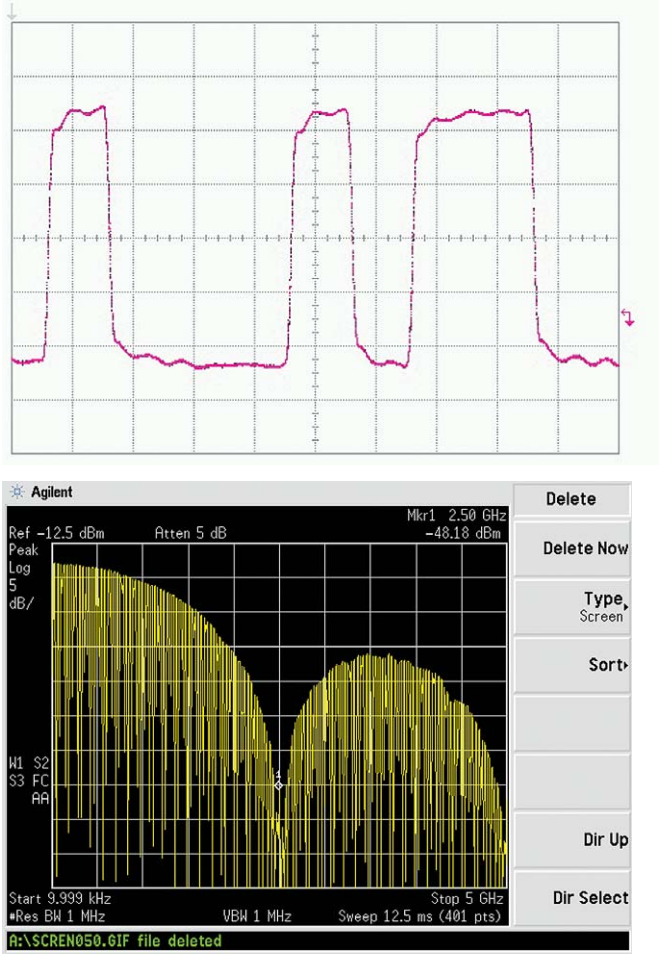


Figure 4. Data in time and frequency

If a transmitter is timed by a jittery clock, the clock jitter can be transposed to the data stream. In the time domain the edges of the data will be misplaced from their ideal time positions just as they are for the clock. This is easy to observe and interpret in the time domain, but difficult to interpret in the frequency domain. Random jitter causes the energy of each spectral line to spread. Jitter transfers power from each spectral line into modulation sidebands. Unless the data pattern is very short, or the bandwidth of the modulation is very narrow, the spectrum due to jitter at one spectral line will overlap with the adjacent lines.

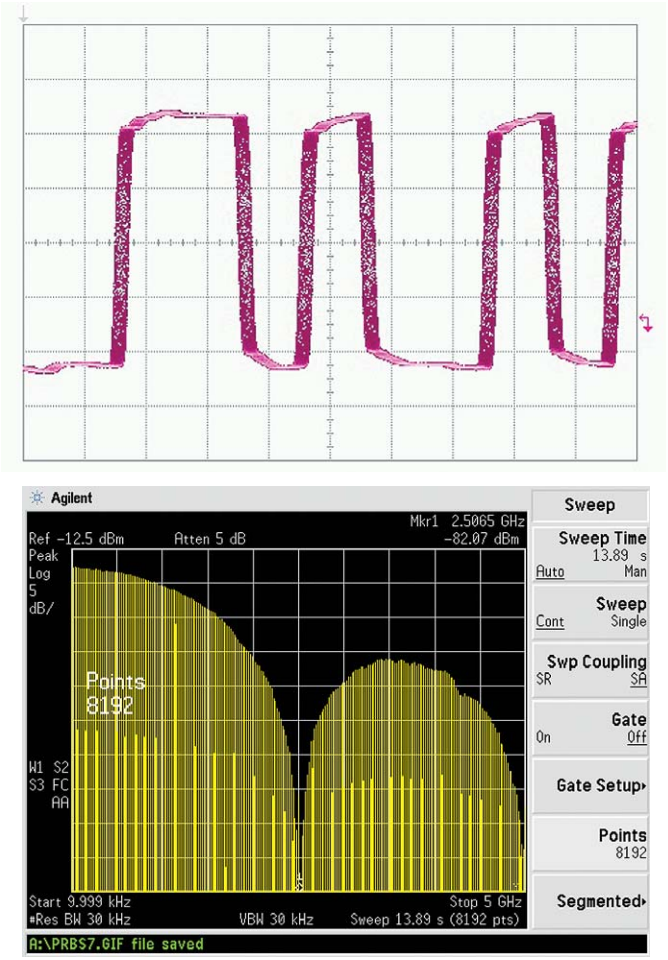


Figure 5. Time and frequency representation of jittery data

This complicated "overlapping" spectrum makes it impossible to derive the jitter or phase noise spectrum of a data stream using a spectrum analyzer based test system. The 86100C/86108A or 83496B system can observe the jitter or phase noise spectrum of data signals. This architecture has two distinct advantages over a spectrum analyzer based instrument. Since the phase detector in this system is designed to sense the phase difference between the recovered clock and the data, the measurement is not limited to clock signals but can be made on a data signal. In this case the jitter spectrum is that of the equivalent clock for the data signal being measured. Also, clock recovery circuits typically have wide bandwidth analog PLLs capable of tracking or tolerating large wander and modulation typically found in clock signals for personal computer busses, such as with SSC. The jitter transfer and subsequent complementary or observed jitter transfer (OJTF) of the clock recovery circuit are internally measured. This allows the Fourier transform of the error signal which is divided by the OJTF to calculate the total jitter on the input signal. This enables the system to measure higher magnitudes of jitter at low frequencies, as is the case with SSC.

Using frequency domain jitter analysis to characterize PLL bandwidth and jitter transfer

Jitter transfer is a measure of how much jitter is present at the output of a device compared to the level of jitter that is present at the input of the device. The output versus input ratio is usually measured over a range of jitter frequencies. The concept is similar to a frequency response measurement of an RF component such as an amplifier where the input stimulus is a small-signal sinusoid that is swept over a range of frequencies. The output and input are monitored as the frequency is swept and the amplifier frequency response can be displayed.

This leads to the concept of a jitter transfer bandwidth. In devices that employ some form of clock extraction circuit or PLL, as the frequency of the jitter increases to high rates, the jitter transfer ratio will begin to drop from unity and continue to drop with increased jitter frequency. The key difference in this measurement technique compared to the amplifier frequency response discussed above is that the input signal has a fixed nominal rate. However, the input signal is intentionally phase modulated. The frequency of the modulation is swept over the range of interest.

For example, a transmitter operating at 2.5 Gb/s may use a 100 MHz clock as its timing reference. A PLL-based multiplier circuit within the transmitter can be used to create a 2.5 GHz clock from the 100 MHz input and the transmitter output will be a 2.5 Gb/s data stream. If there is jitter on the reference clock, how much will be present on the output data? This is described by the jitter transfer measurement.

A 100 MHz clock is frequency modulated. The frequency of the modulation is initially low (perhaps 200 kHz) and sequentially incremented logarithmically to multiple decades to 20 MHz or higher. At each modulation frequency, the magnitude of the jitter is measured both at the input and the output of the transmitter. The jitter measurement is achieved using the phase detector technique discussed above. (Note that the measurement system controls the frequency and magnitude of the jitter stimulus, hence it 'knows' to look for and examine a specific jitter tone). Knowing the input jitter and the output jitter at a multitude of jitter frequencies allows the jitter transfer response to be constructed. From the jitter transfer response, PLL bandwidth and peaking parameters can be extracted.

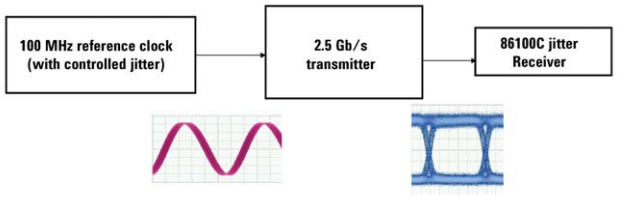


Figure 6: PLL/jitter transfer test system block diagram

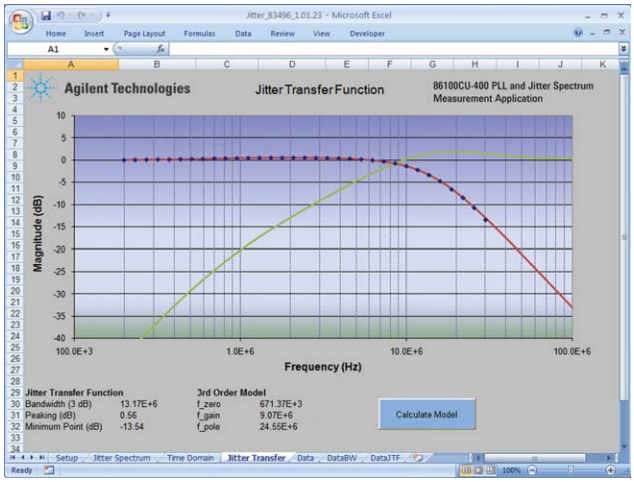


Figure 7: Jitter transfer/PLL bandwidth result for a PCI-Express transmitter

The measurement concept can be extended to a variety of device types. A clock recovery circuit is measured similarly to the transmitter discussed above. However in this case, the input stimulus will be data with controlled jitter and the output response can be either the derived clock signal or the regenerated data signal. The basic measurement is still the ratio of the jitter on the output (data or clock) to the jitter on the input data signal. The last of the four classes of measurements the system can measure is for a "clock in/clock out" system such as a clock multiplier circuit.

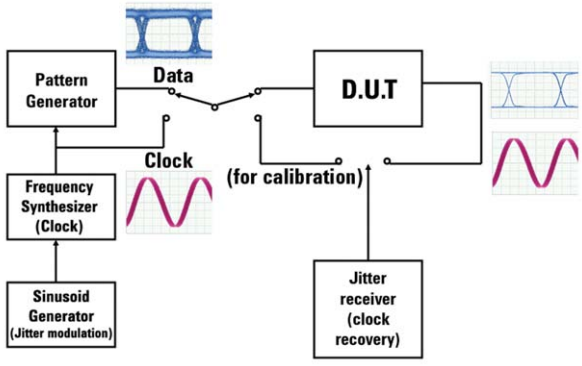


Figure 8: The test system is capable of four possible combinations of clock or data at the input or output of the test device

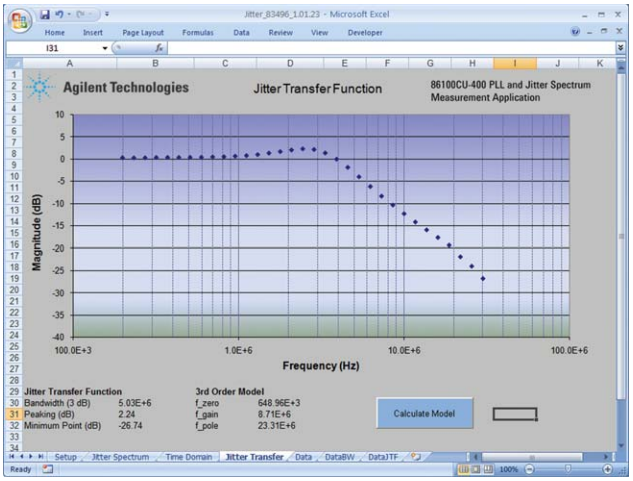


Figure 9: Jitter transfer/PLL bandwidth result for a 5 Gb/s clock recovery circuit

Configuring a PLL bandwidth/jitter transfer measurement system

The test system consists of a source to produce a jittered clock or jittered data to stimulate the test device, and a jitter receiver to measure the test device response. As mentioned, the jitter receiver is implemented through the clock recovery system of either the 86100C/86108A or 86100C/83496B. These clock recovery systems are based on Hogge phase detectors, which are ideal for high-performance instrumentation in that they provide repeatable and accurate results even when the transition density of the test signals vary significantly from the typical 50%. Several instruments can be configured as jitter sources. The fundamental requirement is that the 86100C test system controller must be able to set the magnitude and frequency of the jitter and the rate of the clock or data. The following list indicates instruments that have been verified for proper system operation:

Agilent N4903A JBERT: The JBERT provides the ideal jitter source, as it has an internal jitter system and can produce either clock or data signals over a very wide range of rates. The N4903A also provides the most stable and repeatable jitter source.

Agilent 81150A 120 MHz Function generator: This function generator can provide a jittered reference clock for serial data transmitters.

Agilent N5182A MXG RF Vector Signal Generator: This signal generator can provide jittered clock signals at rates to 6 GHz. It can serve as a clock source stimulus or as a clock for a pattern generator to produce jittered data. For a differential clock signal, a balun is required.

Agilent E8267D Precision Signal Generator: This signal generator can produce clock signals with precise amounts of jitter or be used to time a pattern generator for precise amounts of jitter on a data stream or as a jittered clock stimulus. I/Q modulation capability is required

Agilent 33250A function generator: This source can be used to generate jitter at specific amplitudes and frequencies. It can modulate pattern generators and BERTs that have delay line modulation inputs to provide jittered data or clock signals.

Enhancing PLL bandwidth/jitter transfer measurement accuracy through calibration

While the hardware used in the jitter transfer measurement is stable and repeatable, measurement accuracy can be enhanced through some basic calibration steps. The largest contributors to inaccuracy are unflatness of the source (jittered data or jittered clock) and the unflatness of the jitter receiver. For example, if the jittered source fluctuates in jitter magnitude as the jitter frequency is incremented, the magnitude variation could be incorrectly interpreted as being the response of the test device. Similarly, if the jitter receiver accuracy varies according to the jitter frequency, it can be difficult to distinguish this from variation in the device under test (DUT). However, test system unflatness can be normalized out of the measurement result through a two-step measurement process and eliminate the bulk of measurement errors. This allows for an accurate measurement without relying on a factory based calibration of the system.

Prior to measuring the DUT, a calibration measurement is made with the source connected directly to the receiver (with the DUT removed). The source will increment its jitter frequency, with each frequency point measured by the receiver. If the source produces the expected jitter level at each frequency, and the receiver precisely measures the expected value, the transfer result would be a flat line (assuming a constant jitter magnitude was configured by the source). If either the source or the receiver does not have a flat response, the resulting measurement will include this unflatness. The overall flatness of the entire test system is observed.

The DUT is then placed between the jitter source and the jitter receiver. The resulting response will be due to the combination of the test system and the DUT. However, if the DUT measurement is divided by the initial test system measurement (without the DUT), the result will be the response of the DUT alone. Any systematic unflatness of the test system should be common to both measurements and be removed from the DUT result.

The system calibration process can be complicated by the fact that many test scenarios are for DUTs that produce an output signal that is very different than the input signal. For example, a transmitter that produces a data stream timed with a multiplied reference clock requires the test system source to produce a low rate clock signal (perhaps 100 MHz) and the test system receiver to accept a high rate data stream (2.5, 5, or 8 Gb/s). In the test system calibration step, if the source is set to produce a 100 MHz clock, the receiver will be measuring a signal that is different than what the DUT will produce. If the source is set to produce a high rate data stream, the receiver will observe a signal similar to the DUT output, but the source conditions will be different than what the DUT must receive. For the calibration process to be accurate, the calibration configuration should be as close as possible to the DUT test configuration.

In the above example, the problem is solved as follows. In the calibration setup, the source is configured to produce a data pattern identical to what the DUT will produce. The calibration measurement is made and recorded. Before the DUT is connected, the source data pattern is altered to mimic a 100 MHz clock. For example, if the DUT will produce a 2.5 Gb/s data stream, the source is set to 2.5 Gb/s, but the pattern is changed to 111111111111000000000000 and appears as a 100 MHz clock, which the DUT requires. If the DUT operates at 5 Gb/s, after calibration the source pattern is changed to 11111111111111111111111100000000 00000000000000000, remaining at 5 Gb/s. In this scenario, the only deviation in test system configuration from calibration to actual DUT test is the source pattern. Since the source jitter performance will vary little if at all with changes in pattern, the calibration process should eliminate any test system unflatness. While the procedure may appear complicated, from a user perspective it is achieved with little effort as it is automated as part of the PCI-Express ® compliance measurement.

In all scenarios, the objective is to have the calibration setup match the DUT measurement setup as closely as possible. Some test scenarios are easier than others. A clock recovery DUT will have identical calibration and measurement configurations if the DUT output is measured at the data line output(s), but will require adjusting the source pattern or receiver rate if the DUT clock output is to be measured rather than the data line. In the reference clock based transmitter discussed above, if the test system source is a simple clock source rather than a pattern generator, the preferred calibration technique (pattern adjustment) is not possible. Again, the calibration process should still be as close as possible to the DUT test configuration. If the source can only produce a 100 MHz clock, the calibration configuration will route this clock to the test system receiver set at 200 Mb/s (a 100 MHz clock is perceived as a 200 Mb/s 10101010 data stream). When the DUT is measured, the test system receiver must be changed to accept a signal at the full (2.5, 5 Gb/s etc.) data rate. The

calibration process will eliminate the majority of system unflatness, but it does rely on the test system receiver performance being consistent from 200 Mb/s to the full DUT data rate.

One technique that can be used to verify the stability and precision of the test system is to calibrate the system and then leave the test system source connected to the receiver. Ideally, any subsequent measurement should result in a flat line at 0 dB. If the system fluctuates, this will be observed as a transfer result that deviates from 0 dB.

Another important feature that enhances the precision of the jitter transfer result is "collision avoidance". It is not unusual for a test device to produce some periodic jitter at its output even when the input signal is jitter free. If this periodic jitter falls within the range of frequencies that are used to measure jitter transfer, it is possible that the jitter stimulus and the DUT produced jitter will 'collide' or interfere with each other. The self produced jitter can be misinterpreted as being a response to the test system stimulus and corrupt the jitter transfer measurement.

Prior to the jitter transfer measurement, the test system can observe the jitter spectrum of the DUT output signal and determine if any significant periodic jitter tones are present. The test system can then adjust the frequencies that will be produced by the stimulus so that transfer measurements are not made where interference with the DUT jitter might occur.

It is important to note that this technique provides an absolute measurement of jitter transfer. The ratio of output jitter to input jitter is measured directly. This is important when any measurements of PLL bandwidth or peaking are obtained. An absolute transfer measurement does not require an estimate of the jitter frequency where unity transfer (0 dB) occurs. A process that assumes unity (0 dB) transfer occurs at DC and then curve fitting or forcing low frequency measurement points back to DC can lead to measurement error if the true frequency response does not follow the curve fitting assumptions. In the 86100C system, bandwidth and peaking information are based on a direct measurement of the output to input ratio.

For a procedure on how to use the system, see 86100C-400 Measurement and Compliance Suite Users Guide (part number 86100-90110) found at **www.agilent.com/find/jtf**.

Using frequency domain jitter analysis to solve jitter problems: a case study

Reduction of jitter requires identification of its root causes. High-speed digital engineers have learned the benefits of separating jitter into its random and deterministic components, both for accurate assessments of total jitter to low probabilities as well as identification of jitter types. While jitter separation techniques can be used on clock signals as well as data signals, additional information is needed to really understand the performance of a signal, and perhaps more important, provide insight into how the jitter performance can be improved.

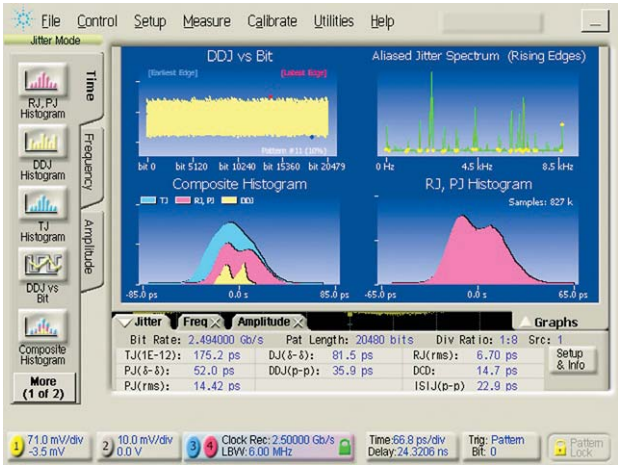


Figure10. Jitter histograms and components for a 2.5 Gb/s PCI Express data signal using 86100C jitter mode

Figure 10 shows the jitter measurement results for a PCI-Express data signal. The total jitter (TJ) at a probability of 10^{-12} is175 ps or 0.44 UI. There are several significant contributors to the jitter. Data dependent (DDJ) effects including ISI and duty-cycle distortion (DCD) are relatively small. Periodic jitter (PJ) is significant, and the random jitter (RJ) is large. Because the RJ is listed as an rms value assumed to represent the standard deviation of a Gaussian distribution, its impact on the TJ at a 10^{-12} level requires it be multiplied by ~ 14, making it the largest contributor.

Where does the jitter come from? The DCD can be due to DC offsets or differences in rise and fall times of signal edges. ISI can be due to device or channel bandwidth limitations. Both DCD and ISI effects are relatively easy to observe on the time domain waveform and can often be diagnosed with an oscilloscope. PJ and RJ can be observed with an oscilloscope, but it can be difficult to see the details necessary to determine root causes.

Observing the jitter spectrum of the data signal

Observation of the jitter spectrum provides a wealth of information on periodic and random jitter. Figure 11 shows the jitter spectrum for the PCI Express data signal of figure 10. The horizontal axis is logarithmic and is the frequency range of the measurement. The vertical axis is also logarithmic with units of seconds. This plot represents the spectrally resolved jitter of the data signal measured with the 86100/86108A or 83496B system.

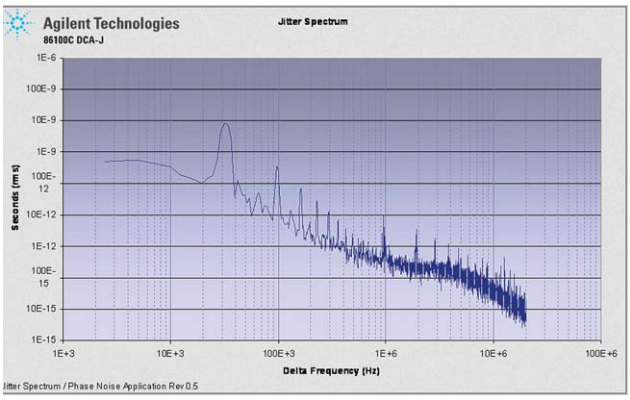


Figure 11. Spectrally resolved jitter of a PCI-Express data signal

The most dominant element of the plot is the wide spectral component at 33 kHz. This is the spread-spectrum clocking (SSC) used to pass electromagnetic interference requirements. This element results in approximately 10 ns rms of jitter. (It should be noted that the measurement of PJ as shown in figure 10 is made with the 86100C triggered with a clock derived from the data stream. The 86100C jitter mode measurement will display a significantly reduced value of SSC, as the triggering signal will have the same jitter as the signal being observed. See Product Note 86100-5 page 10. The measurement from the 86100/86108A or 83496B system is a direct jitter measurement and will show the full magnitude of the jitter versus frequency, including the full magnitude of the SSC component.) In addition to the SSC there are many distinct spectral components which are observed as lines or "spikes" in the spectral display.

The SSC is not a sinusoidal jitter mechanism, but rather causes the signal to deviate according to a triangle function. Thus there are spectral components at harmonics of 33 kHz (3X: 100 kHz, 5X: 165 kHz, 7X: 231 kHz and so on). The harmonic signals should roll off at a 60 dB per decade rate. SSC is an intentional or expected jitter mechanism. After the SSC harmonics have trailed off (they become insignificant and approach the spectral noise floor a little below 1 MHz) there is a significant spectral component at approximately 1 MHz. This is unexpected and requires a different view of the signal to determine its source.

Time domain waveform analysis

The jitter signal derived from the 86108A or 83496B phase detector can also be processed to display the delta frequency versus time of the input signal, indicating how far and how fast a data or clock signal varies from nominal frequency as a function of time.

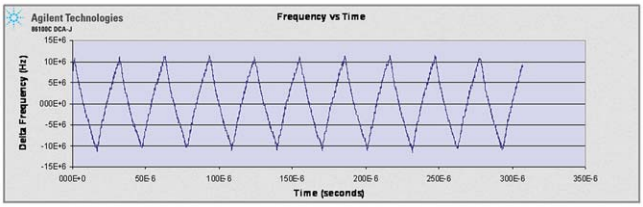


Figure 12. Delta frequency versus time for a PCI Express data signal

Figure 12 shows some expected and unexpected results. First, the frequency varies according to a triangular shaped function. This is the SSC intentionally imposed on the signal. However, the modulation is not quite triangular. The trajectory has some curvature rather than the true triangle function. This may be intentional. The trajectory of the frequency deviation is jagged, having a small, almost "staircase" shape riding on the SSC profile. At first glance, this might appear to be an artifact of a low resolution measurement. In reality, this is an indication that the frequency deviation of the SSC function is done in small steps rather than in a continuous fashion. Zooming in, the time between steps is slightly larger than 1 us. This explains the existence of the periodic jitter tones at just below 1 MHz and at harmonic multiples (2, 3, 4 ...MHz). A summarization of the SSC performance, including amplitude, frequency, and profile information is currently under development (August 2008) and will be available as part of the measurement suite.

The random jitter from the measurement of figure 10 was 6.7 ps. What is the root cause of this component of jitter? Can it be improved? Returning to the jitter spectrum plot of figure 12, random jitter is primarily seen as the noise of the jitter spectrum. In other words, if the spectral lines were removed, the residual spectrum represents the random jitter. The 6.7 ps random jitter (measured in the time domain) is the result of the aggregate noise spectra.

At this point it is useful to measure the 100 MHz reference clock that is used to synchronize the 2.5 GHz data signal.

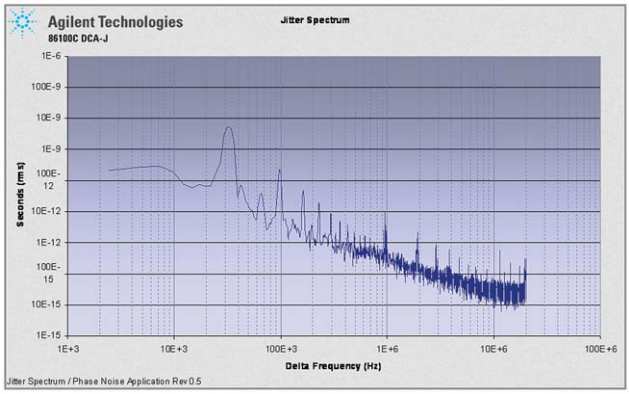


Figure 13. Jitter spectrum of the PCI Express reference clock

The jitter spectrum for the reference clock is very similar to that of the 2.5 Gb/s data signal. The SSC and its harmonics are the same. The tones at 1, 2, 3...MHz are also present. It is clear that the periodic jitter of the data signal is a direct result of the periodic jitter transferred from the reference clock. The spectral noise has a similar shape for both data and clock, except over the 3 to 20 MHz range. The differences may be due to the VCO of the transmitter PLL contributing some random jitter, and the bandwidth of the transmitter PLL altering the spectrum of the random jitter contributed by the reference clock.

This case study provides a clear example of the importance of being able to view the jitter spectrum on both clock and data signals. The jitter separation results of figure 10 indicate the magnitude of the jitter problem. But there is sparse information on where the jitter is coming from and how it might be reduced. On the other hand, the jitter spectrum provides a signature or fingerprint of the jitter. It is very clear that the virtually all of the jitter degradation from the reference clock has been transposed directly on to the data signal. Improving the jitter performance of the data signal could be performed by altering the jitter spectrum through a specific PLL design, or through going to the root source and improving the performance of the reference clock.

Using virtual PLL's to emulate system level performance

Some jitter analysis techniques take a system level approach and examine the jitter from the context of how it would appear after being manipulated by transfer functions created by PLL's and propagation delay. The 86100/86108A or 83496B system allows the signal under test to be processed by user defined PLL's (two PLL's, up to third order) and transport delay. The effective jitter can then be displayed as if it had actually passed through the defined system.

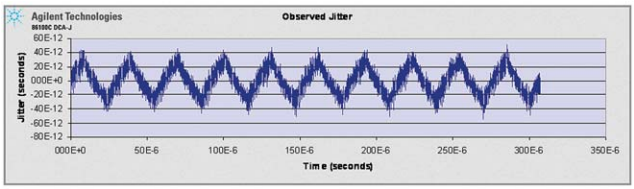


Figure 14. Jitter of a clock signal having passed through virtual PLL's and transport delay

Figure 14 shows the PCI Express reference clock jitter as a function of time as if it had been processed by two PLL's separated by a finite propagation delay. Once again, the SSC profile is observed, but is seen as the actual time deviation that would be observed by a receiver in the emulated system. The SSC is suppressed due to the tracking of the virtual PLL. Random jitter not tracked out by the virtual system is also observed.

To gauge the magnitude of the jitter, a vertical histogram can be constructed for the observed jitter plot of figure 14.

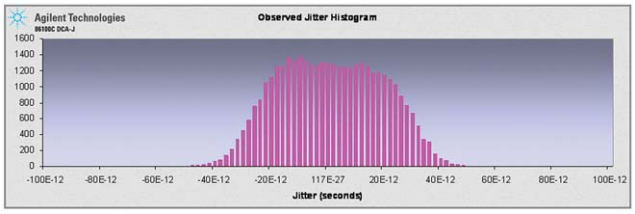


Figure 15. Histogram display of the observed jitter seen in figure 14

The jitter magnitude after the post processing is approximately 100 ps rms. The histogram shape is as expected. The ideal SSC histogram would be rectangular. The addition of a random jitter element results in Gaussian type tails in the distribution.

The clock (or data) can be examined further by observing the phase error and the input phase.

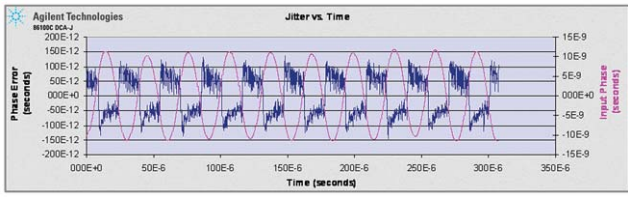


Figure 16. Input phase and phase error

The parabolic shape trace is the phase modulation seen at the input of the 86108A or 83496B phase detector. Note that since phase is the integral of frequency, the triangle shaped SSC frequency modulation function yields a parabolic shaped phase deviation. Viewing the input phase in the jitter domain provides an important trouble-shooting capability. If there are ever phase transients, for example when a PLL loses synchronization or exceeds its allowable phase range, the phase "glitch" can be observed directly in the input phase trace. The phase error trace (noisy 'square wave") is an indication of the actual signal that the 86100C/86108A or 83496B measurement system is observing.

Theory of Operation

The 83496B clock recovery module is commonly used to derive a clock signal from data streams. The clock recovery system of the 83496B is also used in the 86108A Precision Waveform Analyzer. The derived clock signal is then used as a timing reference or "trigger" for the 86100C oscilloscope to display waveforms. The clock extraction process is based on a phase locked loop design.

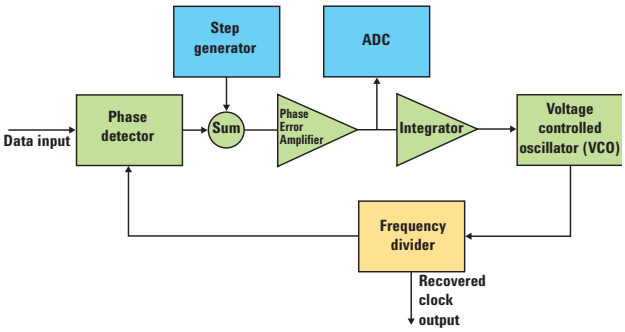


Figure 17. Block diagram of the 83496B

The output of the VCO is compared at the phase detector to the incoming signal (clock or data). If there is a phase/frequency difference between the VCO and the data, the phase detector produces an error voltage proportional to that difference. This then adjusts the VCO frequency so that it tracks or "locks" to the incoming signal.

Consider a clock or data signal that has phase noise/jitter. The frequency that the VCO will try to lock to is constantly changing. The error signal created will be constantly changing. The error signal will effectively be an analog signal representing the phase noise/jitter of the incoming data/clock. By placing an analog-to-digital converter (ADC) at the output of the phase detector, the error signal can be monitored. It is similar to having an oscilloscope probe at the phase detector output.

There are some important distinctions between the phase detector/ADC approach and the approach based on acquiring the actual data or clock waveform with a very fast oscilloscope and extracting jitter information through post processing. Observing jitter/phase noise requires extremely long record lengths when very fast real-time oscilloscopes are used. It takes a relatively long amount of time (and hence a long time record) to observe something that happens slowly. The phase detector approach is not subject to this problem, as it is observing the baseband jitter directly and not the high-speed waveform.
A much slower sample rate can be used to accurately observe the jitter. Also, the processing overhead/long measurement time associated with very long waveform records is not an issue with the phase detector approach. On the other hand, the ADC in the 83496B operates at 40 megasamples/s yielding a measurement bandwidth limited to 20 MHz and the ADC in the 86108A operates at over 50 MSa/s yielding a 25 MHz bandwidth.

The 83496B/86108A has an adjustable loop bandwidth that is user definable. Intuitively it would seem that the loop bandwidth should be set to the highest value possible in order to have the minimum impact on the observed error signal. However, a reduced loop bandwidth results in a larger error signal, and improved dynamic range for the measurement system. The optimum loop bandwidth is the smallest value that still allows the 83496B to phase lock to the signal.

The loop bandwidth of the 83496B/86108A will impact the frequency response of the system and alter the spectrum of the error signal. This can be corrected for if the loop response is known. The 83496B/86108A is capable of internally characterizing its loop response. This is performed automatically as part of the measurement procedure after the loop bandwidth has been configured in the setup process.

The main acquisition system of the 86100C/86108A is not used in the phase noise measurement. That is, there is no requirement to have the signal go into any of the main oscilloscope channels. All signal acquisition takes place within the 83496B/86108A clock recovery module. The PC running the analysis software will interface with the 86100C/86108A mainframe, but only as a means to communicate to the 83496B/86108A and extract the phase noise signal. Yet it is often extremely useful to take advantage of the ability of the system to observe the waveform being analyzed. Proper signal amplitudes, patterns, de-emphasis levels etc. can be easily verified using the oscilloscope capabilities of the 86100C.

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