High-Speed Digital Interconnect Modeling

Product Note 85240-1

Overview

With digital circuit designs pushing operating clock rates into the hundreds of Megahertz, designers are increasingly faced with a variety of problems caused by circuit characteristics that can be ignored at lower clock rates. Phenomena that are insignificant at lower frequencies can cause circuit failures at higher clock rates due to decreased noise margins.

This Product Note describes some of the major problems now faced by designers of high-frequency digital circuits, and shows how the HP Picosecond Interconnect Modeling Suite can be used to understand and solve them.

Common High-Frequency Design Problems

There are several major categories of design problems that must be solved by high-frequency digital circuit designers, such as:

- Transmission line delay
- Impedance mismatches
- Effects of active line drivers and receivers
- Transmission line coupling
- Ground bounce and ground loops
- Parasitic effects of connectors

Improperly designed high-speed digital circuits may suffer from any of these problems, and the symptoms (degraded signal waveforms, unexpected signal impulses, lower noise margins, and circuits that simply do not work) may not give any immediately useful clues as to the cause of the problem. These circuits can often only be debugged by designers with experience in high-frequency signal effects, using the proper simulation models and tools hand-in-hand with high-frequency test equipment.

The HP Picosecond Interconnect Modeling Suite allows designers of high-speed digital circuits to closely examine the effects of high-frequency phenomena on critical sections of digital circuit layouts. It helps in the creation of design rules, models, and overall architectures. It is not designed to be a replacement for SPICE or other digital design software. Rather, it is designed to supplement them, and to add component models and analysis capabilities that do not exist elsewhere.

To simulate high-frequency circuits, special-purpose simulators with high-frequency models are needed. Older, low-frequency circuit simulators do not take into account the necessary high-frequency circuit phenomena. For instance, a complete model for a transmission line must include impedance, delay time, and coupling to other nearby transmission lines. Low-speed models might only include the delay and the loss.

The HP Picosecond Interconnect Modeling Suite makes available two different types of simulators for high-speed circuits, plus an electromagnetic simulation engine called HP Momentum that is used to simulate arbitrary circuit geometries. Interconnect networks are specified in a schematic format, with a simple layout generator available to help visualize the geometry and to move the network into HP Momentum. Finally, a SPICE model generator is used which makes it possible to transfer the results of specialized high-frequency analyses into SPICE. Together, these tools allow designers to create models for specific circuit layouts and transfer them to SPICE or other tools for complete system analyses.

Simulation Technology

To properly apply the tools in the HP Picosecond Interconnect Modeling Suite, it is important to understand the simulation technology that the suite makes available. This section presents a brief overview of the HP Picosecond Interconnect Modeling Suite's available simulation technology. The Appendix to this Product Note includes more in-depth information on the simulators, which should be understood by designers using them.

AC Analysis

AC analysis, which is a part of the HP Picosecond Interconnect Modeling Suite, uses frequency-domain simulation techniques combined with Fourier series analysis to simulate the response of linear circuits to digital waveforms. AC analysis is by far the fastest simulation type, and accurately models signal crosstalk, propagation delays and loss on transmission line structures and lumped-element circuit components. However, AC analysis cannot simulate the effects of nonlinear circuit components.

As a rule of thumb, it is generally best (fastest) to use AC analysis whenever possible. It should be possible to model most interconnect structures – IC packages, traces on PCBs or ICs, connectors, vias, etc. If nonlinear devices must be included in the simulation, use HP Impulse or a SPICE simulator. If the physical layout of a circuit makes it impossible to model with the HP Picosecond Interconnect Modeling Suite's built-in simulator components, then other simulators such as HP Momentum must be used instead.

HP Impulse

HP Impulse, which is also included with the HP Picosecond Interconnect Modeling Suite, is a time-domain simulator tool that, like SPICE, uses finite-difference methods and discrete time steps to analyze nonlinear circuits. Unlike SPICE, HP Impulse can use a technique called dynamic convolution to include transmission lines and frequency-domain device models (S-parameters) in its simulations. While HP Impulse simulations take longer than AC analysis, HP Impulse must be used when active nonlinear devices like line drivers and receivers are to be included in the simulation.

HP Momentum

HP Momentum is an option to the HP Picosecond Interconnect Modeling Suite that adds the ability to find the response of arbitrary circuit layouts. Using the Method of Moments technique, HP Momentum can handle 2-dimensional layouts with an unlimited number of layers and vias. Although this type of simulation can take a relatively long time, it is the only way to accurately model layout geometries that are not included as built-in models for AC analysis. However, the results of HP Momentum simulations can be included in both AC analysis and HP Impulse simulations, allowing designers to use HP Momentum for small parts of circuits and use the faster simulators for larger, more complete simulations.

SPICE Model Generation

Although HP Impulse is a capable time-domain simulation tool, other SPICE-derivative simulators are heavily used in the digital design world. To support their use, the HP Picosecond Interconnect Modeling Suite includes a SPICE model generator. The results of HP Picosecond Interconnect Modeling Suite analyses can be translated into SPICE models and output as netlist files. A variety of third-party simulator netlist formats are supported.

Examples of Common High-Speed Digital Problems

The use of the HP Picosecond Interconnect Modeling Suite can best be illustrated through a series of simple examples. This section shows results for coupling, delay times, and impedance matching.

Finding the Impedance of a Given Line Width

Transmission line impedances can easily be calculated using any number of simple computer programs or textbook equations. These techniques are accurate and useful, but they have two drawbacks: they only account for a single frequency, and they usually assume that the transmission line is isolated from any external coupled signals. The HP Picosecond Interconnect Modeling Suite can be used to perform these simple impedance calculations, but it can also be used to extend impedance calculations beyond these boundaries.

The *effective* impedance of a transmission line is a function of frequency, and can change significantly as frequencies get higher. Most commonly, this is the result of a dielectric constant that changes as a function of frequency. Since a digital signal is made up of many harmonic components, this changing impedance can have a significant effect on the signal.

Another factor that can affect impedance calculations is the presence of nearby transmission lines. If the nearby lines are close enough to cause significant coupling, then they are close enough to affect the electric field distribution and hence the line impedance.

Often, the goal of making circuits as small as possible dictates that all transmission lines be as thin as the manufacturing process allows. For some types of digital logic e.g., ECL, these lines must then be terminated in the proper impedance. To achieve the best noise margins, it is important to calculate this impedance accurately.

The HP Picosecond Interconnect Modeling Suite includes a prepackaged impedance simulation that calculates the best impedance for a given transmission line, including all coupling effects and any effects of signal harmonics. This can be used to examine the effects that overly-simple calculations have on terminating impedances. Figure 1 shows a simple impedance calculation using this prepackaged simulation component.

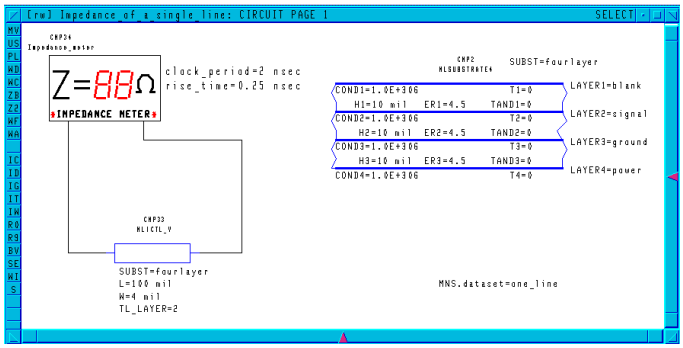


Figure 1. *Simulation setup for calculating the impedance of a single transmission line. For the geometry specified here, the line impedance is calculated as 87Ω (not shown in this figure).*

When simulated, the simple circuit in Figure 1 yields an answer of 87Ω. This can be contrasted with the case on an 8-line data bus, as shown in Figure 2.

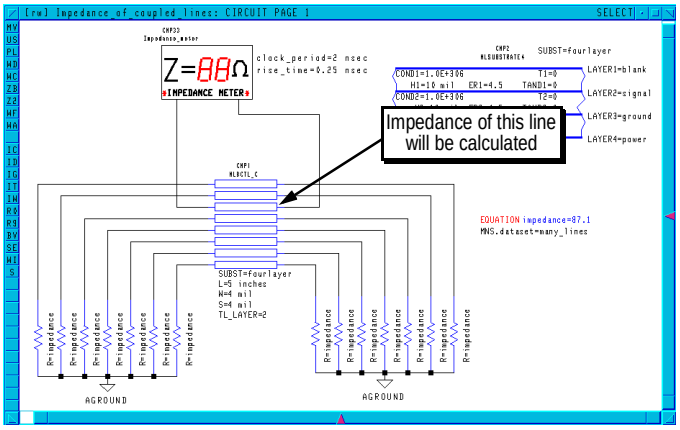


Figure 2. *Simulation setup for calculating the impedance of the third line of an 8-line data bus. The other seven lines are terminated in 87Ω, which is the calculated impedance of a single line. This simulation yields a result of 72Ω.*

In Figure 2, all lines but one of an 8-line-wide bus are terminated in 87Ω, which is the impedance calculated in Figure 1. Then, the impedance of the third line is calculated. This calculation finds the impedance that gives the smallest signal reflection on that line, including all coupling effects. Interestingly, the effective impedance of this line is only 72Ω, or 20% less than the impedance of an identical but isolated line.

The effects of coupling on impedance calculations are also evident on the other lines, but in varying amounts depending on the amount of coupling present. For instance, if the simulation in Figure 2 is repeated for one of the outer lines instead of the third line, the calculated impedance is 79Ω, a result which is expected because there are fewer coupling effects on the outer lines.

It is also important to note that coupling is strongly dependent on the length of the transmission lines. The example in Figure 2 is for 5-inch-long coupled lines. If this length is reduced to 1 inch, the calculated impedance of the third line rises to 74.5Ω. Obviously, if the lines are very short the impedance will approach the value for the isolated line (87Ω).

Finding the Correct Line Width for a Given Impedance

The HP Picosecond Interconnect Modeling Suite can also be used to design traces that compensate for coupling and other high-frequency effects. Figure 3 illustrates this case. In this figure, the dielectric constant of the substrate is defined to be a function of frequency. The prepackaged simulation component varies the width of the transmission lines to minimize the total signal mismatch over all frequencies. Since most of the energy in a digital signal is at or near the clock frequency, this simulation uses a weighted average so that the lower frequencies have more of an effect on the optimization than the higher frequencies. The transmission line width found by this optimization yields the lowest signal reflections for this geometry, even in the presence of coupled lines and a frequency-dependent dielectric constant

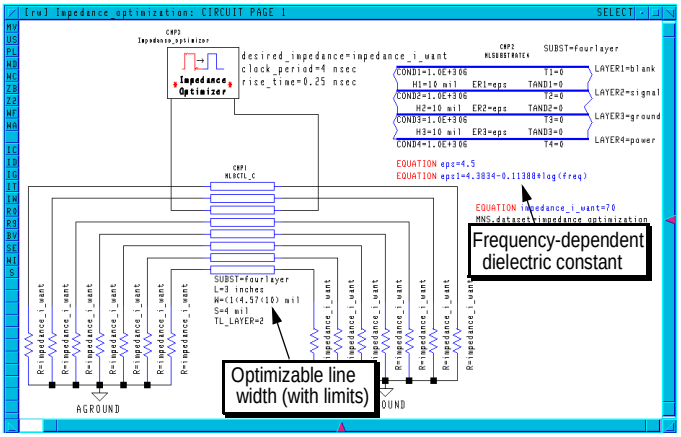


Figure 3. *HP Picosecond Interconnect Modeling Suite optimization setup to find the correct transmission line width for a 70Ω line in the presence of coupled lines and a frequency-dependent dielectric constant.*

Again, the results obtained from the simulation in Figure 3 depend on the length and number of coupled transmission lines. For the case shown here, a 70Ω line is calculated to be 4.6 mils wide. Contrast this value to the width of an isolated 70Ω line on the same substrate, which is 7.5 mils.

Creating SPICE models

To create a SPICE model in the HP Picosecond Interconnect Modeling Suite, an S-parameter analysis must be performed. An S-parameter analysis is functionally similar to an AC analysis in that it is a linear, small-signal analysis. However, an S-parameter analysis requires a different schematic setup than an AC analysis.

Figure 4 shows a small part of an IC package that has been entered into the HP Picosecond Interconnect Modeling Suite. An S-parameter source element is attached to each of the eight signal ports of the circuit. The figure also shows the S-parameter simulation setup. In this case, the simulator will calculate 1001 S-parameters for the circuit from 10 MHz to 11 GHz.

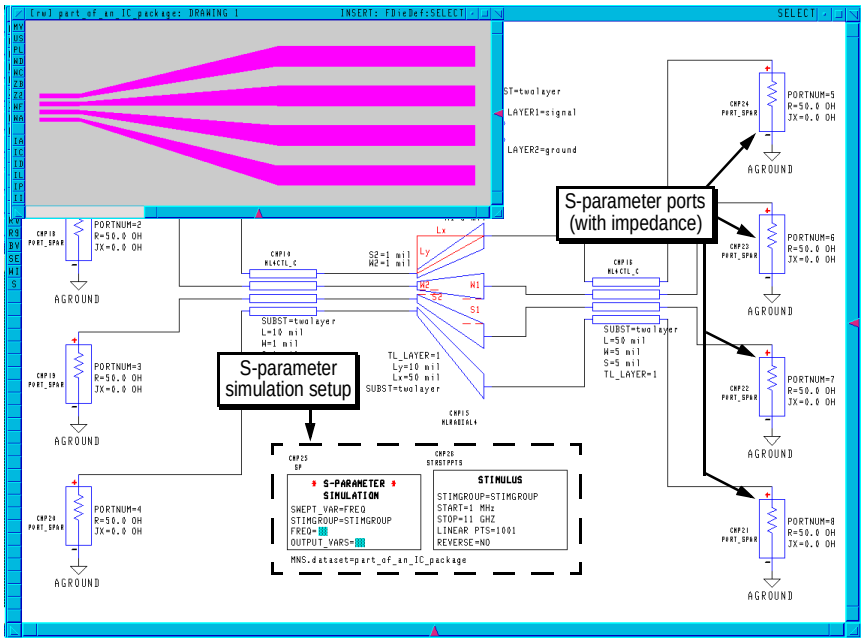
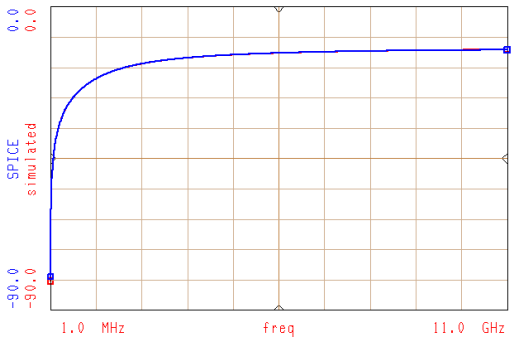


Figure 4. *A part of an IC package setup for S-parameter analysis. The results of the S-parameter analysis can be used to create a SPICE model for this circuit. The smaller window at the upper left shows the layout of this circuit.*

The S-parameter data that is generated by the simulation in Figure 4 is used by the SPICE model generator. The SPICE model generator's options are covered in more detail in the Appendix. For this example, a ladder network model was created. The SPICE model generator was instructed to match the simulated S-parameters well enough to handle a digital signal with a 1 ns risetime. In this case, the SPICE model generator was able to do considerably better than that. The SPICE netlist, and a plot of both the SPICE model results and the original S-parameter results, are shown in Figure 5.

Figure 5. *Results of simulating the circuit of Figure 4 plotted on top of a simulation of the SPICE model parameters. The data shown is for the crosstalk between two adjacent lines. Because the two plotted traces lie almost directly on top of one another, there appears to be only one line on the plot. The actual SPICE netlist is shown on the right.*




```
SPICE 2G6 netlist generated from [S] parameters
.subckt IC 1 2 3 4 5 6 7 8
* L in nH, C in pF
L1 1 9 1.79N
R1 9 13 0.0141919
C1 13 0 0.0225846P
L2 2 10 1.16466N
R2 10 14 0.0143795
C2 14 0 0.0131744P
L3 3 11 1.16421N
R3 11 15 0.014314
C3 15 0 0.0131845P
L4 4 12 1.17785N
R4 12 16 0.0140278
C4 16 0 0.0226284P
K1 L1 L2 0.76478N
C5 13 14 0.0342071P
K2 L1 L3 0.591963N
C6 13 15 0.00653479P
K3 L1 L4 0.48817N
C7 13 16 0.00412892P
K4 L2 L3 0.758814N
C8 14 15 0.0313088P
K5 L2 L4 0.59173N
C9 14 16 0.00653523P
K6 L3 L4 0.764251N
C10 15 16 0.034258P
L5 13 17 1.179N
R5 17 5 0.0141919
C11 5 0 0.0225846P
L6 14 18 1.16466N
R6 18 6 0.0143795
C12 6 0 0.0131744P
L7 15 19 1.16421N
R7 19 7 0.014314
C13 7 0 0.0131845P
L8 16 20 1.17785N
R8 20 8 0.0140278
C14 8 0 0.0226284P
K7 L5 L6 0.76478N
C15 5 6 0.0342071P
K8 L5 L7 0.591963N
C16 5 7 0.00653479P
K9 L5 L8 0.48817N
C17 5 8 0.00412892P
K10 L6 L7 0.758814N
C18 6 7 0.0313088P
K11 L6 L8 0.59173N
C19 6 8 0.00653523P
K12 L7 L8 0.764251N
C20 7 8 0.034258P
* end of the sub circuit
.ENDS
```

Transmission Line Crosstalk Using AC Analysis

Parallel transmission lines always couple energy into each other, causing the signal on each line to interfere with the signal on all other nearby lines. This interference is a complicated function of the substrate material, the substrate thickness, the transmission line widths, the distance between the transmission lines, the clock frequency and risetime, and the length of the lines. The HP Picosecond Interconnect Modeling Suite is particularly good at modeling signal coupling between transmission lines.

One way to examine the effects of transmission line coupling is to drive a single line with a pulse train, and examine the pulse train as it exits the other end of the line. The signal will be coupled into any parallel transmission lines and can be observed at both ends of them. At high frequencies, clock signals can be almost completely coupled from one line into another if lines become too long.

Figure 6 shows a simulation setup that can be used to examine the effects of coupling on clock signals. Eight parallel transmission lines on the second layer of a 4-layer structure, are connected to a simulation component. The clock period is 2 ns (500 MHz) with a risetime of 0.25 ns. The traces are 3 inches long, which is electrically a long line to a 500 MHz signal.

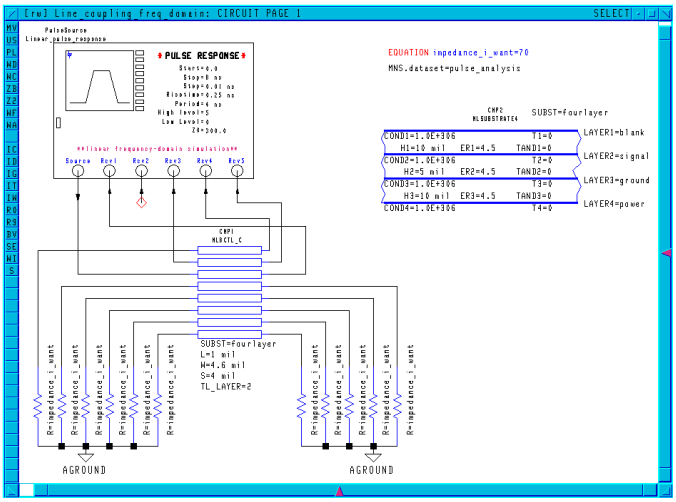


Figure 6. *A simulation setup for eight coupled lines using linear AC analysis.*

The transmission lines in Figure 6 are all terminated in 70Ω, and the line width has been previously optimized to ensure that the lines have a characteristic impedance of about 70Ω using the impedance simulations described previously. This minimizes reflections, but does not eliminate them entirely because of coupling effects. Note that not every transmission line is examined in this setup. One line is excited with the clock signal, and its output is examined; both ends of the nearest neighbor are examined; and one output of the next-nearest neighbor is examined. (In general, coupling from lines farther away may be significant, and designers should examine their own circuit layouts carefully to be certain that all significant coupling effects are being examined.)

Linear AC analysis is used here for speed. Since this method yields only steady-state solutions, the start and stop times are valuable only for plotting. The clock signal is assumed have a constant period for all time, and there is no delay time or startup transient. (This is contrasted with traditional time-domain analysis below.)

Figure 7 shows the results of the simulation setup shown in Figure 6. The top trace, labeled *SourcePort*, shows the voltage waveform at the source of the clock signal. It is slightly distorted because of reflections and coupled signals from the other transmission lines, but the original waveform is intact — it rises from 0 to 5 volts, and settles there. Immediately below it, in the trace labeled *Rcvport1*, is the output signal of the driven line.

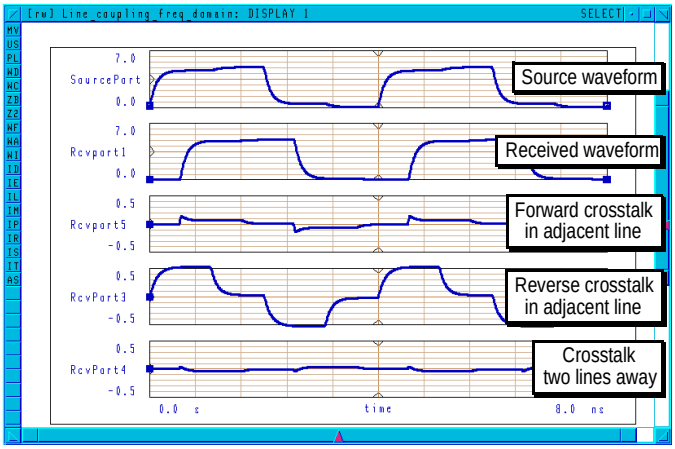


Figure 7. *Results of the simulation setup in Figure 6. The driving clock signal is on the top trace, with the output of the driven line on the second trace. The other traces are coupled signals. Note the change of vertical scale on the three lower traces.*

The following three traces show the outputs of the coupled lines. A good deal of the clock signal is coupled into the closest adjacent transmission line (*RcvPort3* on the plot). This coupling both degrades the original clock signal and lowers the noise margin on the adjacent lines.

The easiest way to eliminate coupling problems is to move the transmission lines farther apart. If that alone does not succeed, then adding grounded "guard" traces between each data line may be sufficient. Unfortunately, these techniques are not always viable options because of real estate limitations, especially for IC designs. Other techniques that can be used to reduce coupling include:

• Move the lines to another layer. The results of placing the transmission lines on the top layer, rather than on a buried layer, are shown in Figure 8. Because the substrate height changes, this move changes the impedance of the lines, and the circuit in Figure 6 has not been adjusted for this. Still, it is clear that signal coupling is dramatically increased on the top layer when compared to buried layers.

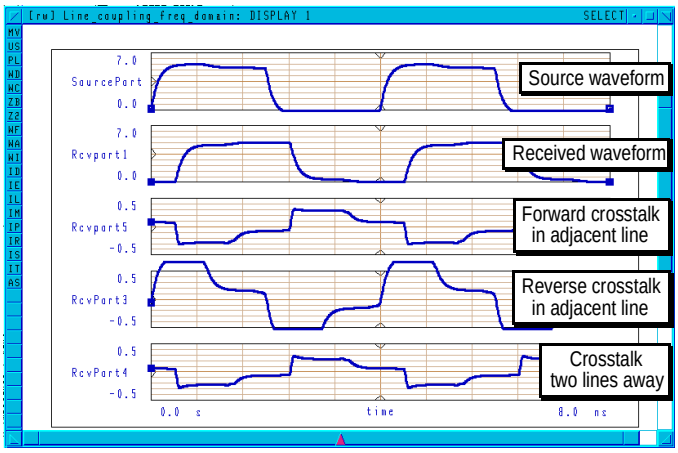


Figure 8. *Results of the simulation shown in Figure 6, only with all transmission lines moved to the top of the substrate. Note the dramatically increased signal coupling on the adjacent lines.*

• Shorten the trace length. The traces in Figure 6 are 3 inches long, which is electrically very long at 500 MHz. If that length can be shortened, coupling should be reduced. Figure 9 shows the results of the same geometry but with the trace length reduced from 3 inches to 100 mils. The coupling is obviously greatly reduced.

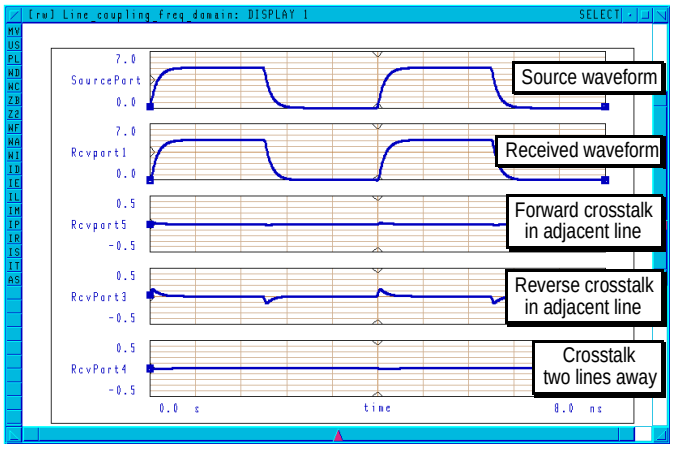


Figure 9. *Transmission line coupling from the circuit of Figure 6, but for 1-mil-long traces.*

• Make the layers thinner. If manufacturing tolerances permit, thinner layers can be a significant advantage. Figure 10 shows the results of the trace geometry from Figure 6, but with a substrate height that is half as thick. To maintain the same line impedance, the trace widths were also narrowed. The spacing between traces was maintained at 4 mils. The result of this changed geometry is not only less crosstalk but a smaller circuit layout.

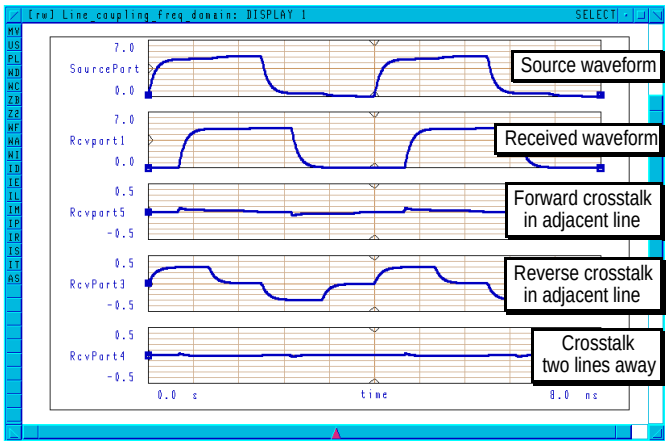


Figure 10. *Results of changing the trace geometry in Figure 6 so that thinner board layers and thinner lines are used, resulting in significantly less crosstalk.*

Transmission Line Crosstalk using HP Impulse Time-Domain Analysis

Transmission line coupling can also be examined using time-domain simulations with tools like HP Impulse. However, there are some differences in the obtained results. Since time-domain simulation techniques includes all transient phenomena, the simulation must be run for a time long enough for the input signal to reach the opposite end of the transmission line and for all reflections after that to die. Further, if there are any significant reflected signals caused by impedance mismatches, the simulation must be run long enough for all multiple reflections to die. AC analysis, which only yields steady-state results, automatically includes all reflections regardless of the time period specified for the simulation. Figure 11 shows the results of a time-domain simulation, using HP Impulse, of the transmission line structure from Figure 6, but with 10-inch trace lengths.

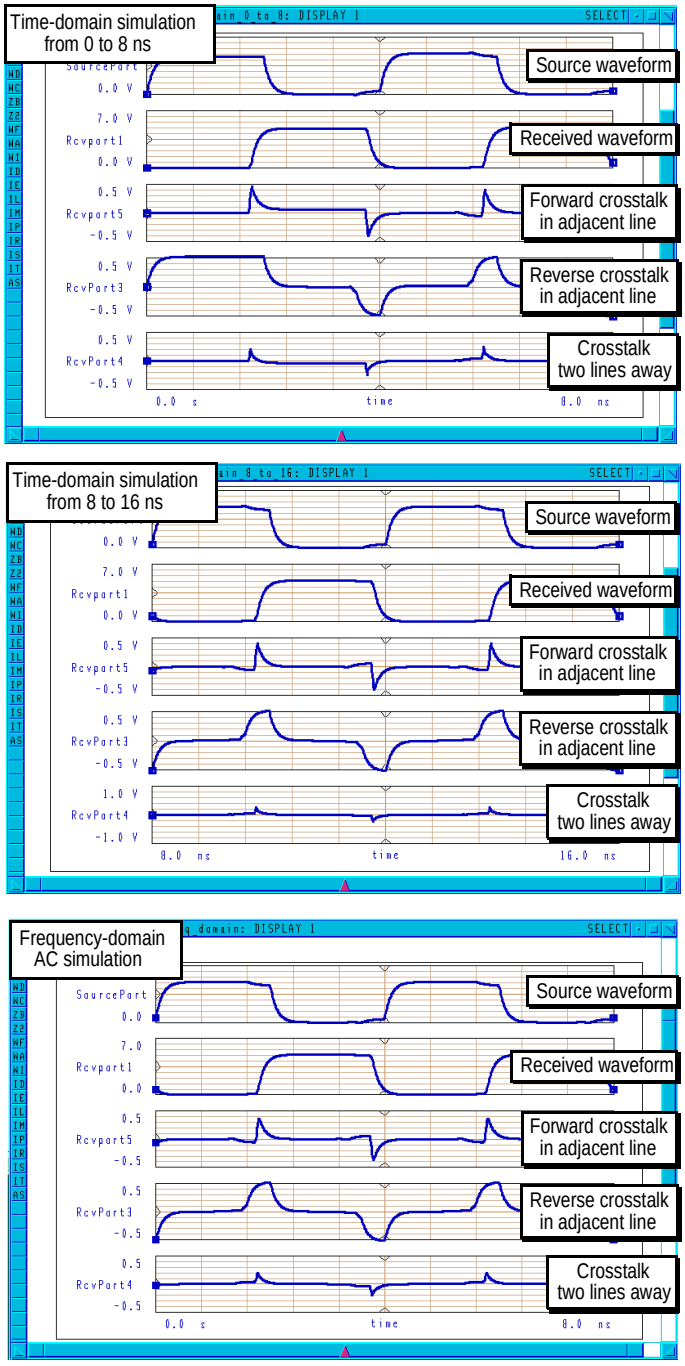


Figure 11. *HP Impulse simulation of the coupled lines in Figure 6, only with 10-inch trace lengths. The top plot shows the results of simulating from 0 to 8 ns, which is before all coupled and reflected signals have reached a steady state. The middle trace shows a later time period, after all transient effects have passed. This can be compared with the identical results from AC simulation, which took much less time, in the bottom plot.*

The results of Figure 11 show no numerical (accuracy) advantage to using nonlinear time-domain simulations for *passive* coupled-line structures. In fact, HP Impulse takes much longer to complete the simulation in Figure 11 than AC analysis. The advantage of using time-domain simulation for analyzing transmission line coupling (or any other circuit effect, for that matter) is that active circuit elements, such as line drivers and receivers, can be included in the simulation. Depending on signal levels, impedance mismatches, and line coupling, the effects of nonlinear devices can be crucial to accurate circuit simulations. The best technique, then, is to use linear analyses whenever possible for speed, and use nonlinear time-domain analyses only when necessary.

Figure 12 shows a setup in the HP Picosecond Interconnect Modeling Suite that is similar to Figure 6 but with IBIS models used as the terminating elements for the transmission lines. (In this example, the IBIS models correspond to some of the IRQ inputs on an Intel 82374 PCI-EISA Bridge being driven at 50 MHz. The transmission lines are 5 inches long.)

The nonlinear IBIS terminations cause part of the signal on each line to be reflected, even though the transmission lines are nominally matched to the correct impedance. Therefore, the transmitted and coupled signals are distorted in distinctly different ways.

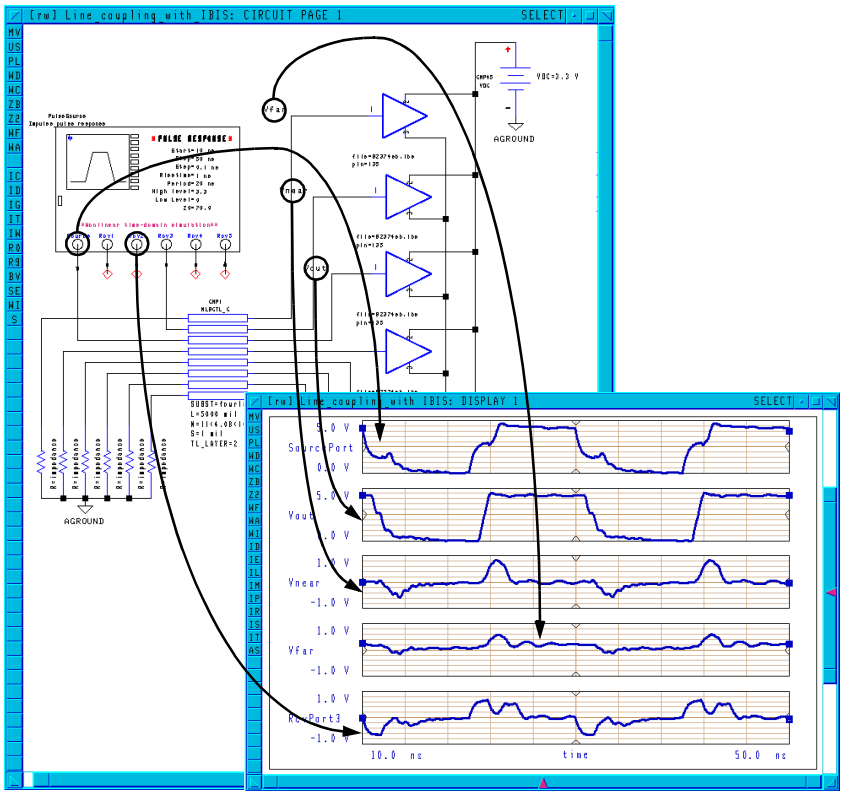


Figure 12. *Simulation setup and results for coupled transmission lines using nonlinear IBIS models as terminations. Note that the pre-packaged simulation component is used as a source for convenience, while most of the output data is captured independently.*

IBIS models

IBIS (I/O Buffer Information Specification) is a public-domain, industry-standard specification modeling input and outputs of digital circuits. Vendors may create IBIS models for their parts and distribute them for use in any IBIS-compatible simulator. Previously, these parts had to be modeled using equivalent-circuit SPICE models. Using IBIS models, the nonlinear effects of integrated circuit I/O buffers can be modeled faster and more precisely, using vendor-supported information.

Many IBIS models are included with the HP Picosecond Interconnect Modeling Suite, but the IBIS model library is continually updated and expanded. The most up-to-date IBIS models, as well as more information about IBIS models themselves, can be obtained from the VHDL International Users Forum Internet server *vhdl.org* using ftp (login as *anonymous*) or through the use of a World-Wide Web browser accessing using the URL *gopher://gopher.vhdl.org:70/11/pub/ibis/models*. The WWW home page for the VHDL International Users Forum is at *http://www.vhdl.org*.

Impedance Mismatches using AC TDR Analysis

If transmission lines are not terminated in the correct impedance, some of the signal on the line will be reflected when it reaches the receiver. Traveling backwards down the transmission line, the reflected signal will reach the source and be partially reflected again. The reflected signal will eventually become attenuated to insignificant levels, but it may take as long as several clock cycles to do so if the clock frequency is high and the transmission line length is long. TDR (time-domain reflectometry) analysis can be used to examine the effects of multiply-reflected signals.

With digital signals, multiple reflections can exist simultaneously on a single transmission line. Compounded with these reflected signals are coupled signals. The coupled signals can also be reflected, and the reflections can themselves be coupled back into a different transmission line. Obviously, the total effect of many reflected and coupled signals is very complicated and is often misdiagnosed as capacitive “ringing” from line drivers and receivers or some other parasitic circuit problem. Figure 13 shows one such result. (Note that Figure 13 shows results for 70Ω lines terminated in 300Ω impedances. It is nearly impossible to achieve a purely resistive 300Ω resistance at high frequencies, but this exaggerated result is used here to more clearly display the combined effects of coupling and reflections.)

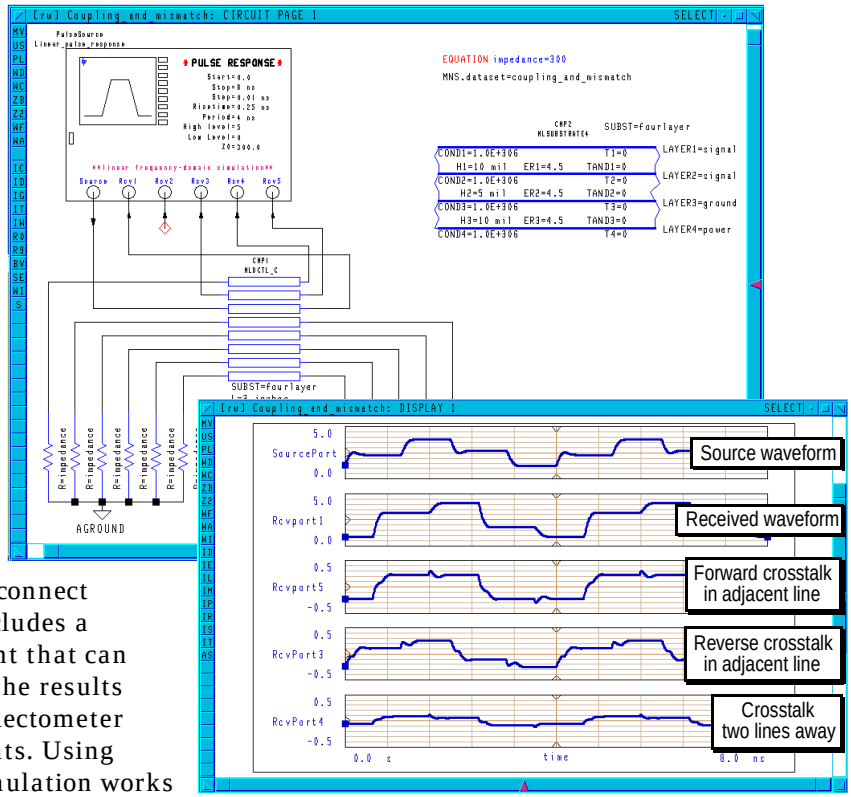


Figure 13. *AC simulation setup similar to Figure 6, only with a significant impedance mismatch (70Ω transmission lines with 300Ω loads). The results show the combined effects of reflected and coupled signals.*

One good way to test for impedance mismatches is to use a time-domain reflectometer (TDR). The HP Picosecond Interconnect Modeling System includes a simulation component that can be used to simulate the results of a time-domain reflectometer on passive components. Using AC analysis, this simulation works identically to the clock waveform simulation described above but with much a longer period. (There is a different TDR simulation component that uses HP Impulse rather than AC analysis for use with nonlinear circuits; see the next section for an example of this.)

Figure 14 shows the simulation setup, using the prepackaged TDR simulation component, of a simple bus structure with an unusual geometry. In this figure, the vertical set of traces have a different line width and spacing than the horizontal traces, resulting in an impedance mismatch.

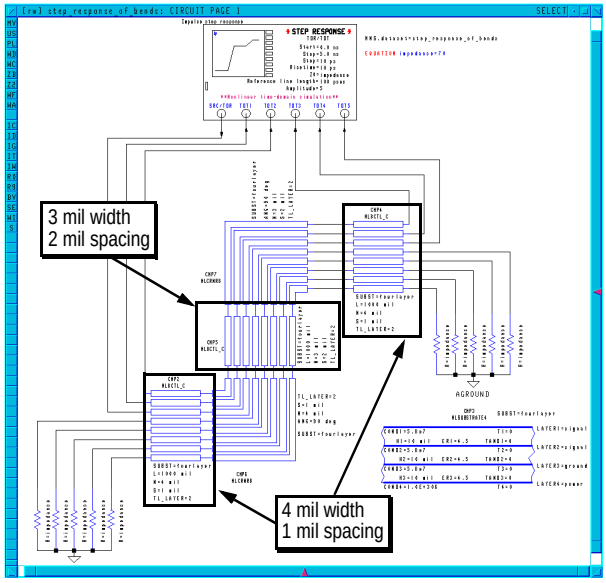


Figure 14. *Transmission lines of different widths set up for a TDR simulation in the HP Picosecond Interconnect Modeling Suite.*

Figure 15 shows the results of this analysis and reveals some of the advantages of using TDR analyses on transmission line structures. At each discontinuity, the plotted TDR data shifts to a different level. The location of each discontinuity can be directly calculated from the time the jump takes place; the length of the discontinuity can be calculated from the length of the step; and the impedance of the discontinuity can be calculated from the height of the step. A reference line (a perfect transmission line of a known impedance and length) is included in the TDR measurement to mark a known impedance level.

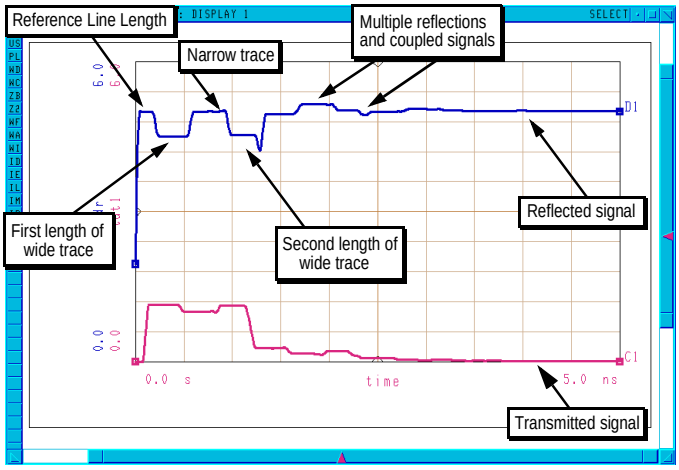


Figure 15. *Results of the TDR analysis in Figure 14.*

Impedance Mismatches Using HP Impulse Time-Domain TDR Analysis

As with the clock waveforms discussed previously, it is often necessary to simulate nonlinear circuits with TDR analysis. For this purpose, the HP Impulse simulator is used.

Figure 16 shows the simulation component that performs TDR analyses using HP Impulse. This simulation component is identical to the AC analysis component in every way except the type of simulation that it uses, and is not discussed further here.

Simulating Power and Ground Planes

In the HP Picosecond Interconnect Modeling Suite's transmission-line model library, the components that are used to define multi-layer PC board or IC substrates and packages allow layers to be defined as ground or power planes. Layers defined in this way are considered to be *ideal* grounds or *ideal* sources of power, with no ground-bounce, coupled signals, or other undesired effects. Characterization of these effects is critical to the success of any high-speed digital circuit. Using the HP Picosecond Interconnect Modeling Suite, non-ideal signal and ground lines can be modeled by simply treating them as signal traces.

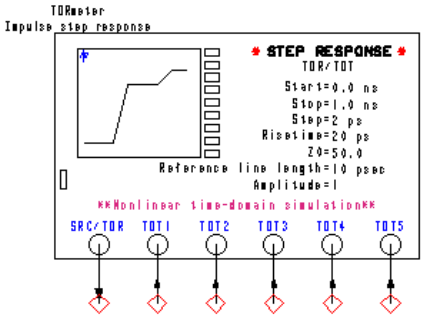


Figure 16. *Simulation control components for TDR simulation using HP Impulse for nonlinear analysis.*

Figure 17 shows the schematic of a simple (in fact, naive) bus structure that distributes signal and ground via traces that are identical to the signal traces. In this setup, the signal and ground lines are the two outer traces in the bus structure, and the other six lines are signals. All of the signal lines are terminated with IBIS models at their outputs. Two of the signal lines are driven simultaneously with a clock signal; the other four signal lines are terminated with 1 MΩ resistors. The substrate component, which defines two layers, specifies that both layers are used for signals (as opposed to ground or power planes).

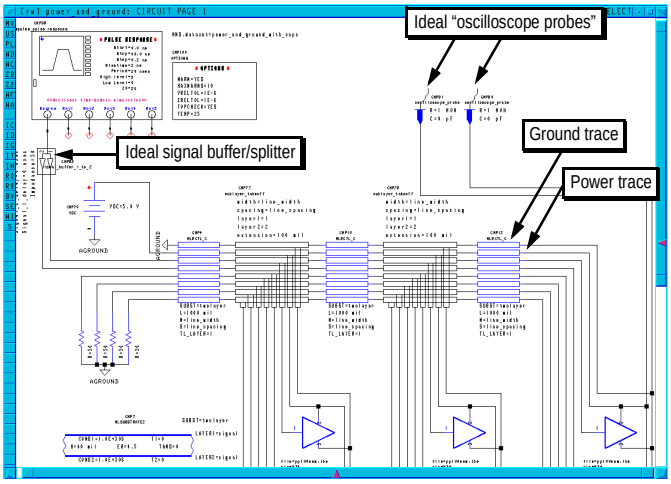


Figure 17. *Simulation setup used to examine power and ground coupling effects in a simple bus structure. The details of the sublayer crossover, including the necessary vias, are "wrapped" into a subcircuit and given a custom symbol.*

Note that the simulation setup in Figure 17 uses ideal oscilloscope probe components rather than the inputs of the simulation source component. In this experiment, the source impedance is small (50Ω), while the probe impedance is high (1 MΩ). Because the impedance of the source component's inputs are equal to the source's output impedance, it is easier to use external probe components for this circuit. The capacitance of the oscilloscope probe components is set to zero, which avoids any signal distortion but does not quite duplicate the results that would be seen with a real oscilloscope.

Figure 18 shows the simulated power and ground waveforms of this circuit as they appear at the oscilloscope probes. The clock frequency, 50 MHz, is clearly much too high for use with this simple power distribution scheme.

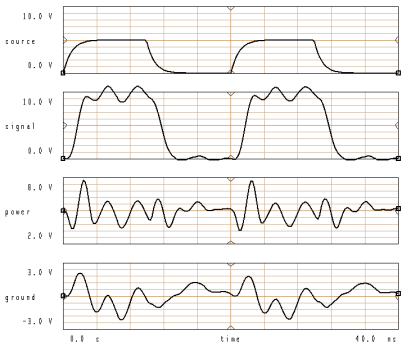


Figure 18. *Simulated results for the circuit of Figure 17. The top trace shows the source (clock) waveform. The second trace shows the signal waveform at the end of the signal path; its amplitude is doubled because of the high-impedance IBIS termination. The third trace show the ripple and ringing at the end of the power line, with voltage spikes of up to 3V present. The bottom trace shows the ground line, with voltage spikes of about 2V.*

The "classical" solution to the problem illustrated in Figure 18 is to periodically insert capacitors from the power line to the ground line. At very high clock frequencies, this may or may not be a successful approach. Figure 19 shows the response of this circuit with large (1 μμF) capacitors inserted at one inch intervals. Here, the noise in the power and ground planes is identical, and the ripples in the signal are reduced. Common-mode interference of this type can sometimes be accepted in digital circuits. However, this particular circuit's power and ground paths are identical. This is rarely the case in practice. To properly examine power and ground problems, a circuit board's exact layout is needed.

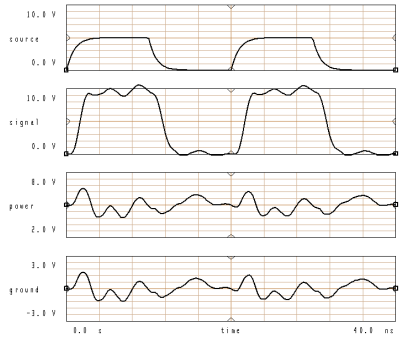


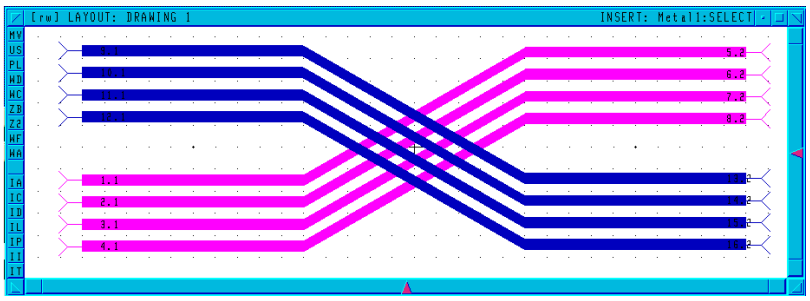
Figure 19. *Results from the circuit in Figure 17, only with 1 μF capacitors inserted at 1-inch intervals along the bus. Note that the noise in the signal is diminished, and the power and ground noise is now common-mode.*

Using HP Momentum

The HP Picosecond Interconnect Modeling Suite's component library includes transmission line models for most common circuit layout geometries, including Manhattan and non-Manhattan layouts. However, because an infinite number of possible layout geometries can be created, an all-inclusive library is impossible to create and would certainly fill up your hard disk. HP Momentum is an electromagnetic simulation tool that can be used to fill these gaps.

Figure 20 shows a layout window from the HP Picosecond Interconnect Modeling Suite. This simple structure shows two 4-line busses crossing on different layers at a 60-degree angle. HP Momentum can be used to generate a model of this structure.

Figure 20. *A layout window from the HP Picosecond Interconnect Modeling Suite. This simple two-layer structure was analyzed by HP Momentum. The traces are embedded in a PC-board material (ε_r=4.5). The traces are vertically separated by 10 mils, with 5 mils of the substrate material covering each side of the board. A ground plane (not shown here) is 500 mils below the traces, simulating a chassis ground under the PC board. The total horizontal length of this structure is 300 mils. The Y-shaped components at the ends of the traces define the location of signal ports for HP Momentum. All of the ports on each end are "grouped" as sets of coupled ports.*



Given the layout shown in Figure 20 and the necessary information about the PC board (dielectric constant, thickness of all layers, etc.), HP Momentum calculates the S-parameters of the structure. The S-parameter data can be used directly in the HP Picosecond Interconnect Modeling Suite, or it can be used to generate a SPICE model.

In the HP Picosecond Interconnect Modeling Suite, HP Momentum results are saved as a "dataset." The S-parameter dataset can then be used in a higher-level simulation, as shown in Figures 21 and 22.

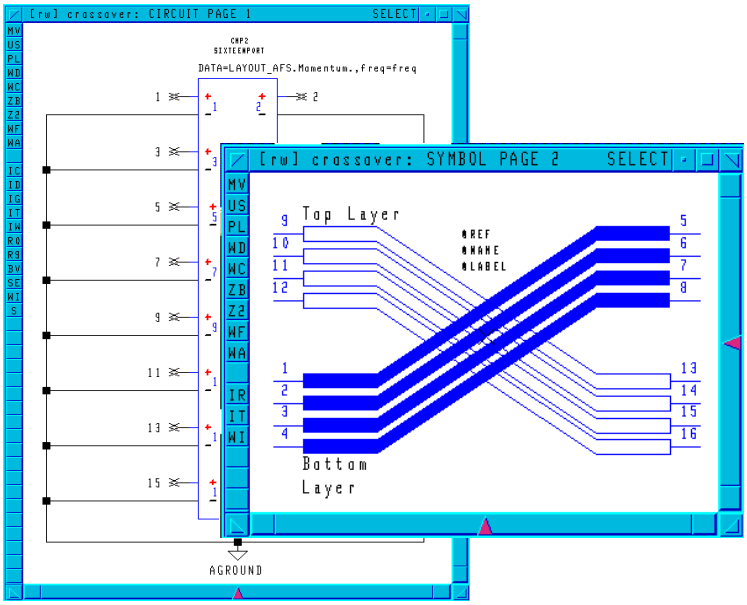


Figure 21. *HP Momentum S-parameter results can be used in higher-level simulations by using S-parameter data components, which simply read pre-computed S-parameters from a dataset. The generic S-parameter data component (left window) is large and unattractive, but can be easily "wrapped" into a subcircuit and given a custom symbol (right window).*

Creating a SPICE Model from HP Momentum Results

To use the HP Momentum results from Figure 22 in another simulator, a SPICE model can be generated. The steps involved in creating SPICE models from HP Momentum simulations are the same as from S-parameter circuit simulations, even though a different simulator was used to create the S-parameters themselves.

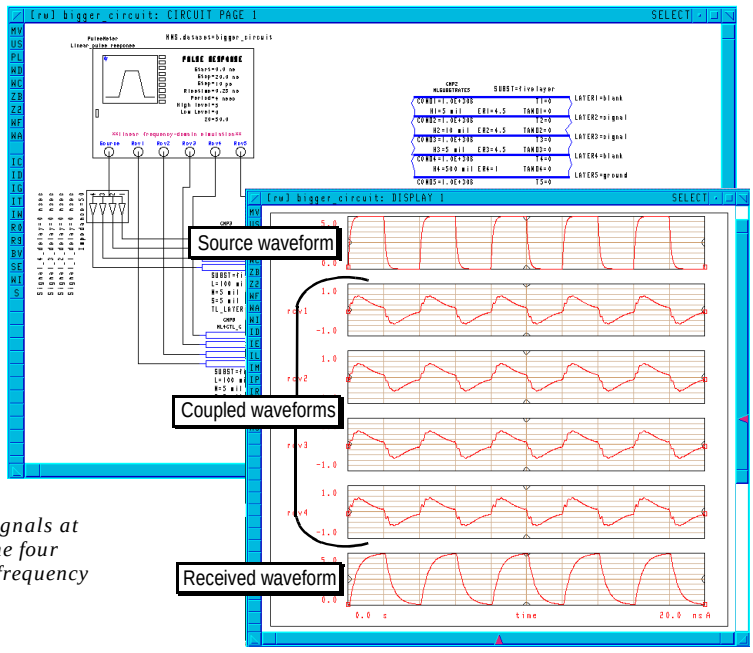
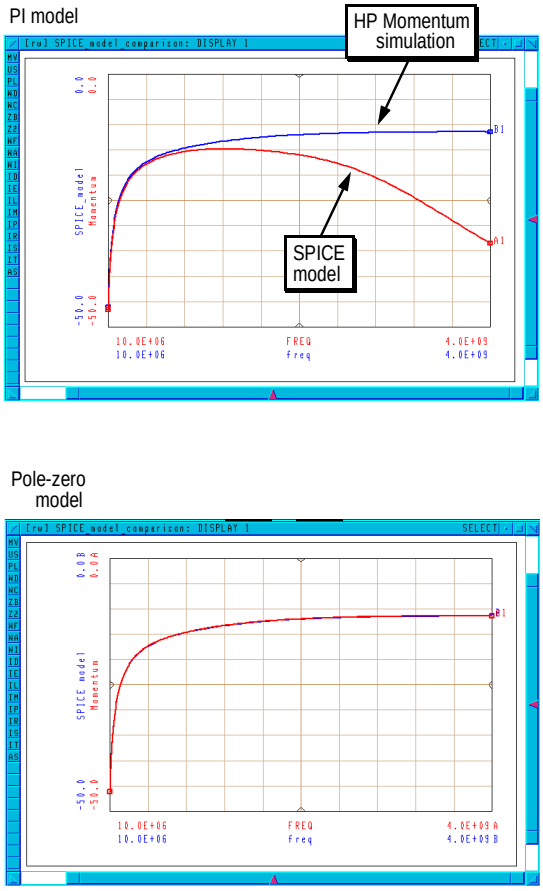


Figure 22. *The HP Momentum-simulated geometry used as part of a larger circuit simulation. The four lines on the top layer are simultaneously driven, and the coupled signals are sampled and measured. The plot shows signals at the source, the receiver, and at the four reverse-coupled ports. The clock frequency is 250 MHz.*

The geometry of the 16-port circuit in Figure 20 results in relatively uncomplicated S-parameters that can be modeled well up to about 800 MHz with the simple PI network option in the SPICE model generator. Above 800 MHz, the best results are obtained with the pole-zero model, even though the pole-zero representation cannot be directly related to a physical circuit representation. Figure 23 shows both results.




```
SPICE 2G6 netlist generated from [S] parameters
.subckt LAYOUT_AFS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
* L in nH, C in pF
C1 1 0 3.48797P                  C30 8 0 1.31375P
C2 1 2 0.0488154P                C31 8 13 1.02124P
R1 1 2 36695.9                   C32 8 16 0.166576P
R2 1 4 30490.3                   C33 13 0 0.692543P
R3 1 10 8117.91                  C34 13 14 1.27666P
C3 1 12 1.04006P                 C35 13 15 0.427104P
C4 2 0 1.09055P                  C36 13 16 0.372077P
R4 2 0 4513.19                   C37 14 15 0.181169P
R5 2 4 15106                     C38 15 16 0.0869215P
C5 2 9 0.202499P                 L1 1 5 10.6509N
C6 2 10 0.190742P                L2 2 6 10.6617N
C7 2 11 0.304618P                L3 3 7 10.6263N
C8 3 9 0.159493P                 L4 4 8 10.6514N
R6 3 9 9042.97                   L5 9 13 10.6826N
C9 3 11 0.0214974P               L6 10 14 10.6582N
R7 3 11 10177.3                  L7 11 15 10.658N
R8 3 12 10658.2                  L8 12 16 10.6816N
R9 4 0 12424.7                   K1 L1 L-2 7.19881N
R10 4 9 23960.8                  K2 L1 L-1 6.06953N
C10 4 10 0.232771P               K3 L1 L0 5.42998N
R11 4 10 16953.2                 K4 L1 L5 4.59527N
C11 4 11 0.241931P               K5 L1 L6 4.54897N
C12 4 12 0.193545P               K6 L1 L7 4.57894N
R12 4 12 127468                  K7 L1 L8 4.63019N
R13 9 0 155054                   K8 L2 L-1 7.21301N
C13 9 10 0.123658P               K9 L2 L0 6.06977N
C14 9 11 0.0589382P              K10 L2 L5 4.55265N
R14 9 11 93854.7                 K11 L2 L6 4.57079N
C15 9 12 0.28859P                K12 L2 L7 4.54759N
R15 9 12 74219.5                 K13 L2 L8 4.57937N
R16 10 0 25793.5                 K14 L3 L0 7.19626N
C16 10 11 0.0431278              K15 L3 L5 4.58339N
R17 10 11 146252                 K16 L3 L6 4.57412N
C17 10 12 0.496265P              K17 L3 L7 4.56982N
C18 11 12 1.30483P               K18 L3 L8 4.5493N
R18 11 12 9773.35                K19 L4 L5 4.63853N
C19 12 0 0.355848P               K20 L4 L6 4.58331N
C20 5 14 0.18751P                K21 L4 L7 4.55227N
C21 5 15 0.261242                K22 L4 L8 4.59536N
C22 6 0 1.1599P                  K23 L9 L6 7.22777N
C23 6 7 0.269519P                K24 L9 L7 6.10138N
C24 6 14 0.0724635P              K25 L9 L8 5.44905N
C25 6 16 0.468736P               K26 L10 L7 7.24489N
C26 7 0 2.01697P                 K27 L10 L8 6.10152N
C27 7 8 1.37524P                 K28 L11 L8 7.22998N
C28 7 14 0.280964P               .ENDS
C29 7 16 0.324217P               * end of  sub-circuit
```

Figure 23. *Results of using the SPICE model generator with the HP Momentum-generated S-parameter of the circuit in Figure 18. These plots show S21, which represents the crosstalk between two inputs. The PI model matches the simulation results well up to about 800 MHz; the pole-zero model matches the simulation results almost exactly throughout the simulated frequency range (the two plotted lines are directly on top of one another). On the right is the PI-model equivalent circuit generated by the SPICE model generator.*

Appendix: Simulation Technology

Proper use of the HP Picosecond Interconnect Modeling Suite requires some knowledge of the underlying linear and nonlinear simulation technology. This appendix is intended to fill in some of those details.

Linear Frequency-Domain Simulation: AC Analysis

Linear AC analysis, which operates in the frequency domain, is a very high-efficiency (fast) technique for certain types of high-frequency problems such as impedance analysis, step response measurements, and clock waveform degradation. While AC analysis does not work well with nonlinear devices such as bus drivers, it is by far the most efficient (fastest) way to analyze passive components and transmission lines. The results of an AC analysis can then be used later in a full nonlinear analysis using HP Impulse or SPICE.

AC analysis in the HP Picosecond Interconnect Modeling Suite has little in common with the familiar AC analysis mode in SPICE. To perform an AC analysis, SPICE first performs a DC simulation to find the operating point of any nonlinear devices in the circuit. Then, SPICE calculates the response of the circuit to small changes around the operating point (it “linearizes” the circuit). SPICE then performs a time-domain analysis of the circuit, given any arbitrary input signal, under the assumption that the voltages and currents everywhere in the circuit are “small” and do not exercise any nonlinear circuit effects.

In the HP Picosecond Interconnect Modeling Suite, AC analysis begins with a DC analysis and a “linearization” of the circuit, just as with SPICE. The similarity with SPICE ends here. After the circuit's linearized response is calculated, it is assumed that all signals in the circuit are sine waves. (Other periodic signal waveforms are easily created using Fourier series.) Furthermore, these sine waves are not allowed to generate any harmonics or nonlinear mixing products. Of course, multiple independent sine waves at different frequencies can exist at the same time. Table illustrates the differences between AC analysis in SPICE and AC analysis in the HP Picosecond Interconnect Modeling Suite.

Table 1. *Differences between SPICE and the HP Picosecond Modeling Suite for AC analysis. Most importantly, the type of AC analysis in the HP Picosecond Interconnect Modeling Suite is much faster than SPICE for the appropriate types of circuit analyses.*

AC Analysis in SPICE	**AC Analysis in the HP Picosecond Interconnect Modeling Suite**
Begins with DC analysis	Begins with DC analysis
“Linearizes” the circuit	“Linearizes” the circuit
Can handle any waveform	Can only handle periodic signals (sine waves and Fourier series)
Simulates in time domain	Simulates in frequency domain
Long simulation times	*Short simulation times*
Finds full transient response (except for nonlinear component effects)	Finds steady-state response only

Since all voltage and current waveforms are assumed to be linear combinations of independent sine waves, the generalized differential equations that describe any circuit's response can be simplified dramatically by the computer and solved very quickly. However, the circuit's transient response is lost in this process. Only the steady-state circuit response is calculated.

Frequency-domain analysis is extremely fast and efficient for certain types of analyses, including:

Impedance: Transmission line impedance is an inherent part of the frequency-domain models used in the HP Picosecond Interconnect Modeling Suite, and impedance is particularly easy to calculate in the frequency domain. Furthermore, a feature of the HP Picosecond Interconnect Modeling Suite allows designers to find transmission line geometries that result in a given impedance (optimization), as well as calculating the impedance of a given line (analysis).

Because the effective impedance of a transmission line can change with frequency, impedance calculations in the HP Picosecond Interconnect Modeling Suite can be made to consider either a single frequency or to calculate an weighted-average impedance over a range of frequencies, taking into account the fact that most of the energy in a digital signal exists at the clock frequency and the first several harmonics. Furthermore, the effective impedance of a line can be affected by the presence of coupling from other nearby lines. The HP Picosecond Interconnect Modeling Suite includes pre-defined analysis setups to help designers examine the effects of all of these problems. Figure 24 illustrates.

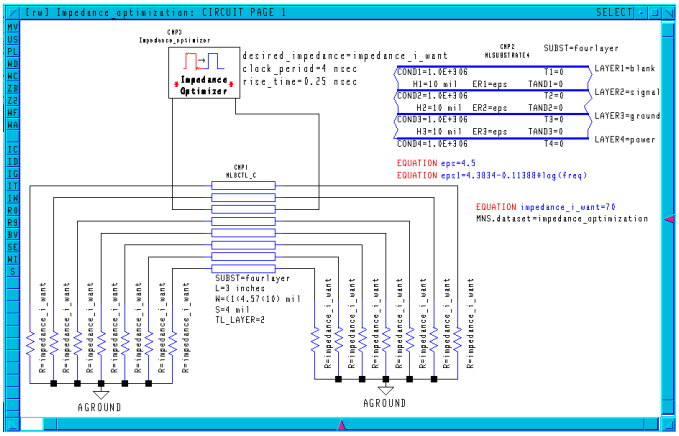


Figure 24. *This window from the HP Picosecond Modeling Suite shows an 8-line-wide bus on the second layer of a four-layer circuit board. The width of the transmission lines is being optimized so that the impedance of the outermost line will be 70Ω.*

Step response: Frequency-domain AC analysis can be used to find the step response of a linear circuit, exactly as it would appear on a time-domain reflectometer (TDR). To do this, a very long-period pulse train is applied to the circuit's input, exactly as it would be implemented with a real TDR.

A time-domain reflectometer is used for viewing discontinuities and impedances in complicated transmission lines. To accomplish this, a very fast-rise-time edge is applied to the input of a network. As it travels through the network, discontinuities such as mismatched transmission line impedances will cause part of the edge to be reflected back to the source. Multiple reflections can (and do) occur, resulting in circuit ringing that can have an unexpectedly long lifetime. By observing the reflected signal, the location of a discontinuity can be calculated from the delay time before the reflection is seen. The impedance of the discontinuity can be calculated from the magnitude of the reflected signal.

Using AC analysis, a pulse train can be created using a Fourier series of independent sine waves. A pulse train with magnitude 1 can be expressed as a series of independent sine waves given by:

$$\text{for } n = 1, 3, 5\ldots \quad f(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\frac{2n\pi t}{T}$$

$$\text{for } n = 2, 4, 6\ldots \quad f(t) = 0$$

where T = the period of the pulse train

This waveform can be easily reproduced in the frequency domain by applying a combination of independent tones, with appropriate magnitudes, to the circuit. The circuit's response can then be reproduced in the time domain by adding all of the output tones together. With voltage probes placed at appropriate points in the circuit the time-domain reflection and transmission responses can be observed.

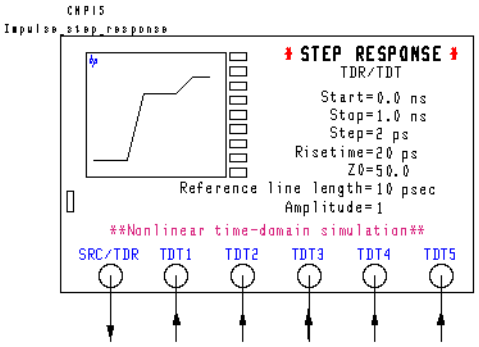


Figure 25. *A pre-built simulation component for finding time-domain reflection and transmission response from the HP Picosecond Interconnect Modeling Suite.*

Clock waveform analysis: Using the same technique as for step response analysis, a clock waveform can be created using a Fourier series. The resulting clock signal can then be viewed in the time domain as though it was on the screen on an oscilloscope.

The HP Picosecond Interconnect Modeling Suite includes pre-built analysis templates for both step response and clock waveform analyses that allow designers to easily examine the response of up to five transmitted signals (see Figure 25).

Coupling*:* Coupling (or crosstalk) between two transmission lines is inherently frequency-dependent and is best modeled in the frequency domain. Using AC analysis, a frequency-domain model for coupled transmission lines can be created quickly. This data can be used to create a lumped-element SPICE model and included in more complete circuit simulations that include nonlinear devices (the SPICE model generation process is discussed later in this product note), or HP Impulse can be used for nonlinear analysis without the need for model generation.

The HP Picosecond Interconnect Modeling Suite includes models for coupled lines in nearly any configuration, including multi-level PC boards. Impedance, step response and clock waveform analyses can be performed on any of these coupled-line models.

Nonlinear Time-domain Simulation: HP Impulse

Digital designers are generally familiar with the time-domain analysis capabilities of SPICE and its numerous commercial derivatives. HP Impulse is a SPICE-like simulator, included with the HP Picosecond Interconnect Modeling Suite, with additional simulation capabilities and models that are important for high-speed circuit simulation.

Transmission lines and connectors have a negligible effect on circuit performance at low clock rates. Other factors, such as gate delay and power supply ringing, overwhelm their small effects. At higher clock rates, however, transmission line delays may be longer than gate delays; connectors cannot be modeled as simple ideal transmission lines; and impedance mismatches can cause high levels of ringing.

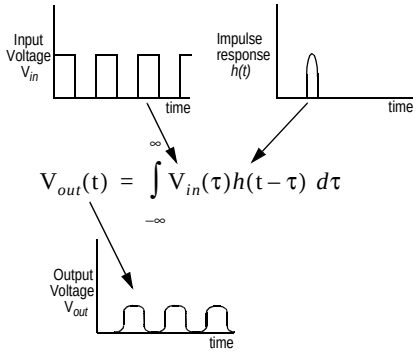


Figure 26. *HP Impulse finds the time-domain response of frequency-domain models using convolution integrals.*

Unfortunately, these high-frequency circuit effects cannot be modeled well in SPICE. Their distributed nature makes these effects easy to model in the frequency domain but difficult time domain. Some of these effects may be modeled using lumped-element equivalent circuits, but good models are not commonly available for all types of circuit interconnecting geometries.

To handle these types of components, HP Impulse adds a new type of analysis to the traditional SPICE algorithms[1]. Called dynamic convolution, this technique allows frequency-domain models to be included in time-domain simulations. Simply put, HP Impulse calculates the impulse response of all frequency-domain component models. Then, to find the actual circuit response, the simulator calculates the convolution integral of these components' impulse responses with the actual time-domain driving voltage. Figure 26 illustrates.

Using dynamic convolution, HP Impulse can perform time-domain simulations on very high-speed circuits while including all high-frequency parasitic effects. Furthermore, actual measured data, like S-parameters, can be used to model elements that have no analytic model.

Time-domain simulations can, of course, duplicate the step-response and clock waveform analysis simulations that can be performed using frequency-domain AC analysis. However, there are some important differences between the results that may be obtained using the two different techniques, for two reasons:

- AC analysis is a linear simulation, while HP Impulse is a nonlinear simulation; and
- AC analysis yields only steady-state information while HP Impulse yields start-up information as well.

For the design engineer using these tools, it is critical to understand the differences. This topic is illustrated in many of the examples in this product note. In general, AC simulation should be used first for speed and efficiency. Later, nonlinear simulation can be used to observe the effects of nonlinear drivers and receivers.

Electromagnetic Simulation: HP Momentum

In general, circuit simulators are limited by the models that are supplied with them. This is particularly true when high-frequency effects such as coupling must be taken into account. For instance, SPICE includes models for basic transmission lines, but it does not include models for the coupling that may occur in complicated multi-layer, multi-line circuit board layouts.

The HP Picosecond Interconnect Modeling Suite includes built-in models for many different layout geometries, including multi-layer circuit boards with coupling between many different lines. Still, it is impossible to supply models for all possible layouts. HP Momentum is one solution to this problem.

HP Momentum uses the method of moments simulation technique to create SPICE models for arbitrary circuit board layouts. By completely solving Maxwell's equations, HP Momentum automatically includes all high-frequency circuit effects in its models. There are only a few general restrictions:

- HP Momentum can only analyze 2-dimensional layered structures, such as multi-layer PC boards. It cannot generate models for arbitrary 3-D structures such as connectors or ribbon cables that are routed between two different circuit boards.
- HP Momentum can only analyze passive components such as transmission lines. It cannot generate models for active devices like bus drivers.
- The method of moments simulation technology uses much more computer memory than conventional circuit simulation techniques, so the size of circuits that can be simulated with HP Momentum is limited.

1. The most recent versions of SPICE have the ability to handle transmission lines through convolution, just as HP Impulse does. However, SPICE does not include all of the high-frequency models that are needed for real-world designs.

Using HP Momentum involves three steps, shown pictorially in Figure 27:

1. Draw the circuit's layout. The HP Picosecond Interconnect Modeling Suite's optional Layout module is ideal for this. Layouts can be created automatically from a schematic diagram, or they can be drawn manually.
2. Define inputs and outputs, and simulate the layout. HP Momentum breaks up the layout into small pieces, called a mesh, and uses the mesh to calculate S-parameters for the layout at all user-specified frequencies.
3. Using the calculated S-parameters, generate a SPICE model for use in further simulations. (For simulations performed in the HP Picosecond Interconnect Modeling Suite, the S-parameters can be used directly without the need to generate a SPICE model.)

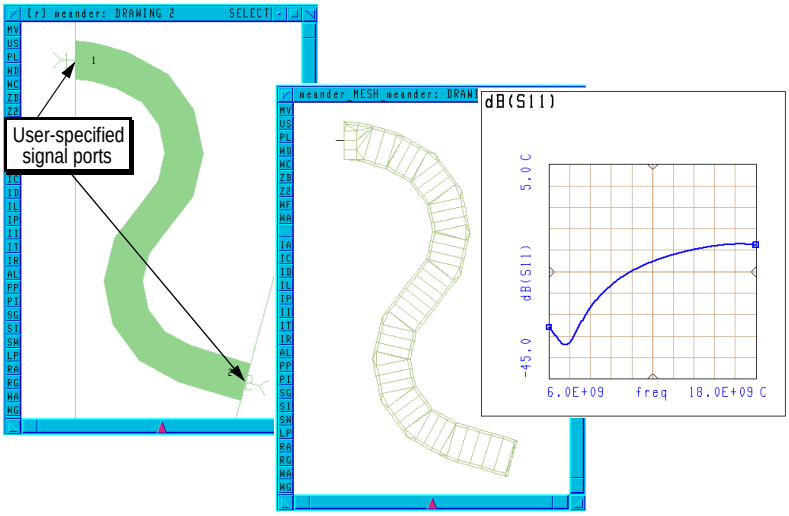


Figure 27. *To simulate an arbitrary layout like this simple curved transmission line, HP Momentum calculates a mesh (middle window) and uses it to find the layout's S-parameters. The S-parameters can then be used to create a lumped-element SPICE model of the transmission line.*

SPICE Model Generation

SPICE model generation provides a bridge between the fast interconnect modeling of AC analysis and the full nonlinear simulation capabilities of SPICE. AC analysis and HP Momentum are fast, efficient tools for calculating the frequency-domain response of passive linear structures. Neither tool, however, can handle nonlinear circuits; and neither tool is suitable for simulating large digital systems in their entirety. For those purposes, SPICE is the most common tool. To assist in these situations, the HP Picosecond Interconnect Modeling Suite supplies a SPICE model generator that extracts lumped-element SPICE models from frequency-domain simulation results.

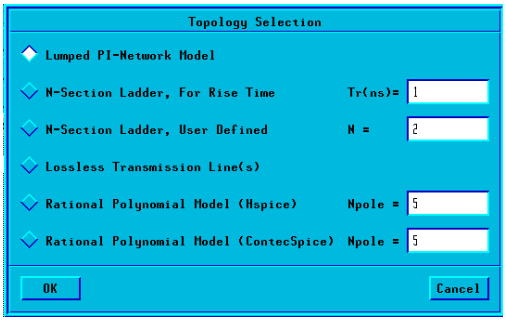


Figure 28. *The HP Picosecond Interconnect Modeling Suite's SPICE model generator offers several choices of lumped-element topology as well as polynomial (pole-zero) models.*

To transform frequency-domain data into lumped-element equivalent circuits, one major hurdle that must be overcome is the choice of topology for the equivalent circuit. Because frequency-domain data contains no information about circuit topology, the SPICE model generator allows the user to choose a topology (see Figure 28). Several possible topologies are included, along with rational polynomial models that can be used with some newer commercial SPICE variations.

The different available model topologies are best used for specific purposes. Transmission lines, for instance, are often best modeled with a ladder network, because that type of network yields the best approximation to the actual response of a transmission line. The following table lists the different available topologies and their suggested uses.

Topology	Suggested Use
Lumped PI Network	Very simple narrowband model; limited accuracy for fast risetime circuits
N-section ladder, for rise time	Transmission line modeling with accuracy to a user-specified risetime
N-section ladder, user-defined	Transmission line modeling with a user-specified number of sections
Lossless transmission line(s)	Fastest, most accurate model for PCB traces
Rational polynomial model (HSpice)	Accurate modeling of arbitrary networks (resistive loss only; no dispersion). Creates a netlist in HSpice format.
Rational polynomial model (ContecSpice)	Accurate modeling of arbitrary networks (resistive loss only; no dispersion). Creates a netlist in ContecSpice format.

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