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# Using External Feedback to Achieve Flat Gain with the MSA-0885

## Application Note S006

### Introduction

One of the classic problems facing the microwave designer is to build a cascadable amplification stage having flat power gain over a broad frequency range. The difficulties arise from the gain vs frequency characteristics of semiconductor devices. Up to some frequency $f_\beta$ transistors exhibit flat gain vs frequency performance. Above $f_\beta$ the gain of the transistor will drop at a rate of 6 dB per octave (i.e. the amplification factor will decrease by 1/4 for each doubling in frequency.) Since $f_\beta$ is a relatively low frequency (300 MHz typically for the SAT bipolar process) the designer is usually working in this area of gain rolloff. Thus a "perfectly matched" amplifier (an amplifier with both $S_{11}$ and $S_{22}$ conjugately matched) will also exhibit a 6 dB per octave gain rolloff. If the amplifier is intentionally mismatched to flatten gain, the result will be high VSWRs at either the circuit input or output. The resulting amplifier will not cascade well due to interactions (impedance mismatch) or load stages.

One solution to this problem is the use of feedback. Feedback allows the designer to trade gain for bandwidth; in essence, through feedback the semiconductor becomes a device with a lower gain and a higher $f_\beta$. The only limitation is that at any given frequency the gain of the feedback amplifier will at best be equal to and usually several dB less than the maximum available gain of the original semiconductor. If both parallel (base to collector) and series (emitter) feedback are used simultaneously, the resulting amplifier can have low input and output VSWRs as well as constant amplification over a wide bandwidth.

HP's MSA line of silicon monolithic amplifiers makes use of this technique to achieve good match and flat gain over very wide bandwidths. There will, however, always be times when a circuit is needed that will perform to a still higher frequency before the inevitable rolloff occurs. What can a designer do? One answer is to use more feedback!

Consider the case of the MSA-0885. This device uses minimum feedback to achieve high gains at low frequencies (greater than 30 dB below 500 MHz) while still having useful gain at high frequencies

(greater than 10 dB at 4 GHz). Through the application of external feedback to the MSA-0885 it is possible to design a well matched single stage amplifier that will have a flat gain response to beyond 3 GHz.

## Initial Simulation

The design begins with a TOUCHSTONE™ computer simulation comparing a standard MSA-0885 amplifier to an MSA-0885 amplifier including additional external feedback. The file is shown in Table 1.

The simulation starts with a description of the substrate material. In this case information for both teflon-fiberglass (ε = 2.2) and epoxy glass (ε = 4.8) substrates is included (As shown the line for epoxy glass is "commented out" of the program). The microstrip lines are then modeled in terms of their physical dimensions in mils. The MSA-0885 is described by a measured set of S parameters contained in a file named MSA0885.S2P. This file is reproduced in Table 2.

**Table 1. Initial Simulation of Feedback Amplifier**

```
VAR
 T1=32          !board thickness (mils)
 W1\110         !microstrip line width (mils)
CKT
 MSUB   ER=2.55 H^T1 T=1 RHO=1 RGH=0   !teflon fiberglass
 !MSUB  ER=4.8  H^T1 T=1 RHO=1 RGH=0   !epoxy glass
!MSA0885 AMPLIFIER (NO FEEDBACK)
 SLC          1       2              L=.5 C=1000
 MLIN         2       3              W^W1 L=100
 S2PA         3       4       5      A:MSA0885
 VIA          5       0              D1=30 D2=30 H^T1 T=1
 MLIN         4       7              W^W1 L=100
 SLC          7       8              L=.5 C=1000
 DEF2P        1       8              A08
!MSA0885 AMPLIFIER (FEEDBACK ADDED)
 SLC          1       2              L=.5 C=1000
 MLIN         2       3              W^W1 L=100
 S2PA         3       4       5      A:MSA0885
 SRL          5       6              R\6.7 L=.5
 VIA          6       0              D1=30 D2=30 H^T1 T=1
 SRLC         3       4              R\225 L=1 C=1000
 MLIN         4       7              W^W1 L=100
 SLC          7       8              L=.5 C=1000
 DEF2P        1       8              AMP

FREQ
 STEP          .1
 SWEEP         .5      6       .5
GRID
 GR1           0       40      5
 GR2           -30     0       -5
OUT
 A08           DB[S21]         GR1
 AMP           DB[S21]         GR1
 A08           DB[S11]         GR2
 A08           DB[S22]         GR2
 AMP           DB[S11]         GR2
 AMP           DB[S22]         GR2
OPT
 RANGE        .1      4
 AMP          DB[S21]>11.3
 AMP          DB[S21]<11.8
 AMP          DB[S11]<-14
 AMP          DB[S22]<-14
```

**Table 2. S Parameters of MSA-0885, $I_D$ = 36 mA**

| Freq. | S11 | | S21 | | S12 | | S22 | |
|---|---|---|---|---|---|---|---|---|
| GHz | Mag | Ang | Mag | Ang | Mag | Ang | Mag | Ang |
| 0.1 | .64 | –21 | 42.29 | 160 | .015 | 40 | .61 | –24 |
| 0.2 | .58 | –39 | 36.89 | 144 | .023 | 50 | .54 | –45 |
| 0.4 | .44 | –65 | 27.20 | 120 | .034 | 54 | .42 | –77 |
| 0.6 | .36 | –82 | 20.57 | 106 | .044 | 53 | .33 | –98 |
| 0.8 | .31 | –95 | 16.31 | 96 | .055 | 53 | .28 | –115 |
| 1.0 | .27 | –105 | 13.36 | 87 | .061 | 51 | .25 | –129 |
| 1.5 | .24 | –125 | 9.24 | 71 | .085 | 50 | .18 | –153 |
| 2.0 | .26 | –147 | 6.82 | 56 | .103 | 47 | .15 | –173 |
| 2.5 | .29 | –159 | 5.57 | 48 | .120 | 44 | .12 | 180 |
| 3.0 | .34 | –175 | 4.51 | 37 | .130 | 42 | .09 | 165 |
| 3.5 | .38 | 172 | 3.80 | 25 | .144 | 37 | .06 | 172 |
| 4.0 | .42 | 161 | 3.21 | 14 | .153 | 33 | .04 | –139 |
| 5.0 | .48 | 135 | 2.43 | –7 | .167 | 24 | .09 | –90 |
| 6.0 | .60 | 102 | 1.88 | –29 | .179 | 17 | .08 | –140 |

Since these S parameters are measured in a fixture that connects the MMIC common leads directly to ground, a via model is used to simulate the added inductance in the ground path incurred by passing through the pc board. Both blocking capacitor and feedback resistor models include appropriate associated parasitic inductance. Bias networks are omitted as they are assumed to incorporate chokes high enough in value to avoid any impedance matching effects.

Working with this model in the “tune” mode, the designer will quickly notice several things. First, it should be possible to build an amplifier with 11 dB of flat gain to past 3 GHz with input and output return loss less than 10 dB. Secondly, the bandwidth limitation is set primarily by the inductance associated with the emitter feedback. The lower this inductance can be kept, the broader the bandwidth over which the amplifier will function. Thirdly, the improved match of the feedback amplifier will actually improve gain performance beyond the 50 Ω power gain of the original MSA-0885 (but not beyond its MAG).

In order to reduce the parasitic emitter inductance, the physical distance to ground has to be decreased. This is done using a new pc board layout which places the emitter resistor directly against the MSA-0885 ground lead on one end and on top of a via to ground on the other (see Figure 1). This construction technique results in a flat gain of 11.5 dB out to 3.3 GHz.

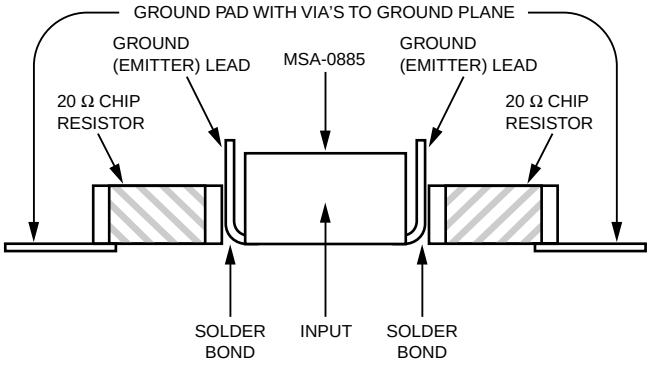



**Figure 1. Diagram of Shortened Ground Path**

Finding the best value for the choke inductor is a complex issue. After trying several inductors of varying values, a 1 µH molded inductor is chosen as it minimizes the high frequency ripple (less than 1 dB) while maintaining the gain at 11 dB. The choice is based solely on observed performance because it is difficult to precisely model the exact parasitics of the choke network.

The inductance associated with the parallel feedback path contributes to the high frequency ripple of the circuit; consequently, the physical length of this path is reduced to a minimum (see Figure 2 for construction technique). The value of the feedback resistor is also increased to 330 Ω, which provides the best gain while still maintaining an input match with more than 10 dB return loss. Open circuit stubs added to the input transmission line are incorporated in the final amplifier to further improve high frequency input match.

## Amplifier Performance

A schematic for the final circuit is shown in Figure 3. Amplifier performance is characterized in terms of S parameters over the 300 MHz to 6.3 GHz frequency range, with the MSA-0885 operating at a device current $I_D$ of 36 mA. Refer to Figure 4a and 4b. These measurements show nearly 12 dB of flat (less than 0.5 dB ripple) gain out to 3.8 GHz, beyond

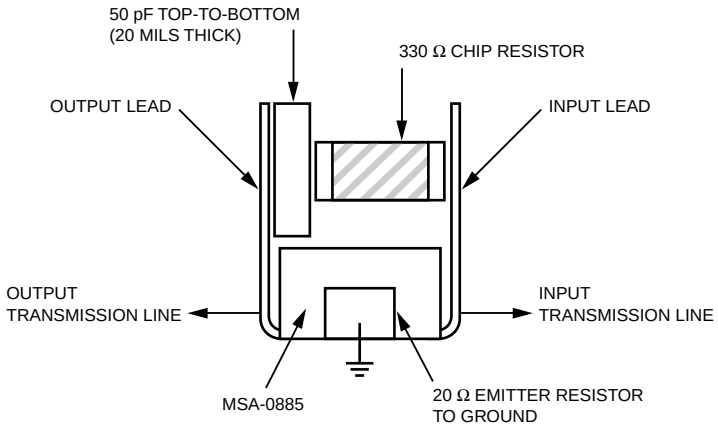
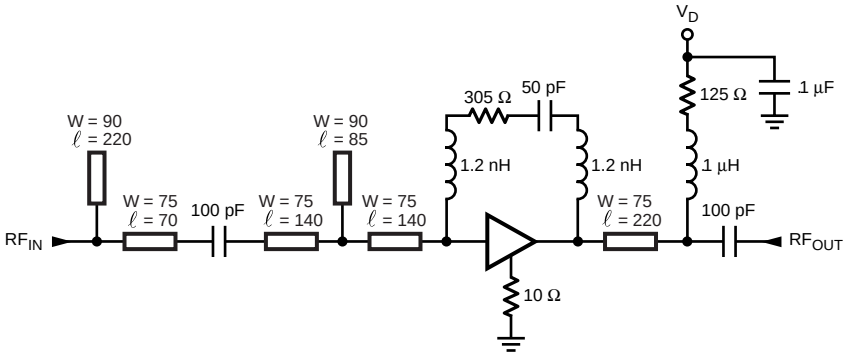



**Figure 2. Diagram of Feedback Path**




BOARD MATERIAL = 1/32" TEFLON-FIBERGLASS (ε = 2.55)

**Figure 3. MSA-0885 Feedback Amplifier Schematic**

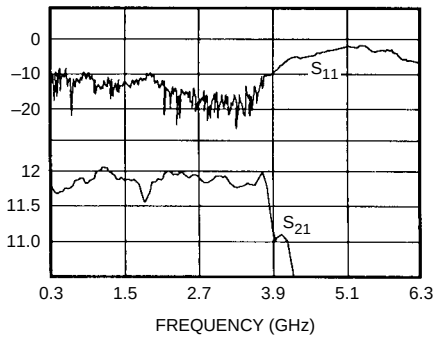



**Figure 4a. $S_{11}$ and $S_{21}$ of MSA-0885 Feedback Amplifier**

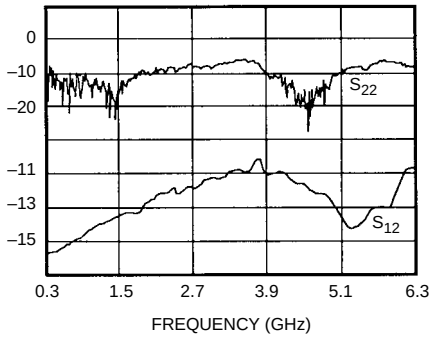



**Figure 4b. $S_{22}$ and $S_{12}$ of MSA-0885 Feedback Amplifier**

which frequency gain rolls off very rapidly. Input and output return losses are on the order of 10 dB over this frequency range. Isolation drops from approximately 15 dB at the low end of the band to 10 dB near 4 GHz.

## Prototype Circuit

A prototype circuit is built, based on the initial simulation. This circuit verifies that the inductance associated with the emitter feedback resistor is the determining element for high frequency gain rolloff. The layout of this initial circuit incorporates an isolated "pad" adjacent to the emitter lead to which both the device lead and the feedback resistor are soldered. Even though the circuit elements are positioned to keep the path length to ground as short as possible, the extra path length introduced by this floating "pad" plus the parasitic inductance of the chip resistor used add 2.2 nH of inductance to the emitter path. This amount of inductance limits the upper frequency at which the amplifier has acceptable performance (less than 1 dB gain rolloff and input and output return losses of more than 10 dB) to below 1.1 GHz.

An aspect of the circuit that has been omitted from the simulation but warrants closer inspection is the bias choke network. The initial design uses a printed high impedance line in series with the bias stabilization resistor as the "choke" between the bias network and the rf circuitry. Measurements show that the impedance of this network is not sufficient to keep the bias network from affecting the load impedance presented to the MSA-0885. The easiest way to correct this problem is to replace the microstrip line with a "lumped" element. A 0.1 μH molded inductor has been tried; the parasitics associated with it caused a large resonance at 3.3 GHz. Next a 100 μH chip inductor is used. While it provides extremely flat gain (0.4 dB ripple) out to 3 GHz, the response fluctuates severely beyond 3 GHz. There are high frequency resonances in the bias network that will have to be minimized through the selection of specific values of choke inductance.

## Second Simulation And Final Circuit

The TOUCHSTONE simulation is reworked (Table 3) to help analyze the problems observed with the prototype amplifier. Special attention is paid to minimizing the emitter inductance and selecting a choke

**Table 3a. Revised Circuit File**

```
VAR
 T1=32          !board thickness (mils)
 W1=75          !microstrip line width (mils)


CKT
 MSUB   ER=2.55 H^T1 T=1 RHO=1 RGH=0   !teflon fiberglass

 MLOC        1                    W=90 L=220
 MLIN        1       2            W^W1 L=70
 SLC         2       3            L=.7 C=100
 MLIN        3       4            W^W1 L=140
 MLOC        4                    W=90 L=85
 MLIN        4       5            W^W1 L=140
 S2PA        5       6       7    A:MSA0885.S2P
 SRL         7       0            R=10 L=.5
 SRL         5       8            R=305 L=1.2
 SLC         8       6            L=1.2 C=50
 MLIN        6       9            W^W1 L=220
 IND         9       10           L=100
 RES         10      11           R=125
 SLC         11      12           L=1 C=1E5
 SLC         9       13           L=.7 C=100
 DEF2P       1       13           AMP


FREQ
 STEP        .1
 SWEEP       .5      6       .5


OUT
 AMP          DB[S21]        GR1
 AMP          DB[S11]        GR1A
 AMP          DB[S22]        GR1A
 AMP          K


GRID
 GR1         0       15      1
 GR1A        30      -30
```

**Table 3b. Output of Revised Circuit File**

| Freq. GHz | DB[S21] AMP | DB[S11] AMP | DB[S22] AMP | K AMP |
|---|---|---|---|---|
| 0.30000 | 11.785 | –16.032 | –16.771 | 1.086 |
| 0.90000 | 11.790 | –13.551 | –14.339 | 1.049 |
| 1 50000 | 11.851 | –11.396 | –12.980 | 1.011 |
| 2.10000 | 12.165 | –11.083 | –13.709 | 0.999 |
| 2.70000 | 12.265 | –14.782 | –15.552 | 0.997 |
| 3.30000 | 12.468 | –21.457 | –12.540 | 0.967 |
| 3.90000 | 11.373 | –7.962 | –11.529 | 0.875 |
| 4.50000 | 9.165 | –4.580 | –16.294 | 0.750 |
| 5.10000 | 6.724 | –3.794 | –13.627 | 0.657 |
| 5.70000 | 5.232 | –4.729 | –6.043 | 0.614 |
| 6.30000 | 4.075 | –8.024 | –0.450 | 0.661 |

network that does not create high frequency resonances. Several circuit changes are implemented based on the new simulation.

At the nominal bias of $I_D$ = 36 mA, the circuit has a noise figure between 4.5 and 6.5 dB when operated in the frequency range where the gain remains flat. Reducing the bias to $I_D$ = 20 mA by decreasing the voltage applied to the bias circuit from 12.5 V to 10 V yields no significant changes in noise performance, but results in a lower gain amplifier. When the current is raised to 50 mA (voltage of 14 V), the noise figure increases by roughly 0.25 dB, and the gain performance is comparable to that observed at the 36 mA bias. The noise performance at these bias points is plotted in Figure 5.

Below 2 GHz, 1 dB compressed power ($P_{1\ dB}$) is significantly influenced by bias. The nominal bias of 36 mA yields the best overall result with a typical $P_{1\ dB}$ of 12 dBm. Above 2 GHz the $P_{1\ dB}$ rolls off fairly quickly (down to 6 dBm at 4 GHz), and is not as strongly influenced by bias level. The measurements of $P_{1\ dB}$ vs frequency as a function of bias current are plotted in Figure 6.

## Conclusion

The design and construction of a broadband flat gain amplifier using MSA-0885 has been discussed. Emitter parasitics and feedback resistor values are the most important considerations in this design to achieve good gain and bandwidth. The final amplifier exhibits nearly 12 dB of flat gain to beyond 3.5 GHz.

Low frequency performance of this amplifier is determined by the values of blocking capacitor used in the feedback network, as well as the series dc blocks in the input and output transmission lines. For all experimental data the low frequency is taken to be 300 MHz. Simulations predict the operational range will extend down to 30 MHz with sufficiently large values of capacitors.

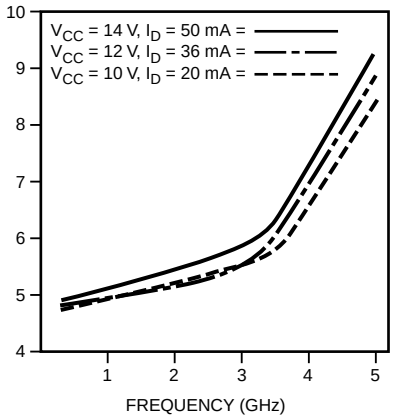



**Figure 5. Noise Figure vs Frequency for MSA-0885 Feedback Amplifier**

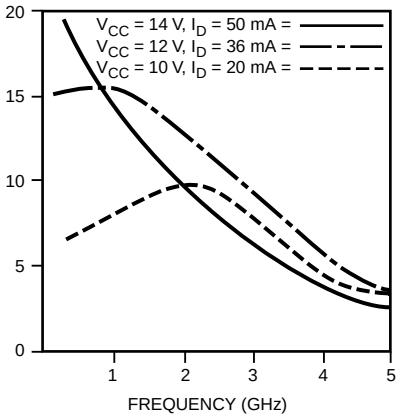



**Figure 6. $P_{1\ dB}$ vs Frequency for MSA-0885 Feedback Amplifier**

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Data Subject to Change



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