Designing with the MGA-72543 RFIC Amplifier / Bypass Switch

Application Note RLM020199

Applies to MGA-72543 GaAs RFIC

Description

The MGA-72543 is a single-stage, GaAs RFIC amplifier with an integrated bypass switch. A functional diagram of the MGA-72543 is shown in Figure 1.

The MGA-72543 is designed for receivers and transmitters operating from 100 MHz to 6 GHz with an emphasis on 1.9 GHz CDMA applications. The MGA-72543 combines low noise performance with high linearity to make it especially advantageous for use in receiver front-ends.

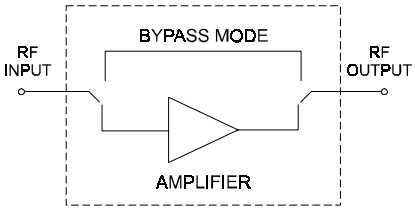


Figure 1. MGA-72543 Functional diagram.

The purpose of the switch feature is to prevent distortion of high signal levels in receiver applications by bypassing the amplifier altogether. The bypass switch can be thought of as a 1-bit digital AGC circuit that not only prevents distortion by bypassing the MGA-72543 amplifier, but also reduces front-end system gain by approximately 16 dB to avoid overdriving subsequent stages in the receiver such as the mixer.

An additional feature of the MGA-72543 is the ability to externally set device current to balance output power capability and high linearity with low DC power consumption. The adjustable current feature of the MGA-72543 allows it to deliver output power levels in excess of +15 dBm (P_{1dB}), thus extending its use to other system applications such as transmitter driver stages.

The MGA-72543 is designed to operate from a +3-volt power supply and is contained in a miniature 4-lead, SOT-343 (SC-70) package to minimize printed circuit board space.

LNA Applications

For low noise amplifier applications, the MGA-72543 is typically biased in the 10 – 20 mA range. Minimum NF occurs at 20 mA as noted in the performance curve of NF_{min} vs. I_d. Biasing at currents significantly less than 10 mA is not recommended since the characteristics of the device began to change very rapidly at lower currents.

The MGA-72543 is matched internally for low NF. Over a current range of 10 – 30 mA, the magnitude of Γ_{opt} at 1900 MHz is typically less than 0.25 and additional impedance matching would only net about 0.1 dB improvement in noise figure.

Without external matching, the input return loss for the MGA-72543 is approximately 5 dB at 1900 MHz. If desired, a small amount of NF can be traded off for a significant improvement in input match. For example, the addition of a series inductance of 2.7 to 3.9 nH at the input of the MGA-72543 will improve the input return loss to greater than 10 dB with a sacrifice in NF of only 0.1 dB.

The output of the MGA-72543 is internally matched to provide an output SWR of approximately 2:1 at 1900 MHz. Input and output matches both improve at higher frequencies.

Driver Amplifier Applications

The flexibility of the adjustable current feature makes the MGA-72543 suitable for use in transmitter driver stages. Biasing the amplifier at 40 – 50 mA enables it to deliver an output

power at 1-dB gain compression of up to +16 dBm. Power efficiency in the unsaturated driver mode is on the order of 30%. If operated as a saturated amplifier, both output power and efficiency will increase.

Since the MGA-72543 is internally matched for low noise figure, it may be desirable to add external impedance matching at the input to improve the power match for driver applications. Since the reactive part of the input of the device impedance is capacitive, a series inductor at the input is often all that is needed to provide a suitable match for many applications. For 1900 MHz circuits, a series inductance of 3.9 nH will match the input to a return loss of approximately 13 dB.

As in the case of low noise bias levels, the output of the MGA-72543 is already well matched to 50 Ω and no additional matching is needed for most applications.

When used for driver stage applications, the bypass switch feature of the MGA-72543 can be used to shut down the amplifier to conserve supply current during non-transmit periods. Supply current in the bypass state is nominally 2 µA.

Biasing

Biasing the MGA-72543 is similar to biasing a discrete GaAs FET. Passive biasing of the MGA-72543 may be accomplished by either of two conventional methods, either by biasing the gate or by using a source resistor.

• Gate Bias.

Using this method, Pins 1 and 4 of the amplifier are DC grounded and a negative bias voltage is applied to Pin 3 as shown in Figure 2. This method has the advantage of not only DC, but also RF grounding both of the ground pins of the MGA-72543. Direct RF grounding of the device's ground pins results in slightly improved performance while decreasing potential instabilities, especially at higher frequencies. The disadvantage is that a negative supply voltage is required.

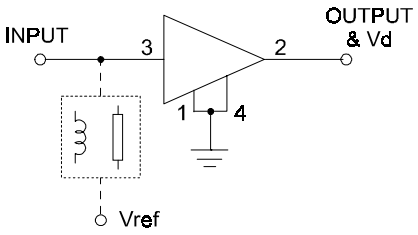


Figure 2. Gate Bias Method.

DC access to the input terminal for applying the gate bias voltage can be made through either a RFC or high impedance transmission line as indicated in Figure 2.

The device current, I_d, is determined by the voltage at V_{ref} (Pin 3) with respect to ground. A plot of typical I_d vs. V_{ref} is shown in Figure 3. Maximum device current (approximately 65 mA) occurs at $V_{ref} = 0$.

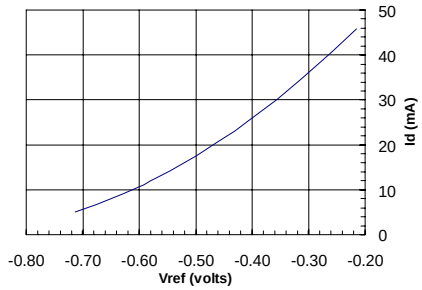


Figure 3. Device Current vs. V_{ref}.

The device current may also be estimated from the following equation:

$$V_{ref} = 0.11\sqrt{I_d} - 0.96$$

where I_d is in mA and V_{ref} is in volts.

The gate bias method would not normally be used unless a negative supply voltage was readily available. For reference, this is the method used in the characterization test circuits shown in Figures 1 and 2 of the MGA-72543 data sheet.

• Source Resistor Bias.

The source resistor method is the simplest way of biasing the MGA-72543 using a single, positive supply voltage. This method, shown in Figure 4, places the RF Input (Pin 3) at DC ground and requires both of the device grounds (Pins 1 and 4) to be RF bypassed. Device current, I_d, is determined by the value of the source resistance, R_{bias}, between either Pin 1 or Pin 4 of the MGA-72543 and DC ground. Note: Pins 1 and 4 are connected internally in the RFIC. Maximum device current (approximately 65 mA) occurs for $R_{bias} = 0$.

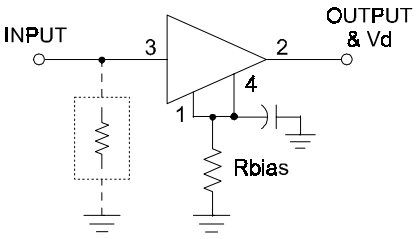


Figure 4. Source Resistor Bias.

A simple method recommended for DC grounding the input terminal is to merely add a resistor from Pin 3 to ground, as shown in Figure 4. The value of the shunt R can be comparatively high since the only voltage drop across it is due to minute leakage currents that in the µA range. A value of 1 KΩ would adequately DC ground the input while loading the RF signal by only 0.2 dB loss.

A plot of typical I_d vs. R_{bias} is shown in Figure 5.

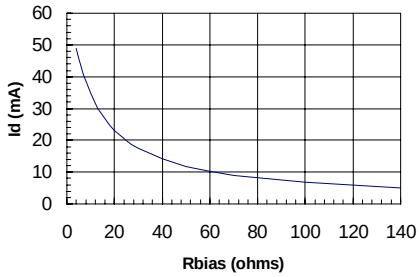


Figure 5. Device Current vs. R_{bias}.

The approximate value of the external resistor, R_{bias}, may also be calculated from:

$$R_{bias} = \frac{964}{I_d}(1-0.112\sqrt{I_d})$$

where R_{bias} is in ohms and I_d is the desired device current in mA.

The source resistor technique is the preferred and most common method of biasing the MGA-72543.

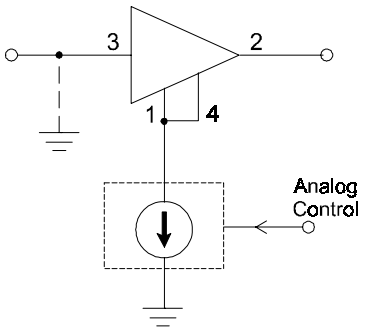
• Adaptive Biasing.

For applications in which input power levels vary over a wide range, it may be useful to dynamically adapt the bias of the MGA-72543 to match the signal level. This involves sensing the signal level at some point in the system and automatically adjusting the bias current of the amplifier accordingly. The advantage of adaptive biasing is conservation of supply current (longer battery life) by using only the amount of current necessary to handle the input signal without distortion.

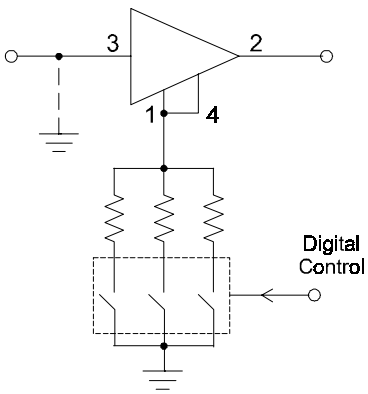
Adaptive biasing of the MGA-72543 can be accomplished by either analog or digital means. For the analog control case, an active current source (discrete device or IC) is used in lieu of the source bias resistor. For simple digital control, electronic switches can be used to control the value of the source resistor in discrete increments. Both methods of adaptive biasing are depicted in Figure 6.

• Applying the Device Voltage.

Common to all methods of biasing, voltage V_d is applied to the MGA-72543 through the RF Output connection (Pin 2). A RF choke is used to isolate the RF signal from the DC supply. The bias line is capacitively bypassed to keep RF from the DC supply lines and prevent resonant dips or peaks in the response of the amplifier. Where practical, it may be cost effective to use a length of high impedance transmission line (preferably $\lambda/4$) in place of the RFC.



(a) Analog



(b) Digital

Figure 6. Adaptive Bias Control.

When using the gate bias method, the overall device voltage is equal to the sum of V_{ref} at Pin 1 and voltage V_d at Pin2. As an example, to bias the device at the typical operating voltage of 3 volts, V_d would be set to 2.5 volts for a V_{ref} of -0.5 volts. Figure 7 shows a DC schematic of a gate bias circuit.

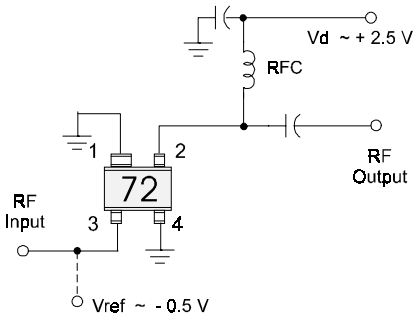


Figure 7. DC Schematic for Gate Bias.

Just as for the gate bias method, the overall device voltage for source resistor biasing is equal to $V_{ref} + V_d$. Since V_{ref} is zero when using a source resistor, V_d is the same as the device operating voltage, typically 3 volts. A source resistor bias circuit is shown in Figure 8.

A DC blocking capacitor at the output of the RFIC isolates the supply voltage from succeeding circuits. If the source resistor method of biasing is used, the RF input terminal of the MGA-72543 is at DC ground potential and a blocking capacitor is not required unless the input is connected

directly to a preceding stage that has a DC voltage present.

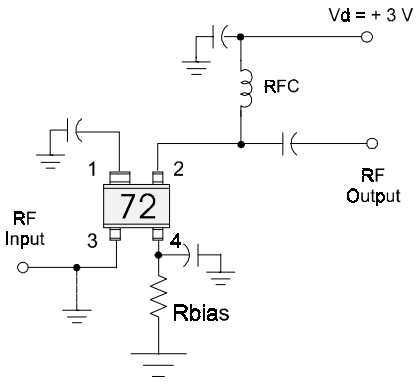


Figure 8. DC Schematic of Source Resistor Biasing.

• Biasing for Higher Linearity or Output Power

While the MGA-72543 is designed primarily for use up to 50 mA in +3 volt applications, the output power can be increased by using higher currents and/or higher supply voltages. If higher bias levels are used, appropriate caution should be observed for both the thermal limits and the Absolute Maximum Ratings.

As a guideline for operation at higher bias levels, the Maximum Operating conditions shown in the data sheet table of Absolute Maximum Ratings should be followed. This set of conditions is the maximum combination of bias voltage, bias current, and device temperature that is recommended for reliable operation. Note: In contrast to Absolute Maximum ratings, in which exceeding any *one* parameter may result in damage to the device, *all* of the Maximum Operating conditions may reliably be applied to the MGA-72543 *simultaneously*.

Controlling the Switch

The state of the MGA-72543 (amplifier or bypass mode) is controlled by the device current. For device currents greater than 5 mA, the MGA-72543 functions as an amplifier. If the device current is set to zero, the MGA-72543 is switched into a bypass mode in which the amplifier is turned off and the signal is routed around the amplifier with a loss of approximately 2.5 dB.

The bypass state is normally engaged in the presence of high input levels to prevent distortion of the signal that might occur in the amplifier. In the bypass state, the input TOI is very high, typically +39 dBm at 1900 MHz.

The simplest method of placing the MGA-72543 into the bypass mode is to open-circuit the ground terminals at Pins 1 and 4. With the ground connection open, the internal control circuit of the MGA-72543 auto-switches from the amplifier mode into a bypass state and the device current drops to near zero. Nominal current in the bypass state is 2 μA with a maximum of 15 μA.

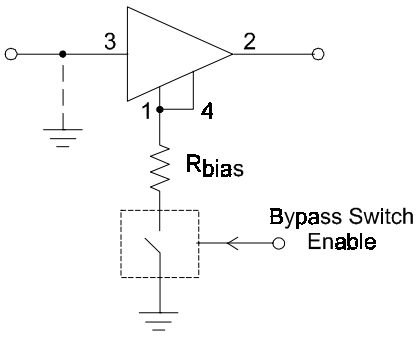


Figure 9. MGA-72543 Amplifier/ Bypass State Switching.

An electronic switch can be used to control states as shown in Figure 9. The control switch could be implemented with either a discrete transistor or simple IC.

The speed at which the MGA-72543 switches between states is extremely fast and will normally be limited by the time constants of external circuit components, such as the bias circuit and the bypass and blocking capacitors.

The input and output of the MGA-72543 while in the bypass state are internally matched to 50 Ω. The input return loss can be further improved at 1900 MHz by adding a 2.7 to 3.9 nH series inductor added to the input. This is the same approximate value of inductor that is used to improve input match when the MGA-72543 is in the amplifier state.

Thermal Considerations

Good thermal design is always an important consideration in the reliable use of any device, since the Mean Time To Failure (MTTF) of semiconductors is inversely proportional to the operating temperature.

The MGA-72543 is a comparatively low power dissipation device and, as such, operates at conservative temperatures. When biased at 3 volts and 20 mA for LNA applications, the power dissipation is 3.0 volts × 20 mA, or 60 mW. The temperature increment from the RFIC channel to its case is then 0.060 watt × 200° C/watt, or only 12° C. Subtracting the channel-to-case temperature rise from the suggested maximum junction temperature of 150° C, the resulting maximum allowable case temperature is 138° C.

The worst case thermal situation occurs when the MGA-72543 is operated at its Maximum Operating conditions in an effort to maximize output power or achieve

minimum distortion. A similar calculation for the Maximum Operating bias of 4.2 volts and 60 mA yields a maximum allowable case temperature of 100° C. This calculation further assumes the worst case of no RF power being extracted from the device. When operated in a saturated mode, both power-added efficiency and the maximum allowable case temperature will increase.

Note: "Case" temperature for surface mount packages such as the SOT-343 refers to the interface between the package pins and the mounting surface, i.e., the temperature at the PCB mounting pads. The primary heat path from the RFIC chip to the system heatsink is by means of conduction through the package leads and ground vias to the groundplane of the PCB.

PCB Layout and Grounding

When laying out a printed circuit board for the MGA-72543, several points should be considered. Of primary concern is the RF bypassing of the ground terminals when the device is biased using the source resistor method.

• Package Footprint

A suggested PCB pad print for the miniature, 4-lead SOT-343 (SC-70) package used by the MGA-72543 is shown in Figure 10.

This pad print provides allowance for package placement by automated assembly equipment without adding excessive parasitics that could impair the high frequency performance of the MGA-72543. The layout is shown with a footprint of the MGA-72543 superimposed on the PCB pads for reference.

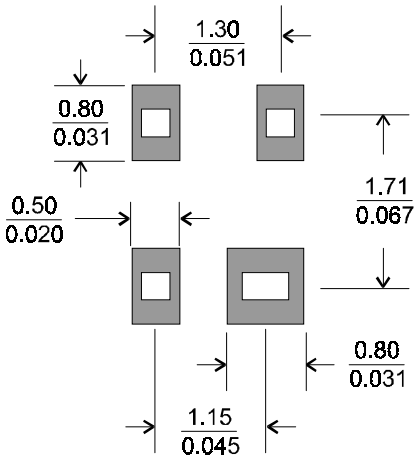


Figure 10. PCB Pad Print for SOT-343 Package (mm/inches).

• RF bypass

For layouts using the source resistor method of biasing, both of the ground terminals of the MGA-72543 must be well bypassed to maintain device stability.

Beginning with the package pad print in Figure 10, an RF layout similar to the one shown in Figure 11 is a good starting point for using the MGA-72543 with capacitor-bypassed ground terminals. It is a best practice to use multiple vias to minimize overall ground path inductance.

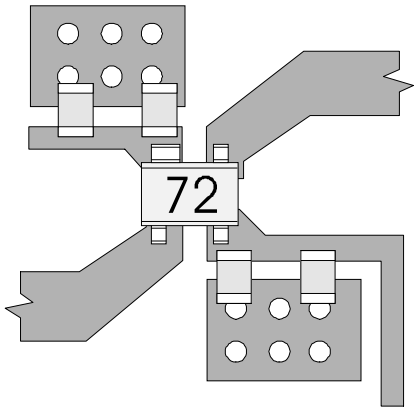


Figure 11. Layout for RF Bypass.

Two capacitors are used at each of the PCB pads for both Pins 1 and 4. The value of the bypass capacitors is a balance between providing a small reactance for good RF grounding, yet not being so large that the capacitor's parasitics introduce undesirable resonances or loss.

If the source resistor biasing method is used, a ground pad located near either Pin 1 or 4 pin may be used to connect the current-setting resistor (R_{bias}) directly to DC ground. If the R_{bias} resistor is not located immediately adjacent to the MGA-72543 (as may be the case of dynamic control of the device's linearity), then a small series resistor (e.g., 10 Ω) located near the ground terminal will help de-Q the connection from the MGA-72543 to an external current-setting circuit.

• PCB Materials

FR-4 or G-10 type dielectric materials are typical choices for most low cost wireless applications using single or multilayer printed circuit boards. The thickness of single-layer boards usually range from 0.020 to 0.031 inches. Circuit boards thicker than 0.031 inches are not recommended due to excessive inductance in the ground vias.

Application Example

An example evaluation PCB layout for the MGA-72543 is shown in Figure 12. This evaluation circuit is designed for operation from a +3-volt supply and includes provision for a 2-bit DIP switch to set the state of the MGA-72543. For evaluation purposes, the 2-bit switch is used to set the device to either of four states: (1) bypass mode – switch bypasses the amplifier, (2) low noise amplifier mode – low bias current, (3) and (4) driver amplifier modes – high bias currents.

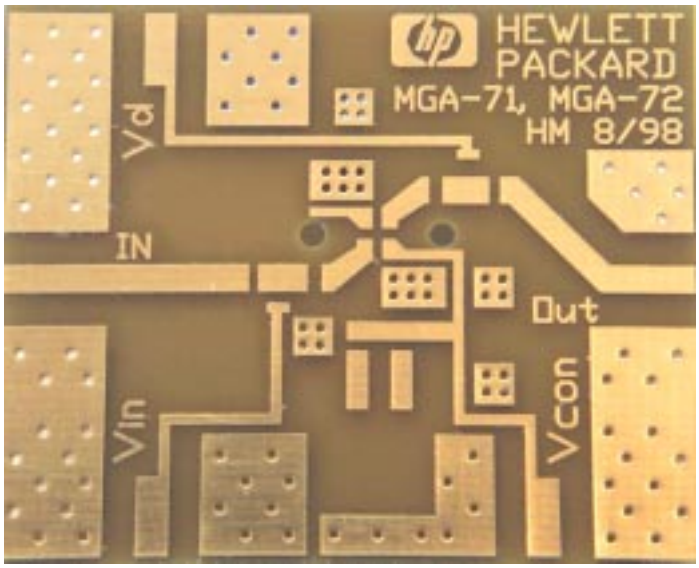


Figure 12. PCB Layout for Evaluation Circuit.

A completed evaluation amplifier optimized for use at 1900 MHz is shown with all related components and SMA connectors in Figure 13. A schematic diagram of the evaluation circuit is shown in Figure 14 with component values in Table 1.

The on-board resistors R3 and R4 form the equivalent source bias resistor R_{bias} as indicated in the schematic diagram in Figure 14. In this example, resistor values of R3 = 10 Ω and R4 = 24 Ω were chosen to set the nominal device current for the four states to: (1) bypass mode, 0 mA, (2) LNA mode, 20 mA, (3) driver, 35 mA, and, (4) driver, 40 mA.

Other currents can be set by positioning the DIP switch to the bypass state and adding an external bias resistor to V_{con}. Unless an external resistor is used to set the current, the V_{con} terminal is left open. DC blocking capacitors are provided for the both the input and output.

The 2-pin, 0.100" centerline single row headers attached to the V_d and V_{con} connections on the PCB provide a convenient means of making connections to the board using either a mating connector or clip leads.

A Note on Performance

Actual performance of the MGA-72543 as measured in an evaluation circuit may not exactly match the data sheet specifications. The circuit board material, passive components, RF bypasses, and connectors all introduce losses and parasitics that degrade device performance.

For the evaluation circuit above, fabricated on 0.031-inch thick GETEK[1] G200D (εr = 4.2) dielectric material, circuit losses of about 0.3 dB would be expected at both the input an output sides of the RFIC at 1900 MHz. Measured noise figure (3volts, 20 mA bias) would then be approximately 1.8 dB and gain 13.8 dB.

[1] General Electric Co.

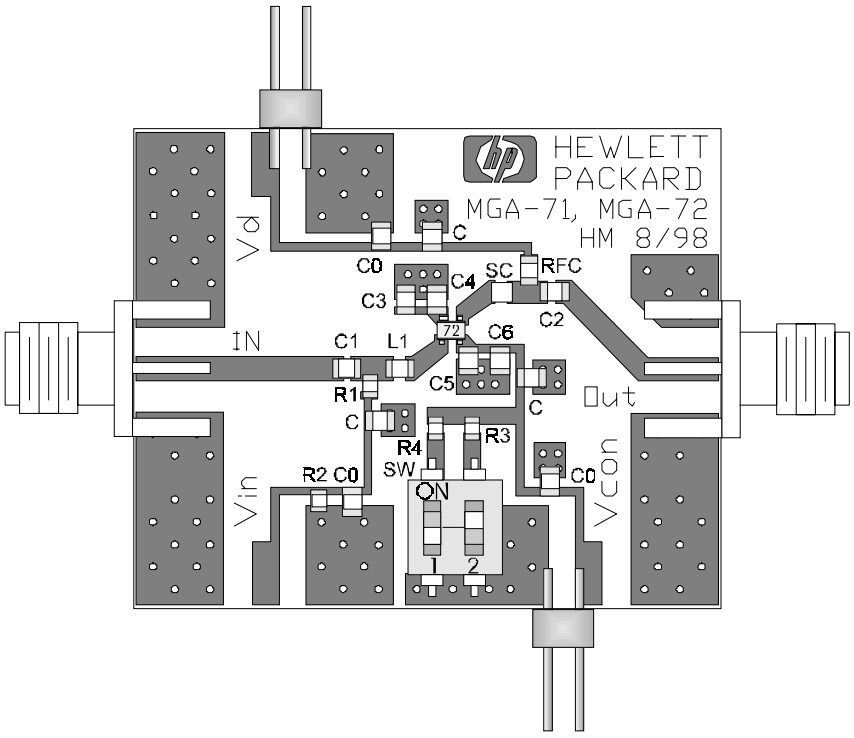


Figure 13. Completed Amplifier with Component Reference Designators.

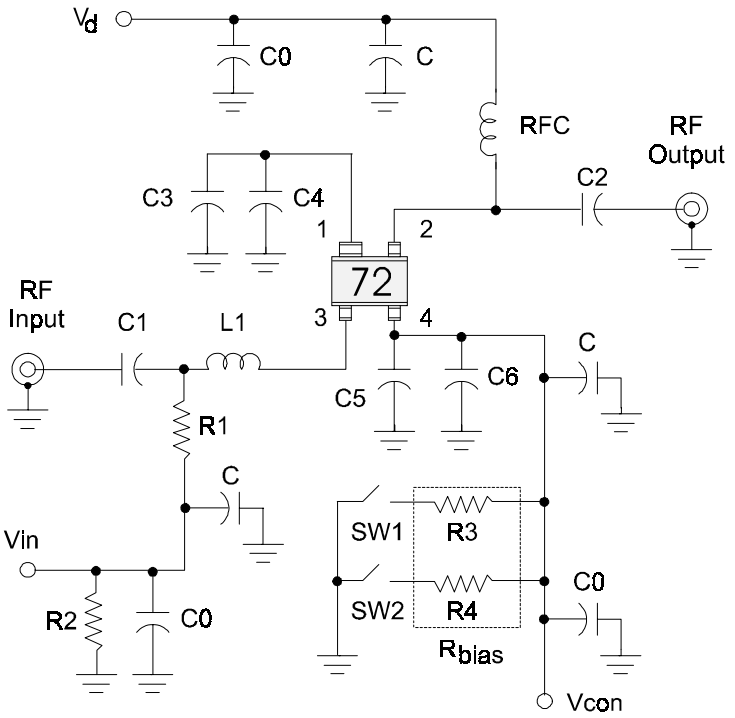


Figure 14. Schematic Diagram of 1900 MHz Evaluation Amplifier

R1	= 5.1 KΩ	C (3 ea)	= 100 pF
R2	= 5.1 KΩ	C0 (3 ea)	= 1000 pF
R3	= 10 Ω	C1	= 47 pF
R4	= 24 Ω	C2	= 47 pF
L1	= 3.9 nH	C3	= 30 pF
RFC	= 22 nH	C4	= 22 pf
SW1, SW2	DIP switch	C5	= 22 pf
SC	Short	C6	= 30 pF

Table 1. Component Values for 1900 MHz Amplifier.

Hints and Troubleshooting

• Preventing Oscillation

Stability of the MGA-72543 is dependent on having very good RF grounding. Inadequate device grounding or poor PCB layout techniques could cause the device to be potentially unstable.

Even though a design may be unconditionally stable (K > 1 and B1 > 0) over its full frequency range, other possibilities exist that may cause an amplifier circuit to oscillate. One condition to check for is feedback in the bias circuit. It is important to capacitively bypass the connections to active bias circuits to ensure stable operation. In multistage circuits, feedback through bias lines can also lead to oscillation.

Components of insufficient quality for the frequency range of the amplifier can sometimes lead to instability. Also, component values that are chosen to be much higher in value than is appropriate for the application can present a problem. In both of these cases, the components may have reactive parasitics that make their impedances very different than expected. Chip capacitors may have excessive inductance, or chip inductors can exhibit resonances at unexpected frequencies.

• A Note on Supply Line Bypassing

Multiple bypass capacitors are normally used throughout the power distribution within a wireless system. Consideration should be given to potential resonances formed by the combination of these capacitors and the inductance of the DC distribution lines. The addition of a small value resistor in the bias supply line between bypass capacitors will often de-Q the bias circuit and eliminate resonance effects.

Statistical Parameters

Several categories of parameters appear within the electrical specification portion of the MGA-72543 data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on a statistically significant number of parts taken from nonconsecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard bell curve.

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the MGA-72543, these parameters are: $V_{c\ test}$, NF_{test}, $G_{a\ test}$, $IIP_{3\ test}$, and IL_{test}. Each of the guaranteed parameters is 100% tested as part of the normal manufacturing and test process.

Values for most of the parameters in the table of Electrical

Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the center of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate amplifier circuit using the MGA-72543, but to also evaluate and optimize trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specification parameters (at 25°C). The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 15 for example, the probability of a parameter being between ±1σ is 68.3%; between ±2σ is 95.4%; and between ±3σ is 99.7%.

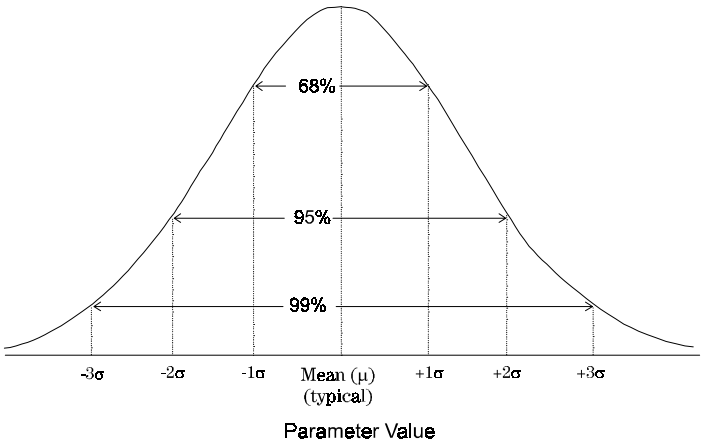


Figure 15. Normal Distribution Curve.

Phase Reference Planes

The positions of the reference planes used to specify S-parameters and Noise Parameters for the MGA-72543 are shown in Figure 16. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

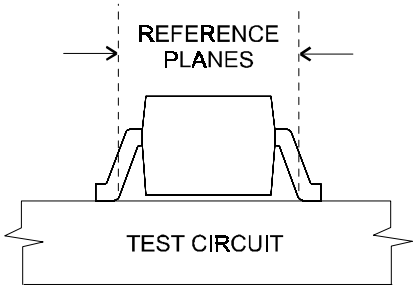


Figure 16. Phase Reference Planes.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-343 package, will reach solder reflow temperatures faster than those with a greater mass.

The MGA-72543 is has been qualified to the time-temperature profile shown in Figure 17. This profile is representative of an IR reflow type of surface mount assembly process. After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for the MGA-72543. As a general guideline, the circuit board and components should only be exposed to the minimum temperatures an times necessary to achieve a uniform reflow of solder.

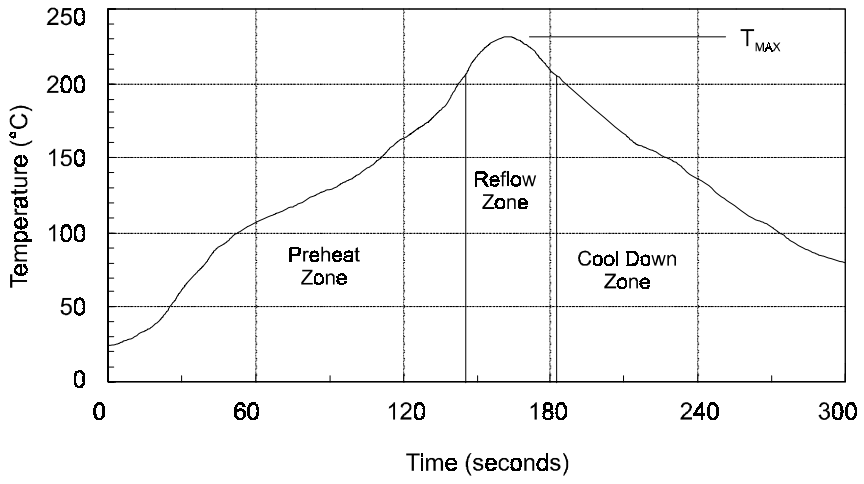


Figure 17. Surface Mount Assembly Profile.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the MGA-72543 is robust in design, permanent damage may occur to these devices if they are subjected to high-energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in failure or degradation in performance and reliability.

Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage & handling
- Inspection
- Assembly & testing
- In-circuit use

The MGA-72543 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

Any user-accessible points in wireless equipment (e.g., antenna or battery terminals) provide an opportunity for ESD damage.

For circuit applications is which the MGA-72543 is used as an input or output stage with close coupling to an external antenna, the RFIC should be protected from high voltage spikes due to human contact with the antenna.

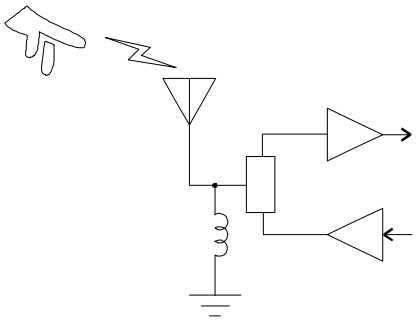


Figure 18. In-circuit ESD protection.

A best practice, illustrated in Figure 18, is to place a shunt inductor (RFC) at the antenna connection to protect the receiver and transmitter circuits. It is often advantegous to integrate the RFC into a diplexer or T/R switch control circuitry.

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or 408-654-8675

Far East/Australasia: Call your local HP sales office.

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