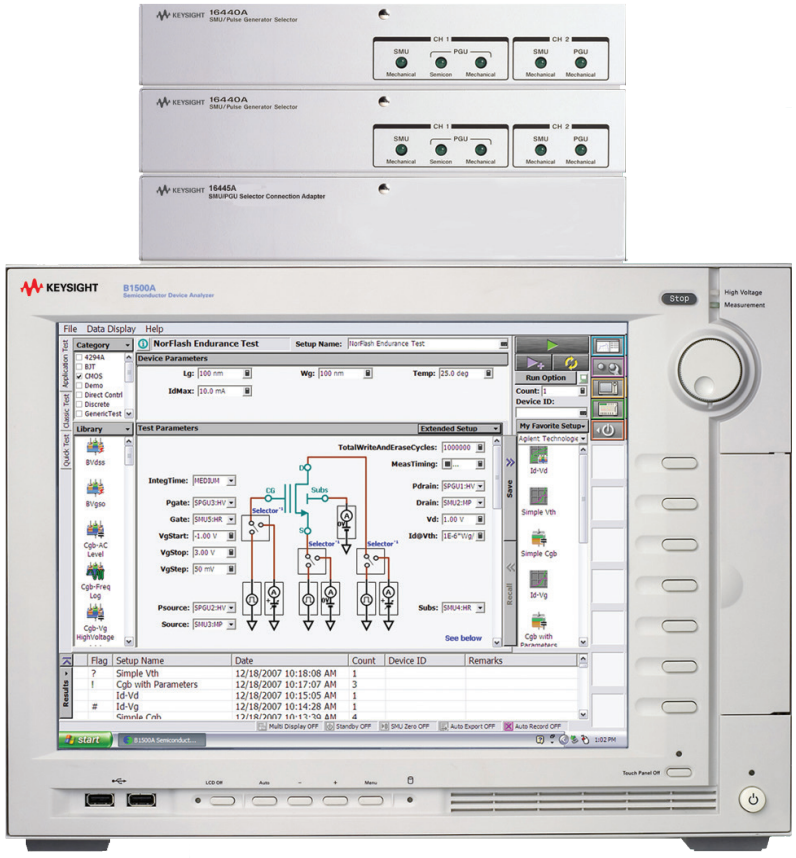
Keysight Technologies

Improving Flash Memory Cell Characterization Using the Keysight B1500A

Application Note



KEYSIGHT TECHNOLOGIES

Introduction

- HV-SPGU outputs ±40 V three level pulses
- One million write/erase cycle endurance test can be performed within an hour
- More than twenty flash memory test applications are ready to use for fast start-up
- ALWG function enables the novel non-volatile memory test

The flash memory market is growing rapidly, driven by MP3 music players, digital camera storage media and the expectation of replacing smaller hard disk drives in the near future. Accompanying this growth is the need to increase memory sizes by reducing the memory cell area through such means as multi-bit or multilevel cell (MLC) and charge trap flash memory. The write/erase characterization of these modern high-density NAND flash memory processes presents many new measurement challenges, such as the generation of extremely accurate voltage pulses and the creation of arbitrary waveforms.

The Keysight Technologies, Inc. B1500A Semiconductor Device Analyzer's new Keysight B1525A High Voltage Semiconductor Pulse Generator Unit (HV-SPGU) provides the accuracy and flexibility to meet the write/erase testing needs of these advanced non-volatile memory technologies. In addition, the B1500A and HV-SPGU offer substantial throughput improvements for write/erase cycle endurance lifetime testing. This application note explains how the B1500A can meet all of these exacting challenges and requirements.

B1500A Flash Memory Test Key Features

The key features of the B1500A flash testing solution include:

- High voltage pulsing capability
  The HV-SPGUs can output ±40 V (80 V peak-to-peak) with a programmable rise/fall time from 20 ns[1] to 400 ms, which meets the needs of modern NAND flash memory cell testing. (See Figure 1).
- High resolution voltage forcing capability
  The output waveforms can be programmed with 0.4 mV resolution, which provides a stable and clean pulse waveform required for evaluating the multi-level flash memory cell technologies.
- Fast open drain semiconductor output switch.
  The pulse switch used to create an open drain status necessary in the erase cycle of a NOR flash cell can respond within 100 µs, which reduces the total test time required to complete a write/erase endurance lifetime test. A simplified schematic image of the HV-SPGU outputs is shown in Figure 2.

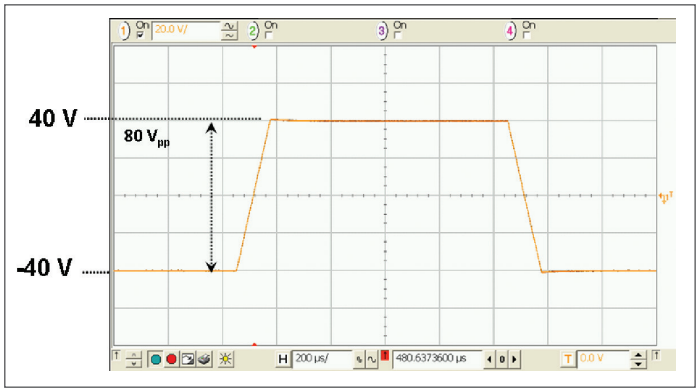


Figure 1. The HV-SPGU has ±40 V output capability

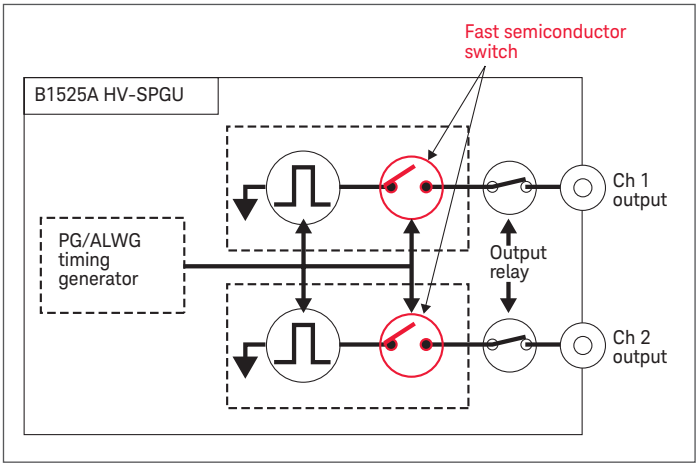


Figure 2. The B1525A HV-SPGU module has two channels, each of which has a fast semiconductor switch in the output path

1. The minimum rise and fall times are 20 ns when |Vamp| ≤ 10 V and 30 nsec when 10 V <|Vamp| ≤ 20 V; both of these cases are for a 50 Ω load.
   Vamp = Amplitude of the pulse.

B1500A Flash Memory Test Key Features (continued)

- Three level pulses
  Each HV-SPGU module has two independent SPGU channels that can each output two or three level pulses (Figure 3). Three level pulses are necessary in NAND flash memory cell testing, and the fast pulse train that can be created without requiring two PGU channels dramatically improves the NAND endurance lifetime test throughput.
- Flash memory test application library
  Twenty new application test definitions for evaluating both NAND and NAND type flash memory cells using the HV-SPGU have been added to the EasyEXPERT memory test application library as shown below:
  - Endurance test
  - Erase and Vth test
  - Write and Vth test
  - Retention test after Erase
  - Retention test after Write
  - Vth and Erasing Time Dependence
  - Vth and Writing Time Dependence
  - Word Disturb test on Erased Cell
  - Word Disturb test on Written Cell
  - Nor Flash Data Disturb test after Erase
  - Nor Flash Data Disturb test after Write

These test definitions can be selected from the EasyEXPERT graphical user interface (GUI, see Figure 4) and can be executed with a few mouse clicks after setting up the test parameters.

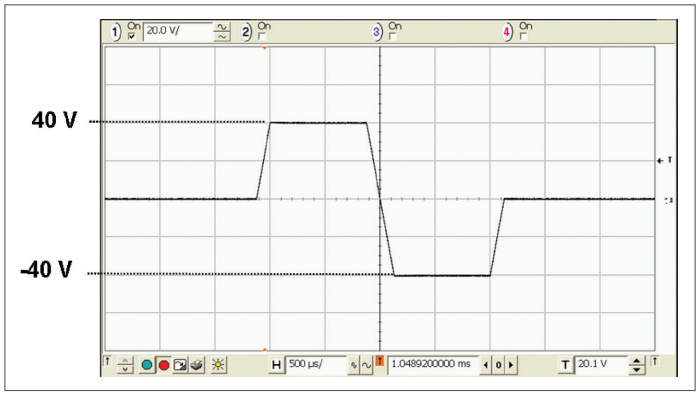


Figure 3. The HV-SPGU can output three-level pulses with ±40 V output swings

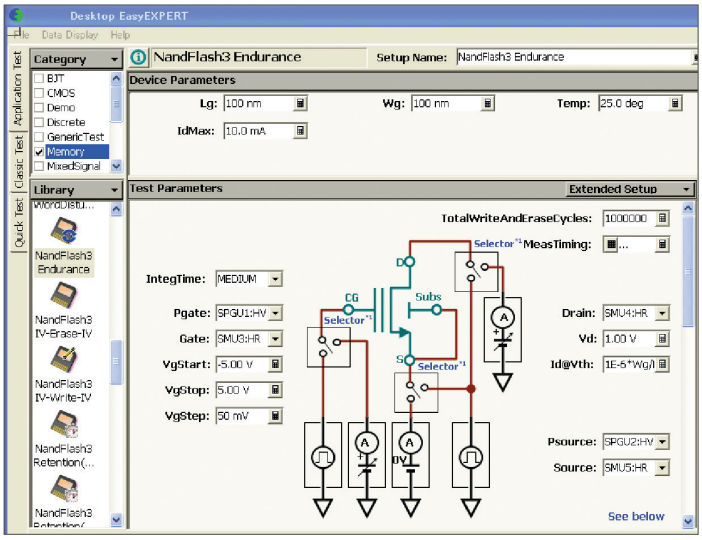


Figure 4. EasyEXPERT flash memory test setup screen example

B1500A Endurance Lifetime Test

This section introduces how flash memory cell testing is performed and improved by using the B1500A.

Performing endurance lifetime testing on the B1500A

Figure 5 shows the typical flow for a flash memory cell write/erase cycle endurance lifetime test. The test begins by first measuring the unstressed memory cell's written and erased Vth to establish a baseline. The test will then perform a series of logarithmically increasing write and erase burst cycles on the cell, measuring the written and erased Vth after the completion of each burst cycle. The number of burst cycles performed depends upon the number of write and erase cycles specified in the test's input parameters. After three write and erase burst cycles the test will plot the written and erased Vth versus the number of write and erase cycles and display this graph as the test progresses. This permits the viewing of the Vth degradation in real time. After the user-specified number of burst cycles has been performed, the test ends and a final plot of Vth degradation is displayed. Figure 6 shows an example of the Vth shift of a NAND flash memory cell over one million write and erase stress cycles measured on a B1500A.

Even where the write and erase cycles are limited to ten thousand cycles as in a commercial specification, characterization of the memory cells in the development phase is usually made for longer periods, for example one million cycles as shown in Figure 6.

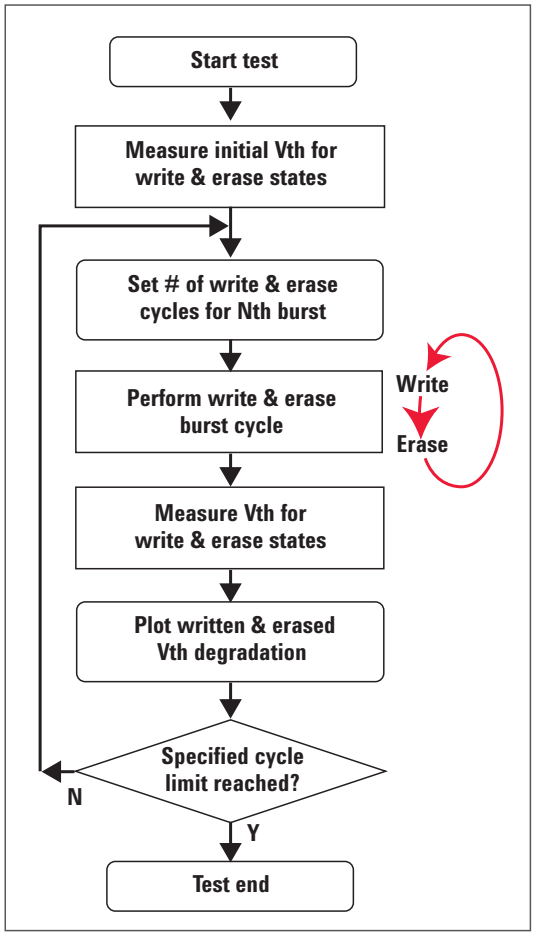


Figure 5. Test fl ow for a fl ash memory cell write/erase endurance lifetime test

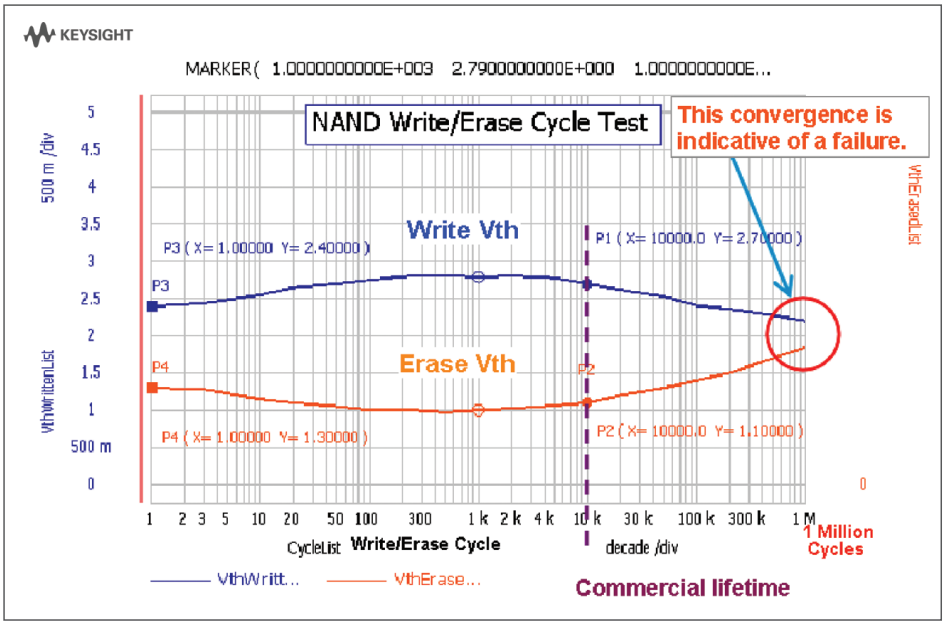


Figure 6. Example showing Vth shift as a result of write/erase endurance testing

B1500A Endurance Lifetime Test (continued)

Test progress monitoring

Figure 7 shows the B1500A test display when performing a NOR flash memory endurance test. The B1500A display shows the progress of the write and erase stress cycles, Vth measurements in write and erase status and the shift in Vth over the stress write/erase cycles.

Test setup

The B1500A library of flash memory application tests supports the Keysight 16440A SMU/PGU selector, which switches between SMUs for Vth measurements and HV-SPGUs for writing and erasing the memory cell. Figure 8 shows a simplified connection diagram for NOR flash memory test using the 16440A. The 16440A switch provides two important flash memory cell testing capabilities: (1) the ability to switch between the SMUs and HV-SPGUs and (2) a reasonable compromise between the high frequency bandwidth and low leakage DC performance that are both necessary for flash memory cell testing.

As can be seen from this example, the flash memory cell test can begin right away without the need to develop flash memory test programs on the B1500A.

Figure 7. Snapshot of B1500A write/erase endurance testing

1. Progress monitor (% of write/erase cycles completed)
2. Most recent written cell Vth measurement
3. Most recent erased cell Vth measurement
4. The progression of the Vth shift

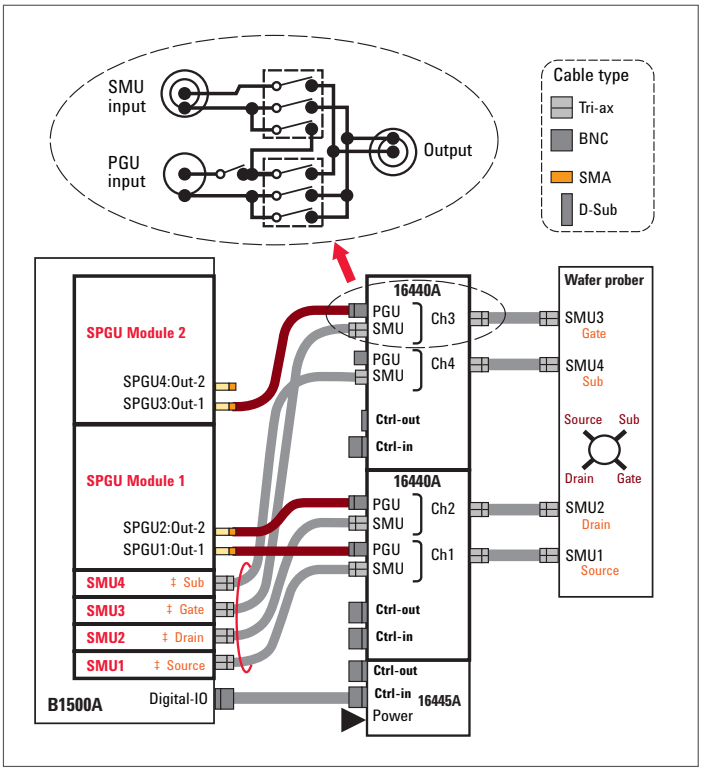


Figure 8. Simplified NOR flash memory cell connection diagram

B1500A Endurance Lifetime Test (continued)

NAND flash test requirements

For testing modern NAND flash memory cells, large voltage amplitude pulses and fast rise/fall times are essential. The B1525A HV-SPGU meets these needs with ±40 V (80 V peak-to-peak) pulse generation capability into a high impedance load (refer back to Figure 2) and a programmable pulse rise/fall time from 8 ns to 400 ms. However, pulse overshoot is also a major concern when testing flash memory cells, and the B1500A has solutions to address this issue.

Prior to the B1525A HV-SPGU, the available solutions for high-voltage pulsing with programmable rise/fall times have been limited (for example the two-channel PGU in the 41501B expander for the 4156C). However, the minimum pulse width of the 41501B PGU is limited to 1 µs.

The write/erase characteristics of flash memory cells are strongly dependent on the applied voltage. This means any overshoot in the write/erase pulse can adversely impact the flash cell characterization. Since modern NAND flash technologies require up to ±40 volt swings, eliminating pulse overshoot is a difficult challenge. Applying a pulse to a flash memory cell with extremely large (essentially open) input impedance in a 50 Ω environment creates an impedance mismatch. When combined with the SMU/HV-SPGU switch this mismatch creates an overshoot that would not be expected under ideal 50 Ω load conditions. A programmable rise/fall time capability is one means to overcome this issue, since increasing the rise/fall time is the fundamental way to eliminate the pulse overshooting and ringing under the high impedance load condition that is typical in flash memory cell testing.

Figure 9 shows a typical write/erase pulse setup for NAND flash memory cell testing. It requires high voltage and three level pulses on one channel to write and erase the memory cell.

Pulse waveform through 16440A SMU/PGU switch

Figure 10 shows a sample pulse waveforms routed through the 16440A and 1.5 m of triaxial cable going into a 1 MΩ oscilloscope input. The rise and fall time vary from 14 ns to 60 ns. The pulse with 14 ns rise time shows considerable overshoot, but increasing the pulse transition time shows clearly that the overshoot is reduced. The overshoot becomes negligibly small at 40 ns rise or fall transition time and it almost disappears at 60 ns pulse transition time setting (refer the enlarged image in Y scale shown in the rectangular frame). As Figure 10 demonstrates, the overshoot introduced when a pulse signal is routed through a bandwidth limited component like the 16440A SMU/PGU selector can be almost eliminated by increasing the pulse transition time.

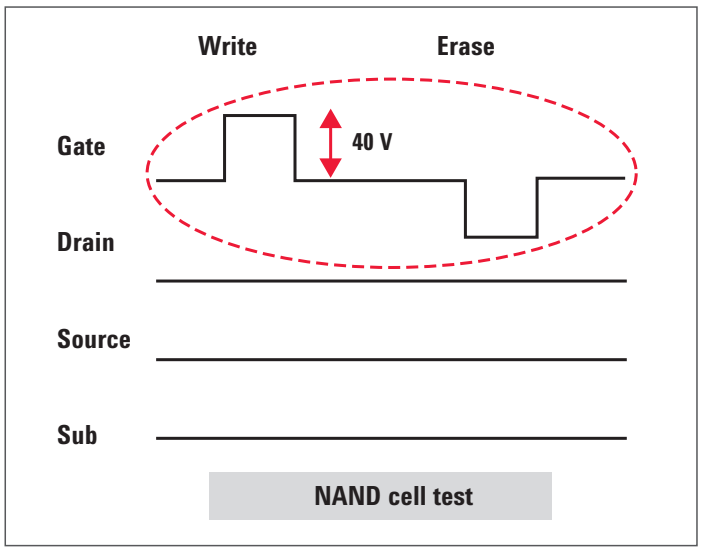


Figure 9. NAND flash memory cell write and erase pulse sequence

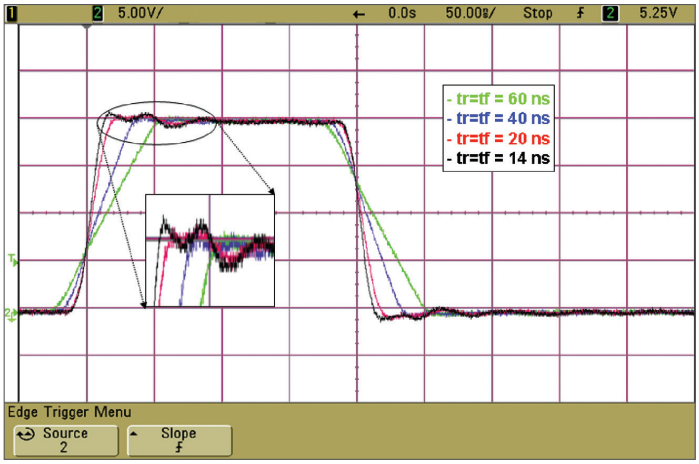


Figure 10. Example showing how varying the rise and fall times on a 200 ns/20V pulse passing through the 16440A and into a 1 MΩ (open) load can impact overshoot

B1500A Endurance Lifetime Test (continued)

Pulse waveform through 16440A SMU/PGU switch (continued)

The 16440A SMU/PGU switch is the most cost-effective solution that supports both high-speed pulses (less than 5% overshoot for 20 ns rise/fall time pulse) and precise dc measurements (less than 100 fA leakage at 100 V) for flash memory test.

NOR flash memory cell test

Figure 11 shows typical write/erase pulses for NOR flash memory cells. Erasing the memory cell typically requires the drain connection to be set to an open or high impedance state. The HV-SPGU meets this need with a high speed semiconductor relay. The B1500A can contain a maximum of five two-channel HV-SPGU modules (Figure 12). This example uses three channels, so two B1525A HV-SPGU modules are needed.

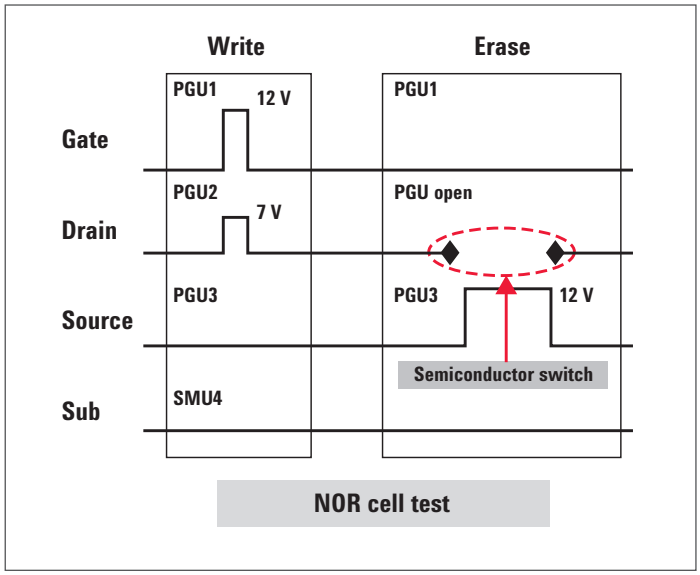


Figure 11. NOR flash memory cell write and erase pulse sequence

Figure 12. Each HV-SPGU module has two independent channels

Faster hardware dramatically accelerates flash memory cell write/erase endurance testing

The following two new HV-SPGU features significantly improve the test time.

1. The HV-SPGUs generate write/erase test patterns internally without any interaction of test sequence control from the central computer. This eliminates a lot of overhead time that slows down flash memory cell write/erase test cycling in older solutions utilizing the Keysight 81110A or the 41501B PGUs.
2. As shown in the HV-SPGU functional diagram in Figure 2, a built-in fast semiconductor switch is available to create an open state to the DUT. The switch is controlled at the firmware (machine) level and synchronized with pulse streams being used to write or erase a flash memory cell. The transition time of the switch from close to open state (or vice versa) is less than 100 µs.

For a one million cycle write/erase endurance test on a NOR flash memory cell with a write/erase cycle of approximately two milliseconds, a rough calculation shows that the endurance test can be finished within 2,000 seconds (2 ms x 106). Of course, this calculation excludes the Vth measurement time in-between the write/erase cycles.

B1500A Endurance Lifetime Test (continued)

Improvement of endurance lifetime cycle test time

The time required to complete endurance lifetime cycle test on a flash memory cell largely depends on how fast the write/erase stress cycle can be performed.

The following example shows a comparison of the test times for a one million write and erase endurance test performed on the 4156C based flash memory solution and the B1500A.

Figure 13 shows the write/erase pulse trains in the 4156C case. It uses two PGUs of the Keysight 41501B SMU and PGU expander box (only one PGU module with 2 PGU channels is available in the case of the 4156C) to the drain and gate, and one SMU is assigned as the source pulse. Since the erase pulse is on the order of milliseconds, the 0.5 ms minimum SMU pulse can be used in place of a pulse generator. The open drain state is implemented by using the semiconductor relay of the 16440A in the case of the 4156C. In the case of the 4156C, each write and erase pulse and open drain condition in the erase cycle have to be controlled at the application software level, which takes about 250 ms for creating each write and erase pulse. In contrast to the 4156C, the B1500A controls all pulse trains at the firmware level and all pulse trains can be controlled in less than one hundred nano-seconds except for the semiconductor relay control.

Table 1 summarizes the test speed comparison data for a one million write and erase endurance test for both NAND and NOR flash memory cells using the 4156C and B1500A. We used the following write/erase cycle times in the example: 2 milliseconds for NAND and 25 milliseconds for NOR flash memory cell. The cycle times are conservative, but most users will see at least a 5x cycle time improvement or obtain a test time of less than one hour when using the B1500A and HV-SPGU solution.

A test speed comparison video between the B1500A and 4156C is available on the Keysight web page shown in the back page of this application note.

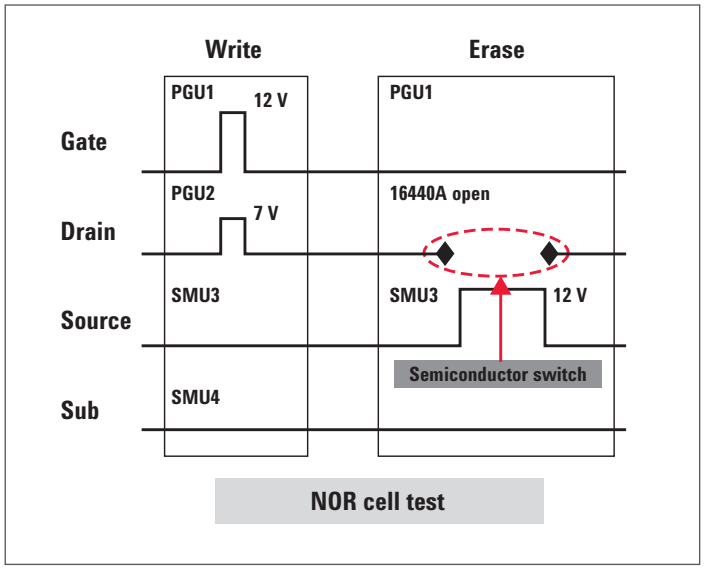


Figure 13. 4156C + 41501B PGU + 16440A based NOR flash cell write/erase pulse sequence

Table 1. Test speed comparison between the 4156C and the B1500A for both NOR and NAND flash write/erase endurance testing

	NAND	NOR
4156C + 41501B PGU	5 days	4 days
B1500A + HV-SPGU	1.7 hours	6 hours

B1500A Endurance Lifetime Test (continued)

Additional key HV-SPGU features

The following sections highlight some additional key features of the B1525A HV-SPGU.

Improved pulse resolution, accuracy and repeatability meet the needs of multi-level cell flash memory test

More so than traditional flash memory cells, multi-level cell (MLC) flash memory require extremely accurate voltage pulses for writing and erasing to insure that the correct data bit is accessed. The B1500A addresses this need with vastly improved voltage pulse resolution.

Prior to the introduction of the HV-SPGU, the most accurate pulse generator supported by the B1500A was the Keysight 81110A pulse pattern generator. The output voltage pulse force resolution of the 81110A is 100 mV. However, the output pulse force resolution of the HV-SPGU in the B1500A is 0.4 mV, which represents more than a 100 times improvement in performance. Moreover, the accuracy and stability of the HV-SPGU's output voltage are also improved relative to that of the 81110A.

In summary, the high resolution, high accuracy, and high stability of the HV-SPGU ensure accurate and repeatable characterization of MLC flash memory cells.

Three-level pulsing capability

A three-level pulse as shown in Figure 3 is required to apply alternating write and erase pulsing to NAND flash memory cells. Unlike the other pulse generator such as the 41501B's PGU, each of the two channels on the HV-SPGU can independently generate three-level pulses. Moreover, the three levels can be selected arbitrarily anywhere from within the -40 V to +40V output range of the HV-SPGU. It is important to point out that the 41501B's PGU cannot output three level pulses as illustrated in Figure 3.

Accurate pulse timing between channels

Another important pulse generator capability is the ability to create accurate and synchronized write and erase pulse widths on multiple channels, even when the pulse widths differ by many orders of magnitude. This is due to the fact that generally the widths of write pulses are on the order of microseconds, while the widths of erase pulses are on the order of milliseconds.

Figure 14 shows an oscilloscope plot of a "typical" write and erase pulse sequence. The waveforms are generated by two different HV-SPGU channels, and consist of three-level write and erase pulses that vary from microseconds to milliseconds. The width of the first pulse on output channel one is 1 µs and the width of the second pulse on output channel one is 1 ms. The width of the first pulse on output channel two is 800 ns and the width of the second pulse on output channel two is 800 µs. From this figure it is easy to see that the write and erase pulses are well synchronized even though the write and erase pulse widths on the two channels are vastly different.

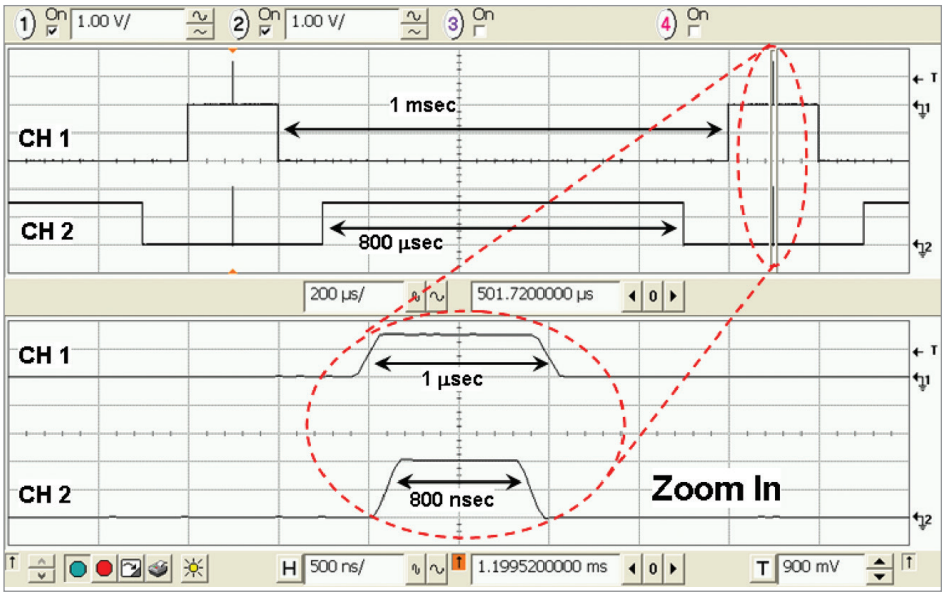


Figure 14. The HV-SPGU exhibits excellent synchronization between the write and erase pulses

Complex Waveform Synthesis Capability for Testing Novel Memory Devices

The new arbitrarily linear waveform generator (ALWG) function available on the HV-SPGU can create complicated pulse sequences required for the characterization of novel non-volatile memory technologies such as charge trap flash memory. ALWG waveforms consist of waveform patterns and their combinations as shown in Figure 15. Each waveform pattern consists of a combination of line segments, and the time between the points can be specified from 10 ns to 671.08863 ms with 10 ns resolution. The output ordering and repetition of each stored waveform pattern can be arbitrarily specified to create the desired output sequence.

Each ALWG pattern can be created by using the ALWG pattern editor GUI (Figure 16) or by copying data from a table created on a spreadsheet.

Figure 17 shows the oscilloscope trace of an example waveform created by using the ALWG editor. As this figure shows, you can combine and repeat all patterns created in the ALWG editor. This permits the easy synthesis of complicated waveforms.

One area where the ALWG function can be used to reduce write/erase endurance test times is MLC flash memory. MLC technology requires pulse steps with more than four levels, which can be easily realized by using the ALWG function with no overhead time penalties. Another application is to create small staircase pulses rather than one large pulse to prevent a sudden large current pulse that could damage a device, or to deactivate the damage caused by stress during the erase sequence on flash memory cells.

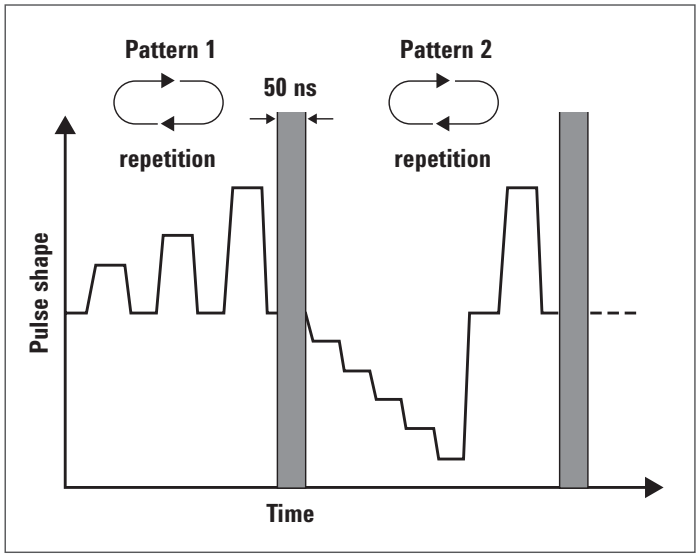


Figure 15. ALWG waveforms can be sequenced together and repeated multiple times

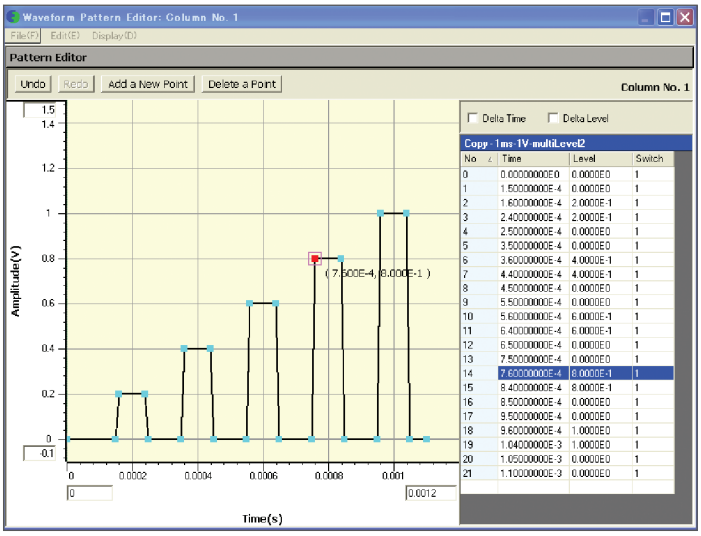


Figure 16. The ALWG pattern editor GUI supports both numeric and graphical waveform creation

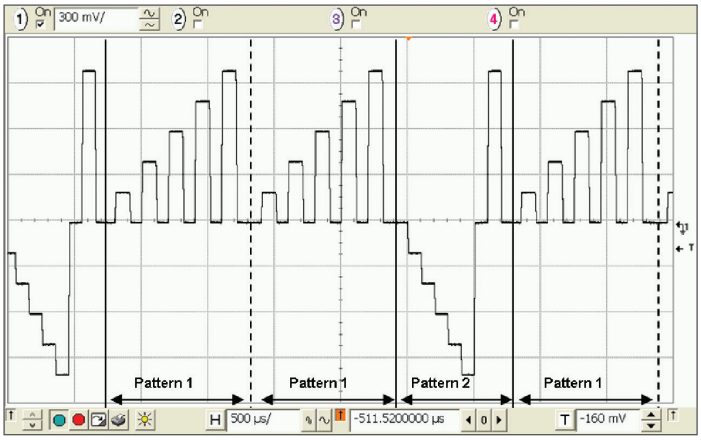


Figure 17. Oscilloscope trace showing how different ALWG patterns can be sequenced together

Summary

The new Keysight B1500A with B1525A HV-SPGU provides a complete solution for state-of-the-art flash memory cell technologies.

The ±40 V output capability of the HV-SPGUs meets the needs of modern NAND flash testing.

The 0.4 mV output force resolution of the HV-SPGU permits the characterization of voltage sensitive devices such as MLC flash memory.

The ultra-fast switching speeds of the semiconductor switches in the SPGU channels reduces the time for write and erase cycles, thereby shortening the NAND flash endurance test time dramatically. With two independent channels per HV-SPGU module (each capable of three-level pulses), the B1500A also provides both faster write/erase pulse streams as well as improved cost-effectiveness.

The ALWG function permits the creation of complex waveforms for characterizing novel new flash cell technologies.

Note:

Following flash memory test video is available at:

- B1500A Flash Testing Demo Video
- B1500A vs. 4156C Flash Testing Demo Video

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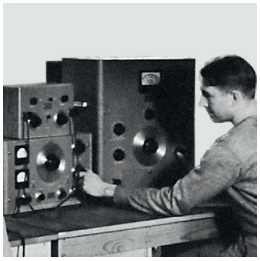

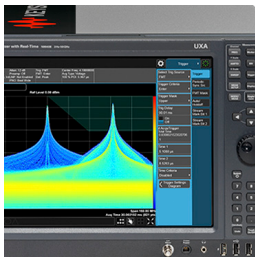

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