Using the Agilent B1500A with a Nanoprober to Perform Failure Analysis

Application Note B1500-7

Agilent B1500A Semiconductor Device Analyzer

Introduction

Recent advances in nanoprobers, which enable the probing of extremely small line widths, permit the electrical characterization of individual devices within an integrated circuit. This application note describes how to use the Agilent B1500A Semiconductor Device Analyzer to make these types of electrical measurements, using SRAM failure analysis to illustrate this technique.

In conventional memory failure analysis, the failed bit is detected by a logic tester and then a Scanning Electron Microscope (SEM) and a Transmission Electron Microscope (TEM) are used to physically observe and determine the root cause of the failure.

However, the SEM and TEM are both destructive tests, and they only allow you to look at one point among several possible failure locations. This greatly restricts the user's ability to locate the specific cause of a failure. In addition, it is difficult to apply conventional physical observation techniques to electrical failures caused by very small residues or abnormal dopant densities, which also reinforces the need to perform some sort of electrical testing.

Conventional probing schemes to electrically test a device require that the device be placed into a TEG (test element group) with probing pads, and this TEG is normally placed in the scribe lines between dice on the wafer. Obviously, this does not permit electrical characterization of the failed locations within an actual die.

Recently, nanoprobers utilizing Scanning Probe Microscope (SPM) techniques that can probe at the

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nm (9-10 nm) level using a piezoelectric actuator have become available. This application note introduces a new failure analysis technique that uses one of the most popular nanoprobers, the N-6000 Fine-structured Device Characteristic Evaluation System made by Hitachi High-Technologies Corporation, and the Agilent B1500A Semiconductor Device Analyzer. The N-6000 can contact directly to devices inside of an integrated circuit, which helps to bridge the gap between physical and electrical failure analysis techniques.

Nanoprobers Solve Problems but Present New Challenges

Using the appropriate preprocessing techniques, it is possible to use a nanoprober to measure individual transistors and wires within a failing device just as if they were test devices within a standard TEG (see Figure 1). This is a revolutionary leap forward; however, the nanoprober creates its own set of measurement challenges because thermal expansion and "creep" by the piezoelectric actuators make it difficult to maintain good electrical contact for long time periods.

The Agilent B1500A Semiconductor Device Analyzer can meet these challenges using the B1500A's EasyEXPERT software capability to quickly run one or more application tests within the short time window when good electrical contact is being made.

The remainder of this application note will show how to use the B1500A and a nanoprober to perform failure analysis on an SRAM cell using data provided by NEC Electronics Corporation.

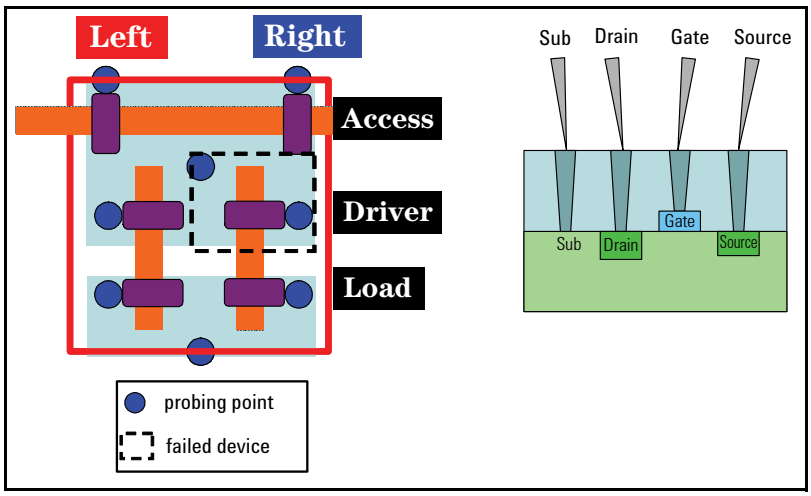


Fig. 1 SRAM and probing overview

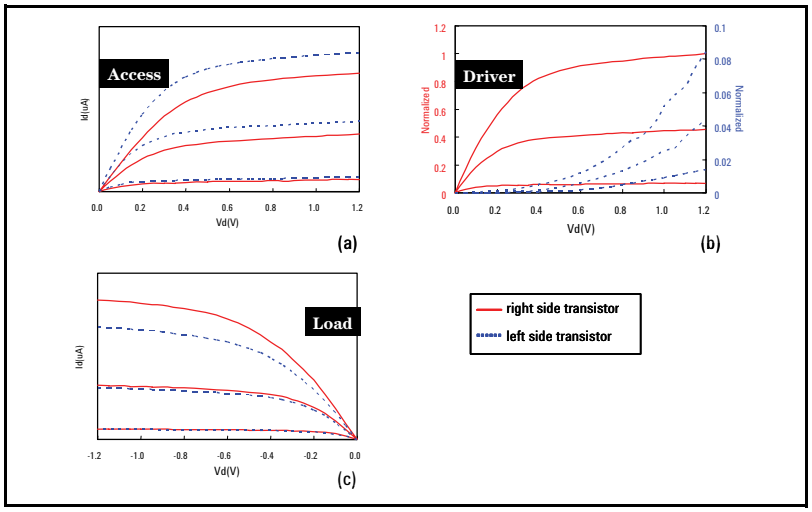


Fig. 2 I-V curve measured by nano-prober and B1500A

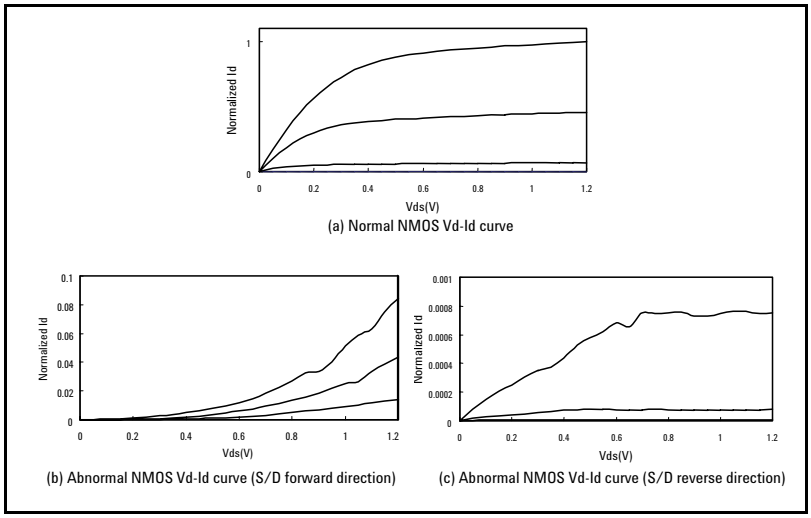


Fig. 3 Failure analysis data on dopant profile defect

An SRAM Failure Analysis Example

The first step in SRAM failure analysis is to identify the location of the questionable bit using a logic tester. However, the logic tester cannot identify which of the six transistors in the SRAM cell is failing. In traditional failure analysis the next step would involve destructive analysis on the SRAM cell using a TEM after estimating the failed transistor location within the SRAM cell by some means. Unfortunately, in some cases the cause of the SRAM failure still cannot be determined, which illustrates the gap between physical and electrical analysis capabilities. As shown in Figure 1, the nanoprober can directly probe the six transistors of an SRAM cell where a failure is suspected and perform electrical evaluation of each cell individually, thus helping to fill in the physical and electrical measurement gap. Of course, in order to perform this type of analysis you must remove the upper layers in order to contact each transistor individually. This is similar to the process performed in traditional failure analysis using a TEM and SEM. As previously mentioned, when using a nanoprober you have a very short time in which to make an electrical measurement. Therefore, the B1500A is a highly appropriate measuring device for this situation due to its large number of furnished application tests, its ability to make measurements with simple parameter settings, and its fast measurement speed.

Figure 2 shows Id-Vd curves for the six transistors of a failing SRAM memory cell measured using the B1500A and a nanoprober. Graph (a) shows the access transistors, graph (b) shows the driver transistors, and graph (c) shows the load transistors. A solid line is used to indicate the left transistors and a dashed line is used to indicate the right transistors. From these graphs it is easy to determine that the cause of the SRAM bit failure is a defective right side driver transistor.

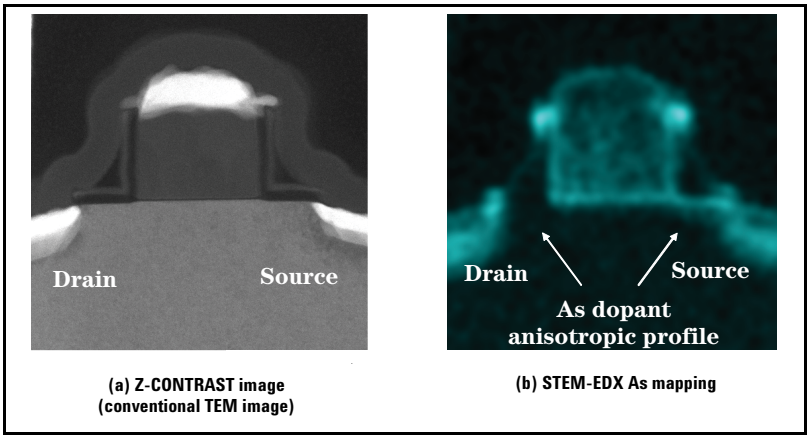


Fig. 4 Sectional view of abnormal NMOS

In order to perform a more detailed analysis on the defective transistor it is necessary to measure the transistor by switching the roles of the source (S) and the drain (D). Figure 3 (a) shows normal transistor characteristics, and Figure 3 (b) shows the characteristics of the apparently bad transistor. Figure 3 (c) shows data measured by reversing the source/drain (S/D) of the transistor (note: this can be done very easily using the B1500A and does not require changing any device connections). In the case where the S/D is in the forward direction, only a digit less current than the normal value flows and the I-V curve shows a downward tendency. Conversely, in the case where the S/D is in the reverse direction, although the IV curve shows an upward tendency, less than 1/1000 of the normal amount of current is flowing.

Comparing the measured results to simulated results, a hypothesis is generated that the arsenic (As) dopant density directly under the electrode of the left side of the failing transistor is not at its specified level. As a next step a cross-sectional TEM image of the suspect transistor is performed.

Figure 4 (b) shows the As dopant anisotropic profile created by EDX (Energy Dispersive X- ray Spectrometer), and it supports the hypothesis of the root cause of the failure. This type of detailed analysis cannot be performed using only conventional observations of the cross-sectional TEM. It shows that the combination of the B1500A and a nanoprober is a more powerful solution than conventional failure analysis techniques alone.

Customizing Application Tests for SRAM Failure Analysis

The Agilent B1500A Semiconductor Device Analyzer with EasyEXPERT software comes standard with more than 150 application tests. These furnished application tests support the vast majority of basic I-V measurement needs Moreover, using the built-in GUI-based application test development environment, it is easy to modify the supplied application tests, create new application tests, and string together sequences of application tests (including support for conditional branching).

The data in Figure 2 shows the result of Id-Vd measurement. As an I-V measurement used to evaluate the MOS transistor in the SRAM, the Id-Vd measurement or Id-Vg measurement is generally performed.

Therefore, in this application note, for the SRAM failure analysis, the example of an application test for which either the Id-Vd measurement or Id-Vg measurement can be selected is introduced.

As previously described, once a failing SRAM cell is identified it is necessary to determine which of the six transistors in the cell is bad. One method to do this is by electrical characterization of each transistor in the cell, and this can be done using a nanoprober. It is also very important to be able to measure a transistor in both directions (reversing the source and drain) to compare actual device performance with simulated device performance, as this can give important insight into processing issues.

There are several ways to achieve the above described measurement. One option is to create two separate sets of application tests with source and drain reversed, and then to perform both sets of tests for each transistor. The drawback of this approach is the time wasted taking unnecessary measurements. A second option is to first perform standard transistor measurements on each transistor, and then to measure the suspect transistor a second time with tests where the source and drain are reversed. The problem with this approach is that, if performed manually, it can take so much time that you may lose electrical contact before you can finish the testing. A third option (similar to option 2) is to first perform standard transistor measurements on each transistor, and then to manually switch the connections on the suspect transistor and repeat the tests. While this eliminates the need to create a

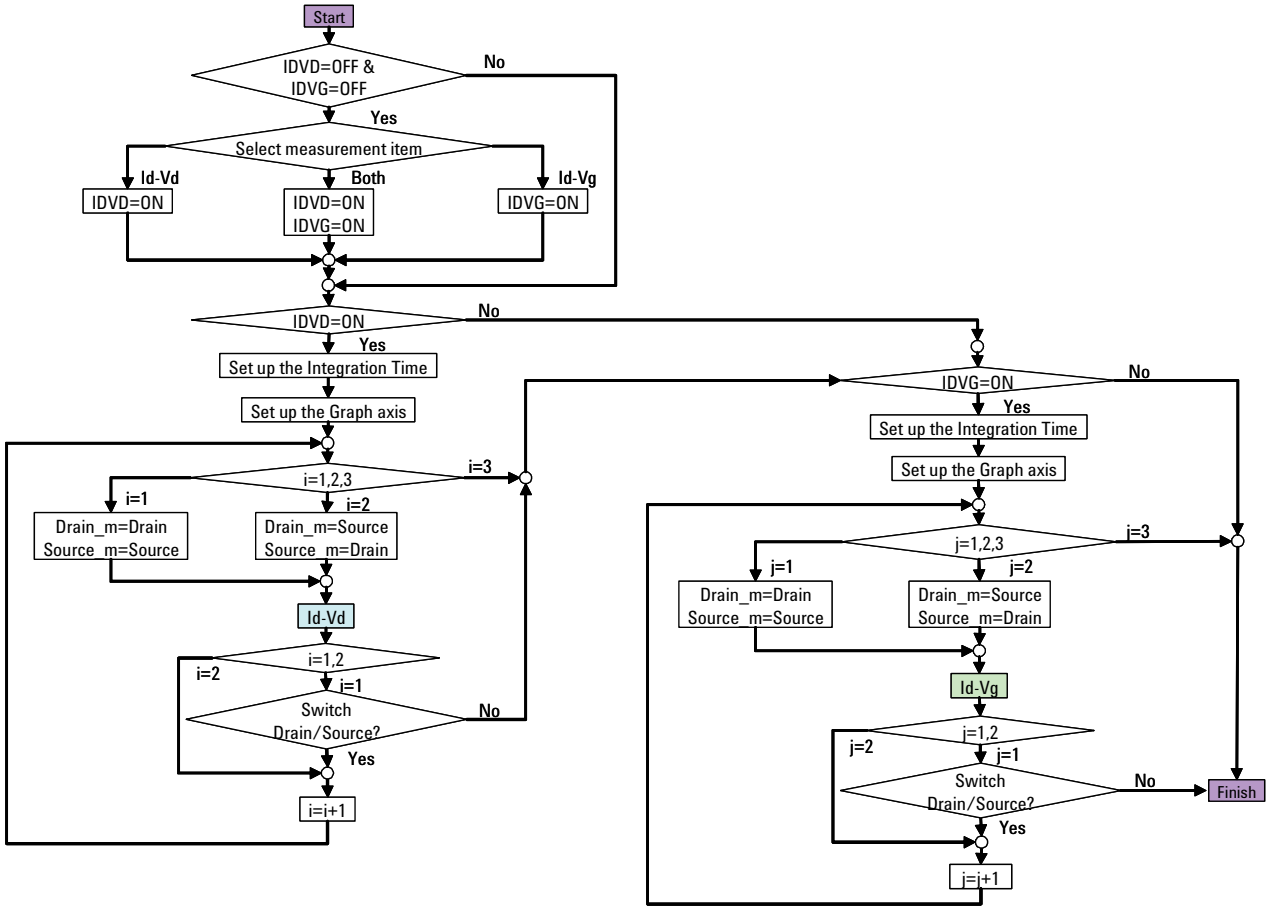


Fig. 5 Flowchart of application test for SRAM failure analysis

second set of tests, it takes even longer to perform this manual switching than it does to switch to a second set of tests as in the second case. Using EasyEXPERT software on the B1500A, it is easy to change the source and drain SMU assignments on the fly. This means that it is easy to reverse the assignment of the source and drain for the transistor identified as abnormal, thereby making the desired measurements in the minimum amount of time.

Sample SRAM Failure Analysis Test Flow

Figure 5 shows the flowchart for the sample application test for SRAM failure analysis. An overview of the program is as follows:

1. Select desired measurement tests (either Id-Vd or Id-Vg measurement, or both)
2. Set up the integration time
3. Set up X axis of the graph screen
4. Assign SMUs to the source and drain (set up the channel)
5. Perform the measurement (Id-Vd measurement or Id-Vg measurement)
6. After checking the measurement result, select the next step in the message box.
   - 6.a Measure after switching the source and the drain (Repeat the above 4 and 5)
   - 6.b End

Note: If both Id-Vd and Id-Vg measurements are selected in step 1 above, then after the Id-Vd measurement steps 2 through 6 are repeated for the Id-Vg measurement.

The main window for the application test definition and the Extended Setup screen are shown in Figure 6. The main window enables the selection of measurement items, the setup of the channel for each terminal of the transistor, and the setup of the measurement condition. The measurement is possible only by setting these parameters in the EasyEXPERT main window. The example of the measurement result of this application test is shown in Figure 7.

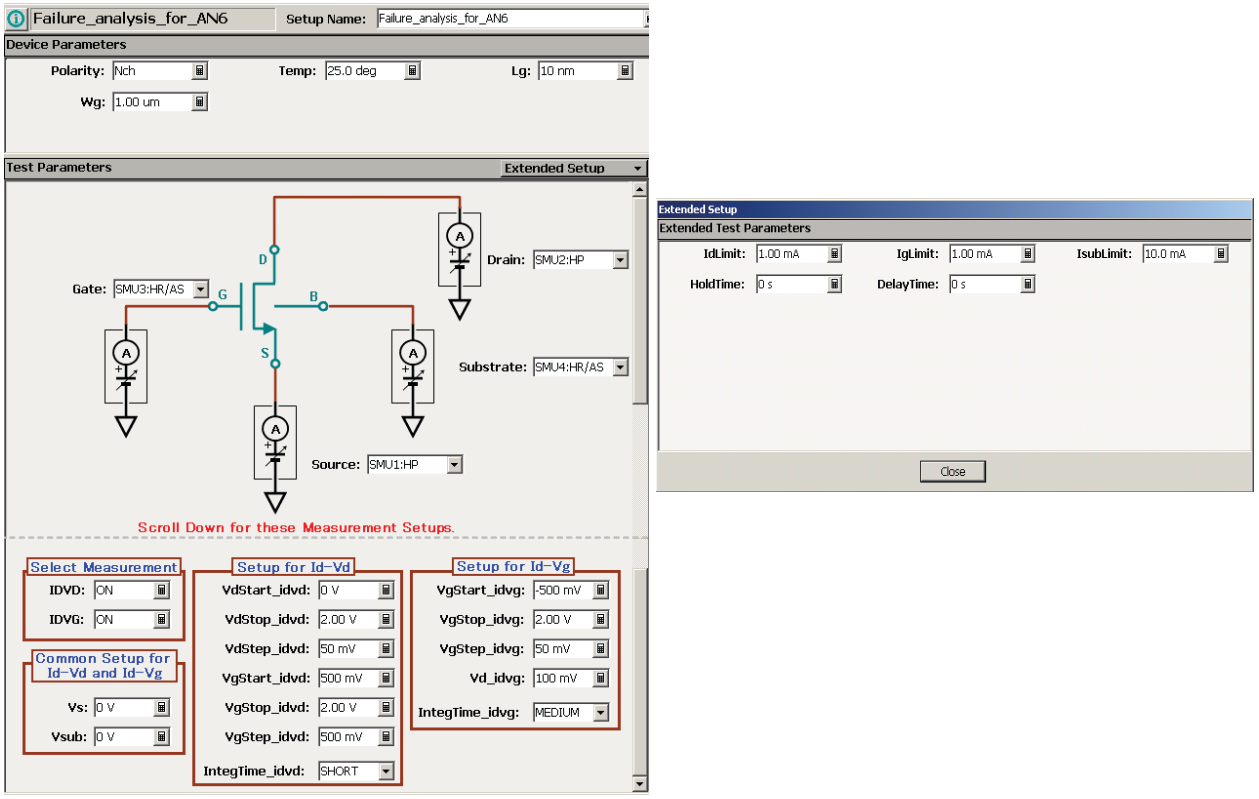


Fig. 6 Main window of application test for SRAM failure analysis, and Extended Setup screen

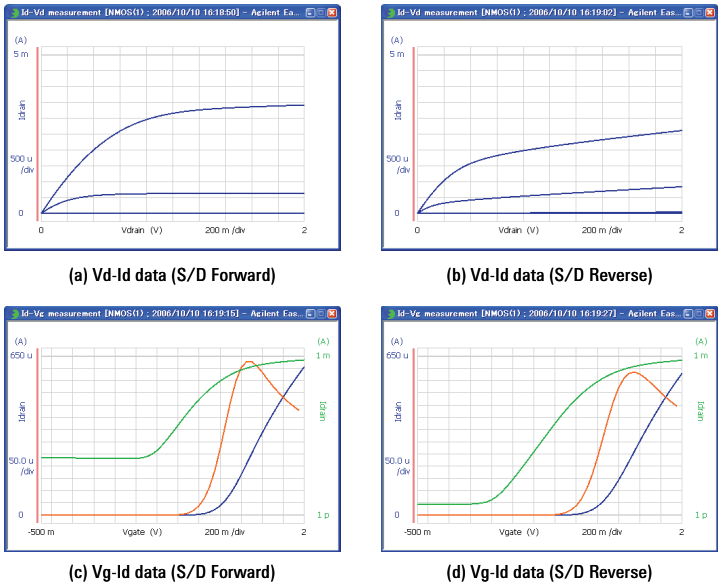
Measurement data is stored automatically as a test record in the list area of Results. In the default condition, the list area of Result shows only the name of the application test that was last shown by the Data Display.

To show all of the executed application tests, select the "Results > Filter > Expand Application Test Results" option from the drop-down menu. All of the measurement data will then be shown in the list area as shown in Figure 8.

Summary

Many failure mechanisms (such as dopant abnormalities) are difficult to detect using conventional failure analysis methods. However, by combining the Agilent B1500A with a nanoprober, it is possible to probe individual transistors within an integrated circuit just as easily as it is to measure devices in a conventional TEG. The ability of the B1500A's EasyEXPERT software to swap SMU pin assignments on the fly, coupled with EasyEXPERT's powerful application test sequencing capabilities, permit the automated evaluation of suspect transistors in both the forward and reverse directions quickly and efficiently. The ability to perform this electrical testing extremely fast is very important when using a nanoprober, since there is a very small time window during which to make the measurements before electrical contact is lost. This application note outlines this process using the debug of an SRAM cell as an example.

The definition file of the application test for the SRAM failure analysis introduced in this application note can be downloaded from the Agilent B1500A web site (http://www.agilent.com/see/B1500A).



(a) Vd-Id data (S/D Forward)

(b) Vd-Id data (S/D Reverse)

(c) Vg-Id data (S/D Forward)

(d) Vg-Id data (S/D Reverse)

Fig. 7 Example of measurement result (Data Display) of application test for SRAM failure analysis

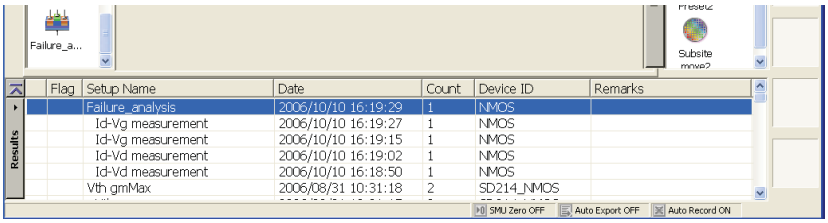


Fig. 8 List area after expansion

References

1) Yorinobu Kunimune, LSI test symposium 2005 proceedings, pp329, 2005

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