

A Complete CMOS Reliability Test Solution

Keysight B1500A Semiconductor Device Analyzer



Introduction

As CMOS device feature sizes continuously scale down there are accompanying increases in both electric field strength and current density, which in-turn act to reduce device lifetimes. These factors make the testing of CMOS device reliability concerns such as gate and interlayer dielectric degradation, hot carrier effects, bias temperature instability and interconnect opens and shorts crucial to guarantee integrated circuit (IC) lifetimes.

The Keysight Technologies, Inc. B1500A Semiconductor Device Analyzer is the next-generation semiconductor parameter analyzer that possesses the measurement capabilities necessary to evaluate the reliability of advanced CMOS LSI (large scale integration) circuits. In addition, the B1500A's resident EasyEXPERT control software comes standard with ready-to-use measurement libraries that cover all of the common CMOS reliability tests.

This application note gives an overview of the B1500A's key measurement features and shows how the B1500A is a complete solution for verifying CMOS process reliability.

Comprehensive State-of-the-art Measurement Capabilities

Ten module slots and a wide selection of source/monitor units (SMUs) and other state-of-the-art module types enable the B1500A to be configured to meet the most exacting measurement requirements of CMOS process reliability testing. The following figure summarizes the available B1500A modules.

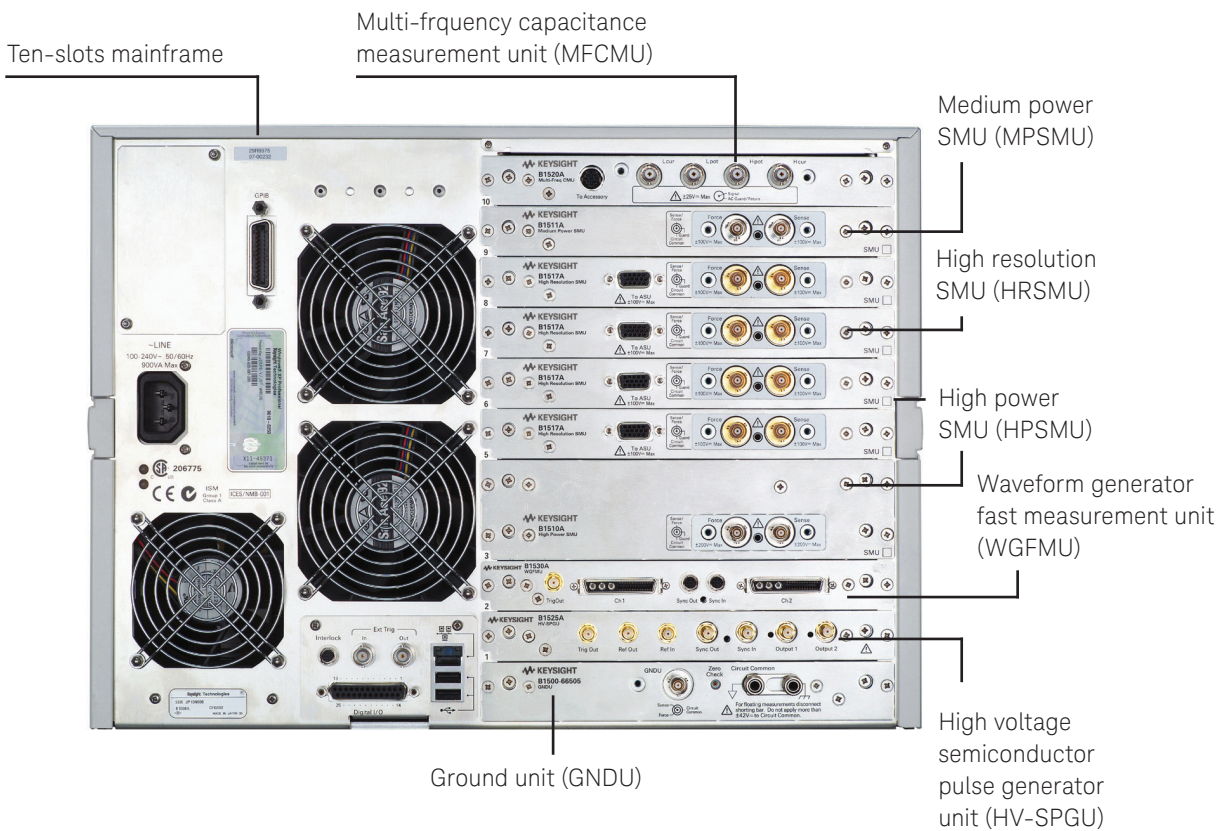


Figure 1. Flexible configuration of measurement modules

Medium Power SMU (MPSMU)

The MPSMU is a general purpose SMU possessing moderate voltage and current sourcing capability and measurement resolution. The MPSMU's maximum output voltage is ± 100 V and its maximum output current is ± 100 mA. The MPSMU's minimum current measurement resolution is 10 fA and its minimum voltage measurement resolution is 0.5 μ V.

High Resolution SMU (HRSMU)

The HRSMU is designed for measurements requiring extreme precision such as gate leakage, off-state leakage and sub-threshold current measurement. The HRSMU's minimum current measurement resolution is 1 fA (versus 10 fA for the MPSMU). In addition, when combined with the atto-sense and switch unit (ASU) the HRSMU can achieve a current measurement resolution of 100 aA (0.1 fA) while still maintaining the same voltage and current sourcing capabilities as the MPSMU.

High Power SMU (HPSMU)

As the name implies, the HPSMU has expanded voltage and current sourcing capabilities relative to the other SMUs. The HPSMU's maximum output voltage is ± 200 V and its maximum output current is ± 1 A. The 200 V output capabilities are useful for breakdown measurements and the 1 A output capability supports important reliability tests such as device interconnect electromigration testing.

High Power SMU (HPSMU) (continued)

All of the B1500A's SMUs are Kelvin with separate force and sense inputs, which is required for accurate measurement of low resistance and high-current devices. In addition, all SMUs support a quasi-static capacitance versus voltage (QSCV) measurement capability, which is useful for evaluating gate dielectric interface defect density. The QSCV function by SMUs also possess a leakage current compensation feature that aids in the measurement of thin gate dielectrics.

High Voltage Semiconductor Pulse Generator Unit (HV-SPGU)

The B1500A's HV-SPGU module is specifically designed for the electrical measurement of semiconductor devices.

Pulse generators can be used in reliability testing to evaluate interface defect densities between the gate dielectric and substrate using the charge pumping method. Pulse generators can also be used to apply pulsed (AC) stress bias for SMS (Stress-Measure-Stress) testing.

The HV-SPGU's frequency range is 0.1 Hz to 33 MHz and each HV-SPGU module has two independent channels. Each channel has ± 40 V sourcing capability (into an open load) and a minimum voltage resolution of 1.6 mV.

An optional 16440A SMU/Pulse Generator Selector unit and 16445A SMU/PGU Selector Connection Adapter are available to support effortless switching between the HV-SPGUs and SMUs.

Waveform Generator / Fast Measurement Unit (WGFMU)

The WGFMU is a two-channel module that combines ALWG (Arbitrary Linear Waveform Generator) voltage pulsing capability with ultra-fast IV measurement. Voltage waveforms can be specified with a minimum sampling rate of 10 ns. By combining ALWG and IV measurement into a single module both DC and AC stress biases can be applied and measurements can be made seamlessly.

The WGFMU module's voltage output has a 16 bit resolution and it covers the following voltage ranges: - 5 V to 5 V, -10 V to 0 V, or 0 V to +10 V. The module's minimum sampling interval for IV measurements is 5 ns and it supports measurement ranges of 1 μ A, 10 μ A, 100 μ A, 1 mA and 10 mA (14 bit resolution).

This module can perform ultra-fast negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) measurements (both DC and AC stress) without any dynamic recovery effects. It can also perform ultra-fast hot carrier injection (HCI) measurements.

Multi Frequency Capacitance Measurement Unit (MFCMU)

High-frequency capacitance versus voltage (HFCV) curves measured using a capacitance meter are typically used to evaluate CMOS device electrical characteristics such as threshold voltage, flat-band voltage and the substrate doping density profile. In addition, by comparing the HFCV curve with a QSCV curve measured using the SMUs the energy distribution of interface defect density can be extracted.

The B1500A's MFCMU module eliminates the need for a separate external capacitance meter. The MFCMU has a frequency range from 1 kHz to 5 MHz, and it can supply a DC bias of ± 25 V. An optional SMU CMU unify unit (SCUU) supports automated capacitance versus voltage (CV) and current versus voltage (IV) switching in positioner-based wafer probing environments, which eliminates the need to use a switching matrix to perform this function. The SCUU also expands the available capacitance measurement DC bias voltage to ± 100 V using either the MPSMUs or HRSMUs as a bias sources.

Ready to Use Reliability Test Library

Keysight EasyEXPERT software, which is resident on the PC-based B1500A, is a powerful Microsoft Windows application program for parametric test. EasyEXPERT provides an easy and effective measurement and analysis environment combined with an intuitive graphical user interface (GUI). Interaction with EasyEXPERT can occur either through the B1500A's touch screen LCD panel or via an optional USB keyboard and mouse. The familiar Windows environment reduces the learning curve and supports easy networking and data export into MS office-based tools. EasyEXPERT employs a unique "top-down" approach to device characterization that allows users to immediately focus on making measurements without having to learn all the intricacies of the instrument hardware. EasyEXPERT comes with more than 240 measurement algorithms conveniently organized by device type, application, and technology, including measurements for typical CMOS reliability test as explained below.

Gate Dielectric Integrity

The effect of high-intensity electric fields on gate dielectrics is a major concern for LSI circuit reliability. Two main techniques are used to gauge gate dielectric integrity: time-zero dielectric breakdown and time-dependent dielectric breakdown.

TZDB (Time Zero Dielectric Breakdown) applies an increasing gate voltage and measures gate leakage current until the dielectric breaks down. The term "time zero" emphasizes that the breakdown is caused primarily by the rapidly increasing electric field in the gate oxide and not the duration of the stress. Of course, in practice the actual ramp rate does have an effect on the breakdown voltage.

TDDB (Time Dependent Dielectric Breakdown) measures dielectric breakdown caused by long-term exposure to a relatively low electrical field. The stress applied during a TDDB test can be either constant voltage or constant current, with the key measurement parameter being the time it takes for breakdown to occur. Typically, the total charge injected into the gate dielectric to achieve breakdown (Q_{bd}) is measured.

Two common time dependent dielectric breakdown tests are voltage ramp (V-Ramp) and current ramp (J-Ramp). The V-Ramp test increases the voltage across a dielectric at a constant linear rate until failure occurs. The J-Ramp test increases current through a dielectric at points that are logarithmically spaced in time. Both tests record the total charge to breakdown (Q_{bd}) and the breakdown voltage (V_{bd}). Both methods are effective to evaluate gate dielectric quality in a short time period, which provides fast feedback to the process engineer. More information on V-Ramp and J-Ramp testing can be found in the JEDEC standard entitled "Procedure for the Wafer-Level Testing of Thin Dielectrics". Table 1 shows a list of application tests for gate dielectric integrity included in EasyEXPERT.

Figure 2 shows a V-Ramp application test example. The process to access this test is as follows. The user first selects the "Reliability" technology category. Next, the user selects the "V-Ramp" application test from the displayed test list. The application test visually displays the connections between the DUT and the SMUs, and the built-in documentation feature describes how this application test works to execute the V-Ramp test. For the final step, the user fills in the measurement parameters and clicks on the start button.

The measurement begins and when completed the breakdown voltage (Q_{bd}) and time to breakdown (T_{bd}) are automatically extracted and displayed on the screen along with the I-V plot. After completion, the measurement results can be automatically stored into EasyEXPERT's built-in database.

Table 1. List of Application Test for Gate Dielectric Integrity

Measurement	Application Test
TZDB	TZDB
TDDB	TDDB Istress, TDDB Istress 3devices, TDDB Istress2, TDDB Istress2 3devices, TDDB Vstress, TDDB Vstress 3devices, TDDB Vstress2, TDDB Vstress2 3devices
V-Ramp / J-Ramp	V-Ramp, J-Ramp

Hot Carrier Effects and Bias Temperature Instability

HCI and NBTI/PBTI are the most important phenomena currently being discussed in the area of advanced CMOS device development and reliability.

HCI degradation is caused by the injection of highly energized (hot) electrons into the gate dielectric. The hot electrons are generated by impact ionization due to electron acceleration caused by the strong electric fields around the drain terminal area as shown in figure 3 (a). The electrons injected into the gate dielectric increase the density of interface defects.

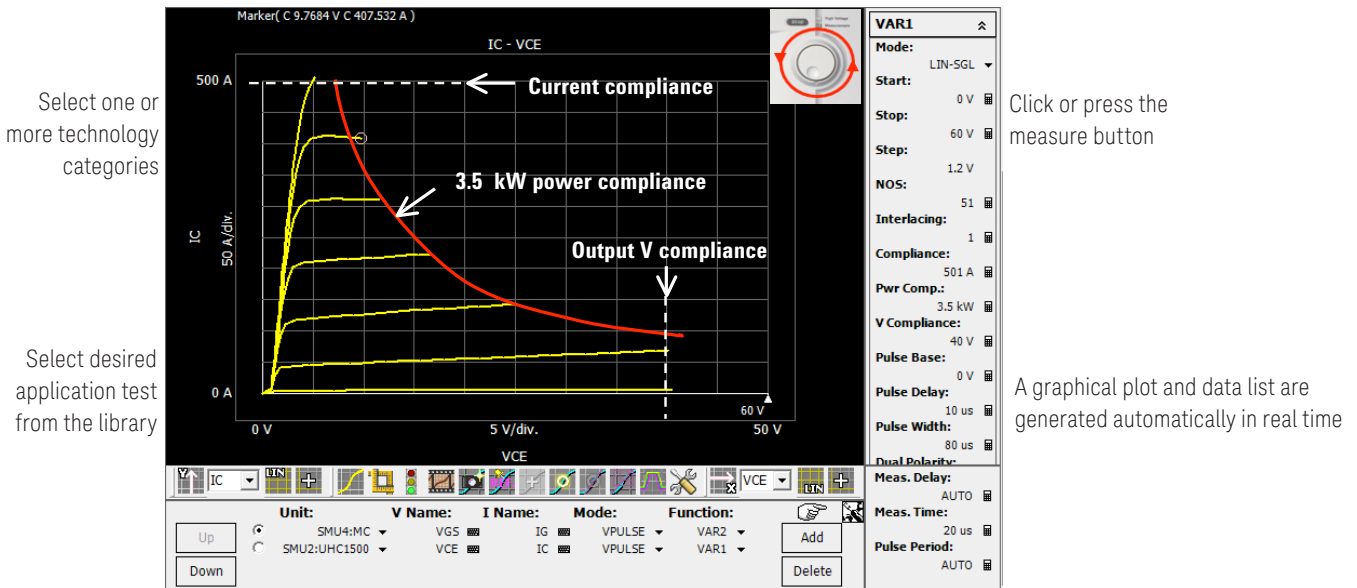


Figure 2. Application example for V-Ramp Test

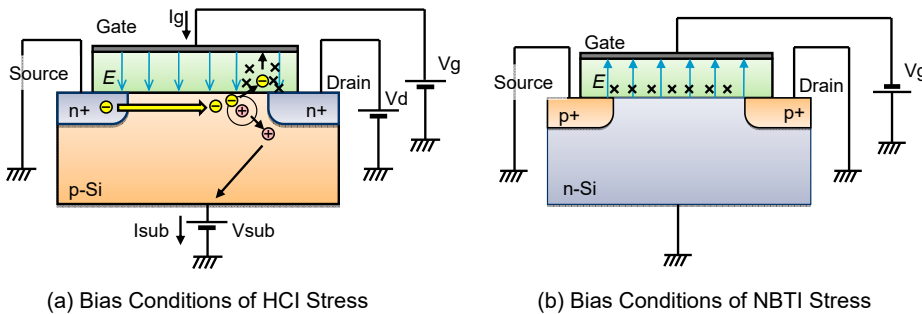


Figure 3. Bias conditions for HCI and BTI stress

Hot Carrier Effects and Bias Temperature Instability (continued)

BTI is a different degradation mechanism that occurs during the MOSFET off-state (please see figure 3 (b)). BTI has the greatest impact on PMOS FETs when they have a negative gate bias voltage applied to them (NBTI). NBTI was first observed in the early 1990's; however, the physics behind this phenomenon is still being debated to this day. Experimental data shows that NBTI degradation gets worse at higher temperatures and thinner gate oxides, which means that advanced semiconductor processes are strongly impacted by this phenomenon.

HCI and NBTI can both shift MOSFET threshold voltage as shown in the figure 4. Thus, obtaining an accurate estimate of HCI and NBTI effects on device lifetimes is essential to insure that the MOSFETs used in an IC meet their reliability criteria.

The typical technique used to evaluate HCI and NBTI degradation is the stress-measure-stress (S-M-S) method. Typically, in an S-M-S measurement the IV characteristics prior to applying stress are first measured as a reference. A stress is then applied and V_{th} (or I_d around V_{th}) is periodically measured during the stress. This permits a plot of the change in V_{th} (ΔV_{th}) or I_d (ΔI_d) versus the accumulated stress time to be created. The lifetime of the MOSFET can then be estimated from this data.

EasyEXPERT includes application tests to perform both HCI and BTI as shown in table 2. EasyEXPERT also includes charge pumping application tests, which are useful to evaluate an increase of boundary defects during the test. The charge pumping application tests work with either in the B1500A's HV-SPGU module or an external Keysight 81110A pulse generator.

For all of these tests where a constant stress is applied over time, it is also very important to minimize the measurement time during which the stress is not applied. Especially in the case of NBTI testing, the devices under test can recover very quickly after stress has been removed and if this occurs the measurement data will underestimate the actual transistor degradation in the field. Similar problems have also been reported for HCI degradation tests as well.

In addition to the aforementioned issues, there is another important factor that can have a serious impact on device lifetime estimates. NBTI testing performed with a pure DC stress gives device lifetime estimates that are much lower than those performed with AC stress. However, AC stress is a more accurate representation of the stress that devices will experience under real-world conditions.

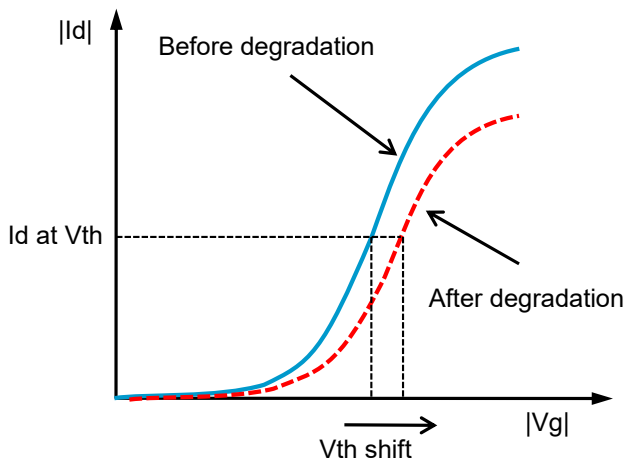


Figure 4. V_{th} shift due to HCI or NBTI Stress

Hot Carrier Effects and Bias Temperature Instability (continued)

Table 2. List of Application Test for FET Reliability Test

Measurement	Application Test
HCI	HCI, HCI2, HCI 3devices
Charge Pumping	Charge Pumping, Charge Pumping2
BTI by SMU	BTI, BTI[3], BTI2 , BTI2[3], BTI 3devices, BTI 3devices[3], Timing On-the-fly NBTI
Ultra Fast BTI by WGFMU	Fast BTI(AC stress Id-Sampling), Fast BTI(DC stress Id-Sampling), Fast BTI(AC stress Id-Vg), Fast BTI(DC stress Id-Vg)

The B1500A's WGFMU module can perform S-M-S testing and apply either DC or AC stress. It can perform both spot and sweep measurements with minimal interruption to the stress as shown in Figure 5. It allows researchers to determine the lifetimes of devices and to differentiate various types of degradation by comparing the results of different stress and measurement types.

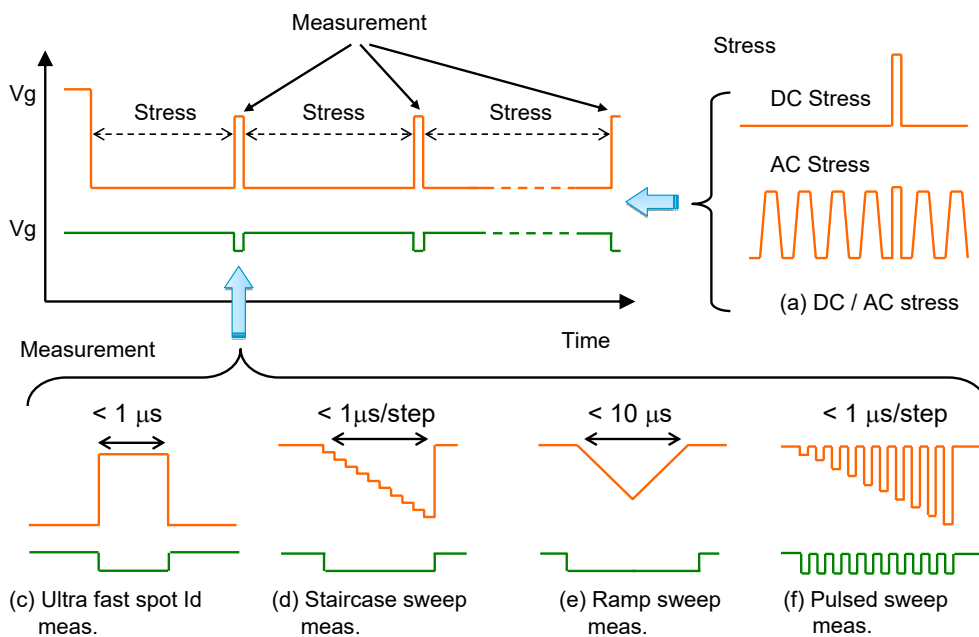


Figure 5. Fast and variable stress and measurement configuration by B1500A.

Interconnect Reliability

Another reliability issue exacerbated by process scaling is Electromigration (EM). EM is the phenomenon in which atoms in the metal interconnect migrate under the influence of the current flow, ultimately resulting in metal voids or interconnect shorts that then cause circuit failure.

In the case of open failures, the metal atoms in the wiring move under the influence of the electron flow until an actual void in the metal line is created. The void increases the current density in the surrounding metal, which in-turn causes the void to grow even larger. This process continues until the void becomes large enough to finally break the connection.

The other typical EM failure mechanism is an extrusion (hillock or whisker) that can cause an interlayer short. In this case, the electron flow squeezes the metal atoms (similar to a toothpaste tube being squeezed hard) until they burst out and create a short into adjacent wiring.

Table 3 shows a list of furnished application tests for EM. Tests are available for both voiding and extrusion failure detection using either voltage or current stressing.

Table 3. List of Application Test Library for Electro Migration Test

Measurement	Application Test
Electro Migration	EM Istress, EM Istress2, EM Istress[2], EM Istress2[2], EM Istress[6], EM Istress2[6], EM Vstress, EM Vstress2, EM Vstress[2], EM Vstress2[2], EM Vstress[6], EM Vstress2[6]

Conclusion

As CMOS device feature sizes continuously scale down there are accompanying increases in both electric field strength and current density, which in-turn act to reduce device lifetimes. In order to understand and meet target device lifetimes, it is important to evaluate all aspects of device reliability, including gate dielectric integrity, hot carrier effects, bias temperature instability and interconnection reliability. For tests such as NBTI that have quick recovery times, the ability to perform fast measurements, minimize stress interruption and provide an AC stress bias are necessary to correctly estimate device lifetime under real-world conditions.

The B1500A is a modular and self-contained instrument that allows you to configure solutions capable of performing even the most challenging reliability test. Keysight EasyEXPERT software provides easy and intuitive instrument control for the B1500A, and the furnished application test libraries reduce the learning curve and allow you to begin making productive reliability tests immediately.

B1500A now supported in Windows 10

B1500A PC platform has been renewed. It includes Windows 10 OS, faster CPU, 8 GB of memory and a solid state drive (SSD). The latest PC platform enables you to perform your software tasks easily while improving your total computing performance.

Windows 10 upgrade option is also available.

For more detail: <https://literature.cdn.keysight.com/litweb/pdf/5991-3327EN.pdf>

www.keysight.com/find/B1500A

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:

www.keysight.com/find/contactus

