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AN-A007: 4 GHz Television Receive Only LNB Design

Introduction

This note describes the design of a modern LNB (low noise block converter) for the C band (3.7–4.2 GHz) TVRO market. The block converter consists of a low noise amplifier (LNA), a self oscillating mixer (SOM), and an IF amplifier. Each of these circuit sections are discussed separately.

LNA Design

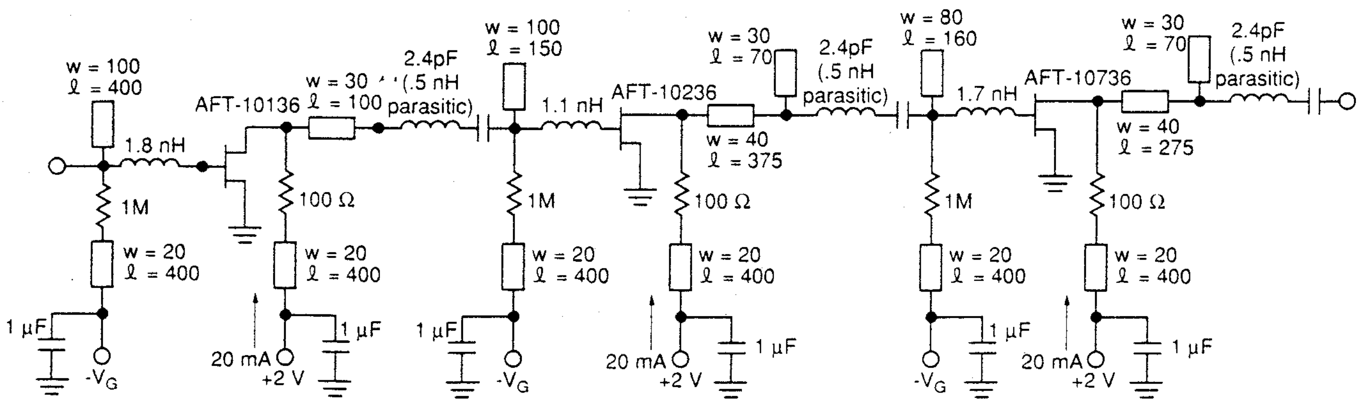
The LNA discriminates the relatively week TV signal received by the antenna from background noise, and amplifies it to a reasonable working level. The most important specification of this section is its noise figure, which must be on the order of 1.0 dB to ensure good picture reception[1]. About 30 dB of power gain is required to raise the signal to a suitable level to drive the SOM, and to ensure that the relatively high noise figure of the SOM is masked. The operating frequency band is 2.7 to 4.2 GHz.

The 1.0 dB noise figure requirement indicates that a GaAs FET must be used for this design. Three stages of amplification are needed to achieve the desired gain. The devices selected are the Avantek ATF-10136, ATF-10236, and ATF-10736. These three GaAs FETs are noise selected versions of a 500 micron device specifically developed for 4 GHz TVRO applications. They are packaged in stripline ceramic packages suitable for commercial applications. The premium noise performance of the ATF-10136 makes it the best choice for the first stage; second stage noise figure is still important, but not as critical as the first stage, so an ATF-10236 is used. The third stage is a gain stage with little contribution to the cascaded noise figure, so an ATF-10736 is most appropriate.

The RF portion of the design uses device catalog s and noise parameters and the linear analysis and optimization program Touchstone™ from EEsof. The input matching circuit must transform the generator impedance (nominal 50 Ω) to the Γ_{opt} of the ATF-10136 if best noise performance is to be obtained. Interstage matches transfer s_{22} of each drive transistor to Γ_{opt} for its load transistor. The output circuit matches the 50 Ω load impedance to s_{22}^* of the AFT-10736 for best power gain. All of these networks can also be realized using combinations of transmission line section, open stub tuners, and series inductors using the gate leads of the packaged FETs.

The finished RF schematic is shown in Figure 1. A print-out of the simulation of this circuit is reproduced in Figure 2. The S and noise parameter data used for the design is given in Figure 3. The predicted noise performance, gain, match and stability of the amplifier is shown in Figure 4.

The amplifier maintains a noise figure of less than .7 dB and an associated gain above 37 dB across the 3.7 to 4.2 GHz frequency range. For the bias circuitry needed to complete the design, we recommend the kind of PNP active bias described in applications note *AN-A002: A 4 GHz TVRO System.*



Substrate = 1/32" Epoxy Glass (ε = 4.8)

Figure 1. 4 GHz Low Noise Amplifier Schematic

```
 ! < 3ATF4G_T.CKT >
 ! 3.7 - 4.2 GHZ 3 STG LOW NOISE AMPLIFIER
 ! USING ATF-10136 ATF-10236 AFT-10736

CKT

 MSUB ER=4.8 H=31 T=1 RHO=1 RGH=0  ! EPOXY GLASS

 MLOC     1                 W=100 L=140
 RES      1     11          R=1E6
 MLIN     11    0           W=20 L=400
 IND      1     2           L=1.8
 DEF2P    1     2           NAIN


 S2PA     2     3     0     A:10136N
 DEF2P    2     3           NA2P

 RES      3     32          R=100
 MLIN     32    0           W=20 L=400
 MLIN     3     4           W=30 L=100
 SLC      4     5           L=.5 C=2.4
 DEF2P    3     5           NAOUT

 MLOC     1                 W=100 L=150
 RES      1     11          R=1E6
 MLIN     11    0           W=20 L=400
 IND      1     2           L=1.1
 DEF2P    1     2           NBIN


 S2PB     2     3     0     A:10236N
 DEF2P    2     3           NB2P

 RES      3     32          R=100
 MLIN     32    0           W=20 L=400
 MLIN     3     4           W=40 L=375
 MLOC     4                 W=30 L=70
 SLC      4     5           L=.5 C=2.4
 DEF2P    3     5           NBOUT

 MLOC     1                 W=80 L=160
 RES      1     11          R=1E6
 MLIN     11    0           W=20 L=400
 IND      1     2           L=1.7
 DEF2P    1     2           NCIN

 S2PC     2     3     0     A:10736N
 DEF2P    2     3           NC2P

 RES      3     32          R=100
 MLIN     32    0           W=20 L=400
 MLIN     3     4           W=40 L=275
 MLOC     4                 W=30 L=170
 SLC      4     5            L=.5 C=2.4
 DEF2P    3     5           NCOUT

   NAIN     1     2
   NA2P     2     3
   NAOUT    3     4
   NBIN     4     5
   NB2P     5     6
   NBOUT    6     7
   NCIN     7     8
   NC2P     8     9
   NCOUT    9     10
   DEF2P    1     10          LNA

FREQ

   SWEEP    0.5   6.0   .5
   SWEEP    3.5   4.3   .1

OUT

   LNA      DB[S21]   GR1A
   LNA      K         GR2
   LNA      DB[NF]    GR1
   LNA      DB[S22]   GR3
   LNA      DB[S11]   GR3


GRID

   RANGE    3.6   4.3   .1
   GR1      0.5   2.0   .25
   GR1A     30    45
   RANGE    2.0   4.5   .5
   GR2      0     20    5
   GR3      -20   0     5
```

Figure 2. LNA Simulation

ATF-10136 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.5	.98	-18	5.32	163	.020	78	.35	-9
1.0	.93	-33	5.19	147	.038	67	.36	-19
2.0	.79	-66	4.64	113	.074	59	.30	-31
3.0	.64	-94	4.07	87	.110	44	.27	-42
4.0	.54	-120	3.60	61	.137	31	.22	-49
5.0	.47	-155	3.20	37	.167	13	.16	-54
6.0	.45	162	2.88	13	.193	-2	.08	-17
7.0	.50	120	2.51	-10	.203	-19	.16	45
8.0	.60	87	2.09	-32	.210	-36	.32	48
9.0	.68	61	1.75	-51	.209	-46	.44	38
10.0	.73	42	1.52	-66	.207	-58	.51	34
11.0	.77	26	1.26	-82	.205	-73	.54	27
12.0	.80	14	1.12	-97	.200	-82	.54	15

ATF-10136 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	Fopt dB	GAMMA OPT Mag	GAMMA OPT Ang	RN/Zo –
2.0	0.4	.70	47	0.46
4.0	0.5	.39	126	0.36
6.0	0.8	.36	-170	0.12
8.0	1.1	.45	-100	0.38
12.0	1.4	.60	-41	1.10

ATF-10236 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.5	.97	-20	5.68	162	.023	76	.47	-11
1.0	.93	-41	5.58	143	.050	71	.45	-23
2.0	.77	-81	4.76	107	.086	51	.36	-38
3.0	.59	-114	4.06	80	.120	35	.30	-51
4.0	.48	-148	3.51	52	.149	18	.23	-67
5.0	.46	166	3.03	26	.172	3	.10	-67
6.0	.53	125	2.65	1	.189	-14	.09	48
7.0	.62	96	2.22	-20	.191	-28	.24	55
8.0	.71	73	1.75	-39	.189	-41	.37	51
9.0	.75	54	1.47	-55	.184	-46	.46	42
10.0	.78	39	1.28	-72	.180	-59	.51	34
11.0	.82	226	1.04	-86	.179	-71	.54	26
12.0	.84	12	0.95	-101	.177	-82	.54	17

ATF-10236 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	Fopt dB	GAMMA OPT Mag	GAMMA OPT Ang	RN/Zo –
2.0	0.6	.73	74	0.33
4.0	0.8	.45	148	0.15
6.0	1.0	.42	-137	0.12
8.0	1.3	.49	-80	0.45
12.0	1.6	.65	-20	1.16

Figure 3. S and Noise Parameters of 4 GHz GaAs FETs

ATF-10736 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.5	.96	-20	5.90	162	.024	77	.50	-10
1.0	.92	-40	5.77	144	.046	66	.48	-21
2.0	.77	-76	4.92	109	.086	52	.39	-34
3.0	.59	-107	4.2	83	.111	40	.33	-45
4.0	.49	-136	3.64	57	.137	24	.26	-61
5.0	.43	-179	3.15	32	.167	9	.14	-65
6.0	.49	138	2.74	8	.179	-5	.05	22
7.0	.57	106	2.32	-13	.183	-18	.19	60
8.0	.68	81	1.92	-32	.185	-33	.33	57
9.0	.73	62	1.62	-50	.183	-40	.42	46
10.0	.77	47	1.41	-66	.182	-52	.46	38
11.0	.82	36	1.12	-81	.186	-67	.50	27
12.0	.85	22	0.98	-97	.189	-75	.51	15

ATF-10736 S Parameters, V_{DS} = 2 V, I_D = 20 mA

Freq. GHz	Fopt dB	GAMMA OPT Mag	GAMMA OPT Ang	RN/Zo –
2.0	0.9	.75	85	0.27
4.0	1.2	.48	159	0.08
6.0	1.4	.46	-122	0.08
8.0	1.7	.53	-71	0.43
12.0	2.0	.69	-14	1.04

Figure 3. (Cont'd) S and Noise Parameters of 4 GHz GaAs FETs

Freq. GHz	DB[S21] LNA	K LNA	DB[NF] LNA	DB[S22] LNA	DB[S11] LNA
0.50000	24.804	872.750	2.435	-2.180	-0.375
1.00000	28.814	237.385	2.103	-5.559	-1.321
1.50000	30.071	97.916	2.040	-7.405	-2.589
2.00000	30.419	41.820	2.031	-7.048	-3.749
2.50000	31.162	11.880	1.885	-5.723	-2.713
3.00000	34.485	1.052	1.552	-4.922	-0.760
3.50000	39.459	1.138	0.957	-24.020	-4.053
3.60000	38.901	1.311	0.830	-18.504	-6.341
3.70000	38.228	1.402	0.714	-13.168	-7.665
3.80000	37.732	1.409	0.620	-11.234	-8.010
3.90000	37.504	1.354	0.561	-10.713	-8.059
4.00000	37.502	1.270	0.551	-11.143	-8.272
4.10000	37.694	1.156	0.591	-12.401	-8.479
4.20000	37.591	1.097	0.674	-13.000	-8.658
4.30000	36.872	1.129	0.804	-10.984	-8.786
4.50000	33.997	1.547	1.206	-7.063	-10.499
5.00000	25.698	4.603	2.852	-4.035	-7.804
5.50000	14.882	11.854	4.937	-4.467	-1.257
6.00000	4.334	33.979	7.179	-4.589	-0.407

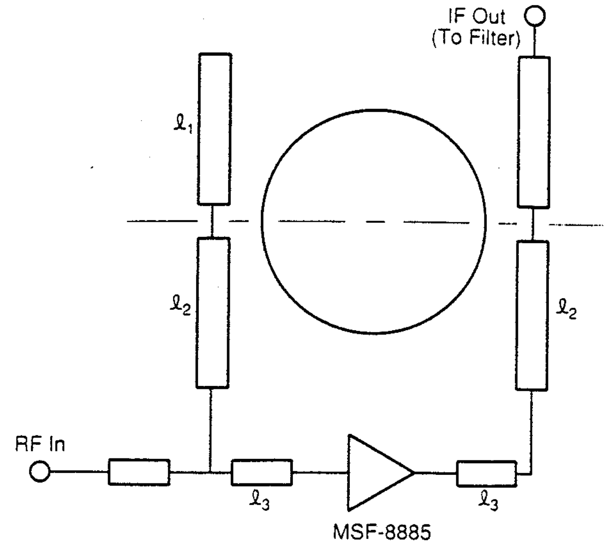
Figure 4. Predicted Performance of 4 GHz LNA

SOM Design

The downconversion of the received 4 GHz signal to a nominal 1 GHz IF frequency is accomplished using HP's MMIC frequency converter MSF-8885. This device uses the EB junction of the input transistor of a Darlington pair to act as an unbalanced mixer. The RF signal is provided to the input of the MMIC by the LNA described above. The LO (local oscillator) signal is created by establishing a feedback loop around the MSF-8885. This loop must provide 360° phase shift around the MMIC at the LO frequency of 5.15 GHz, and have less loss than the MMIC has gain at that frequency. If desired, the loop could be designed to provide a 2.75 GHz oscillator instead (low side injection). The second transistor of the Darlington provides IF gain. The structure has a minimum conversion gain of 7 dB when used in this application.

Note that as there is no isolation in the mixer, filters must be used with this frequency converter. These are realized using simple distributed circuits. A bandpass filter must follow the LNA to keep both the LO and the IF signals from radiating back into its output. A lowpass (or bandpass) network follows the SOM to keep the LO and RF signals from driving the IF amplifier. Additionally, the SOM was designed to oscillate at 5.15 GHz when driven from a 50 Ω generator while loaded with a 50 Ω termination. Consequently, input and output terminations that couple 50 Ω loads into the circuit at 5.15 GHz must be included between the SOM and the input filter and between the SOM and the output filter. The details of this SOM design are reported in applications note, AN-S005[2].

The final schematic is shown in Figure 5. A layout is shown in Figure 6. This board includes an output bandpass filter having 35 dB of isolation at the LO and 25 dB of isolation across the RF range, and an output 50 Ω, 5.15 GHz termination for the LO. It does not include any input filtering or terminations, nor does it include the dc blocking capacitors. All of these functions must be added for proper system operation. The dc bias is fed into the SOM through a bias stabilization resistor; the value of this resistor is selected to provide 35 mA of device current when driven from a +12 V supply line.



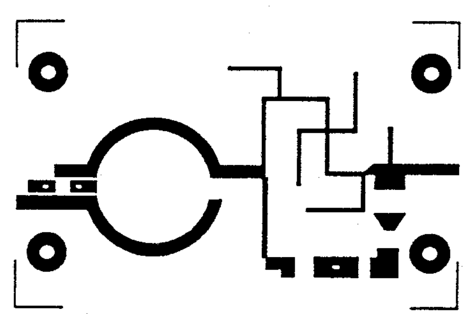
$\ell_1 = 90° \text{ @ LO}$

$\ell_1 + \ell_2 = 180° \text{ @ RF}$

$\angle S_{21} + \ell_2 + \ell_3 = 360° \text{ @ LO}$

Figure 5. RF Schematic of the SOM

The finished downconverter exhibits a typical conversion gain of 9 dB, a single side band noise figure of 13 dB, input and output VSWRs of less than 2.5:1, a 1 dB compression point of +8 dBm, and third order intercept point of +17 dBm.



Component Count:
1- Si MSF
1- PC Board
2- Resistors
1- Capacitor
1- Dielectric Puck
1- RF Choke (Optional)
2- Off Board Blocking Capacitors

Board Material = 1/32" Teflon-Fiberglass (ε = 2.55)

Figure 6. Actual Size SOM PC Board Including Output Low-Pass Filter

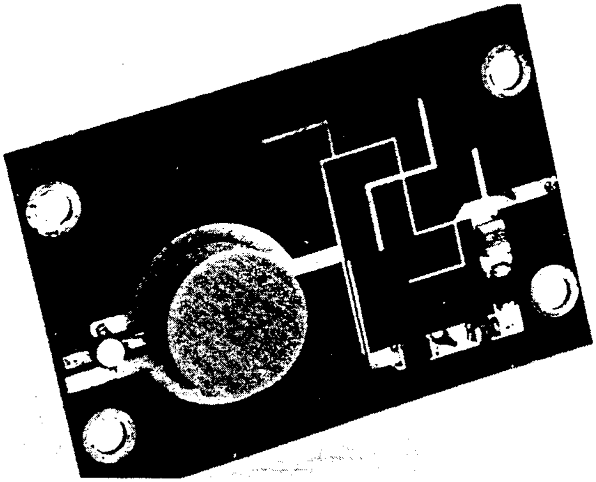


Figure 7. TVRO Circuit Board with Dielectric Puck

IF Design

The final portion of the design is an IF amplifier that increases the output signal level of the SOM to a suitable level to drive the electronics of a television receiver. Between 30 and 35 dB of power gain is needed; the frequency band is 450 to 950 MHz. This amplifier can be realized using plastic packaged MODAMP™ MMICs from HP. This product line is a family of Darlington bipolar amplifiers whose broadband impedance match is set through the use of both series and parallel resistive feedback. The MSA-0885 is selected as the highest gain for this application; a cascade of two of these devices can provide the needed 35 dB of power gain. Since it is desirable to create an IF amplifier with flat gain response across the IF band, some additional circuit elements are incorporated.

The concept for the flattened amplifier is to insert a frequency bypassed "T" pad between two MSA-0885s. Computer modeling quickly shows that the flattening scheme can be simplified, since the capacitors bypassing the arms of the "T" pad dominate the network's frequency response. Thus the flattening structure can be reduced to a series capacitor, a shunt resistor-inductor arm to ground, and a final series capacitor. Note that if the inductance in the shunt arm is realized using a printed transmission line. The added parts count for the flattened amplifier and consist of only one capacitor and one resistor – the second capacitor is needed to serve as a dc block between stages. Sections of 50 Ω transmission line and input and output dc blocking capacitors complete the RF design.

Each device is biased at a device current of 36 mA by dropping the 12 V supply voltage through an RF choke of .1μH in series with an appropriate bias stabilization resistor (111 Ω nominal); a 1μF bypass capacitor on the supply end of this network completes the bias circuitry.

The Touchstone circuit file describing this amplifier is given in Figure 8. The S parameters of the MSA-0885 are reproduced in Figure 9. The predicted gain performance and match are given in Figure 10. A schematic appears in Figure 11. Note that the design bandwidth if the IF amplifier is 450 MHz to 1.5 GHz. This allows the same IF amplifier to be used with either high side injection or low side injection in the frequency downconverter.

System Integration

A few words should be said about integrating the above circuit sections into the finished block converter. It is a good idea to RF shield the various sections of the design from each other. Interior walls surrounding each section should be used to keep the radiated energy from one circuit from being received by another portion of the system. One rule of thumb is to keep the gain in a single enclosure below 40 dB. To help eliminate moding, the cavity should be less than a half wavelength wide at the frequency of operation. A small rigid cavity around the oscillator also helps ensure frequency stability. The expansions and contractions of the housing and substrate that occur over temperature can have significant pulling effects on the oscillator frequency; smaller cavities are more rigid and will deform less, keeping the oscillator performance more consistent. The dc regulator circuitry should also be separated from the RF design, either in a separate cavity or on a separate board mounting on the back side of the RF board. Typical regulator circuitry is given in application note *AN-A002: Design of a 4 GHz LNA for a TVRO System.*

Note that epoxy glass was chosen as the substrate for both the LNA and the IF amplifier. A substrate such as RT Duroid would provide superior system performance due to lower loss and more consistent dielectric properties, and is the preferred board material if electrical performance is the overriding system constraint. Many manufacturers feel that in a market as price sensitive as C band TVRO, they must accept the poorer electrical performance of the less expensive epoxy glass substrates. There is less penalty in the IF stage when the board thickness is thin—1/16" thick board adds enough ground lead inductance in the via holes to affect amplifier gain rolloff at 1.5 GHz. The higher board losses and less consistent dielectric properties of epoxy glass probably result in .1 to .2 dB additional noise in the LNA. Although the SOM circuitry shown does use a Duroid substrate, it is probably appropriate to transfer this portion of the system onto epoxy glass as well. The resonator should be mounted on a small ring or piece of alumina that is mounted directly to the housing. This prevents oscillator frequency pulling that otherwise results from changes in the dielectric constant of the softboard over temperature.

```
! < 2A08G1_T >
! 450 - 1450 MHz AMPLIFIER USING 2 STAGES OF MSA-0885

VAR
        W1=100
        W2\60
        H1=31
CKT
        MSUB    ER=4.8  H=31  T=1  RHO=1  RGH=0     ! EPOXY GLASS

        SLC     1       2              L=.5  C=100
        MLIN    2       3              W^W1  L=100
        S2PA    3       4       41     A:\S_DATA\MODAMP\MSA0885N
        VIA     41      0              D1=20  D2=20  H^H1  T=1
        MLIN    4       5              W^W2  L=100
        SLC     5       6              L=.5  C\3.0
        SRL     6       61             R\25  L=.5
        MLIN    61      0              W=20  L\300
        SLC     6       7              L=.5  C\3.0
        MLIN    7       8              W^W2  L=100
        S2PA    8       9       91     A:\S_DATA\MODAMP\MSA0885N
        VIA     91      0              D1=20  D2=20  H^H1  T=1
        MLIN    9       10             W^W2  L=100
        SLC     10      11             L=.5  C=100
        DEF2P   1       11             IF
FREQ
        SWEEP   .3      1.6     .1
OUT
        IF      DB[S21] GR1
        IF      DB[S11] GR1A
        IF      DB[S22] GR1A
        IF      K
GRID
        GR1     0       40      5
        GR1A    0       -40
```

Figure 8. IF Amplifier Simulation

MSA-0885 S Parameters, I_D = 36 mA

Freq. GHz	S11		S21			S12			S22	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.64	-21	32.5	42.29	160	-36.5	.015	40	.61	-24
0.2	.58	-39	31.3	36.89	144	-32.8	.023	50	.54	-45
0.4	.44	-65	28.7	27.20	120	-29.4	.034	54	.42	-77
0.6	.36	-82	26.3	20.57	106	-27.2	.044	53	.33	-98
0.8	.31	-95	24.3	16.31	96	-25.2	.055	53	.28	-115
1.0	.27	-105	22.5	13.36	87	-24.2	.061	51	.25	-129
1.5	.24	-125	19.3	9.24	71	-21.4	.085	50	.18	-153
2.0	.26	-147	16.7	6.82	56	-19.7	.103	47	.15	-173
2.5	.29	-159	14.9	5.57	48	-18.4	.120	44	.12	180
3.0	.34	-175	13.1	4.51	37	-17.7	.130	42	.09	165
3.5	.38	172	11.6	3.80	25	-16.9	.144	37	.06	172
4.0	.42	161	10.1	3.21	14	-16.3	.153	33	.04	-139
5.0	.48	135	7.7	2.43	-7	-15.6	.167	24	.09	-90
6.0	.60	102	5.5	1.88	-29	-14.9	.179	17	.08	-140

Figure 9. S Parameters of MSA-0885 Used in IF Amplifier Design

Conclusions

The design of a C band TVRO block downconverter has been discussed. Circuitry has been developed for the LNA, a SOM for downconversion, and the IF amplifier. The total RF semiconductor part count for this system is three GaAs FETs and three bipolar MMICs, all of which are available from Avantek Semiconductor Division.

References

1. *Applications Note AN-A001: Design of a 4 GHz LNA for a TVRO System.*
2. *Applications Note AN-S005: Using HP MSF Series Silicon Bipolar MMIC Frequency Converters.*

FREQ -GHZ	DB[S21] IF	DB[S11] IF	DB[S22] IF	K IF
0.30000	36.121	-13.329	-10.729	121.588
0.40000	36.095	-13.650	-11.558	59.546
0.50000	36.594	-13.089	-11.732	29.657
0.60000	36.506	-12.713	-12.046	16.988
0.70000	36.765	-12.073	-12.149	9.777
0.80000	36.582	-11.906	-12.655	6.351
0.90000	36.565	-11.867	-13.722	4.719
1.00000	36.175	-12.050	-14.986	3.800
1.10000	36.170	-12.109	-15.306	2.879
1.20000	35.920	-12.404	-15.763	2.337
1.30000	35.445	-12.846	-16.314	2.010
1.40000	34.761	-13.330	-16.942	1.812
1.50000	33.878	-13.744	-17.660	1.697
1.60000	33.402	-13.928	-18.332	1.585

Figure 10. IF Amplifier Predicted Performance

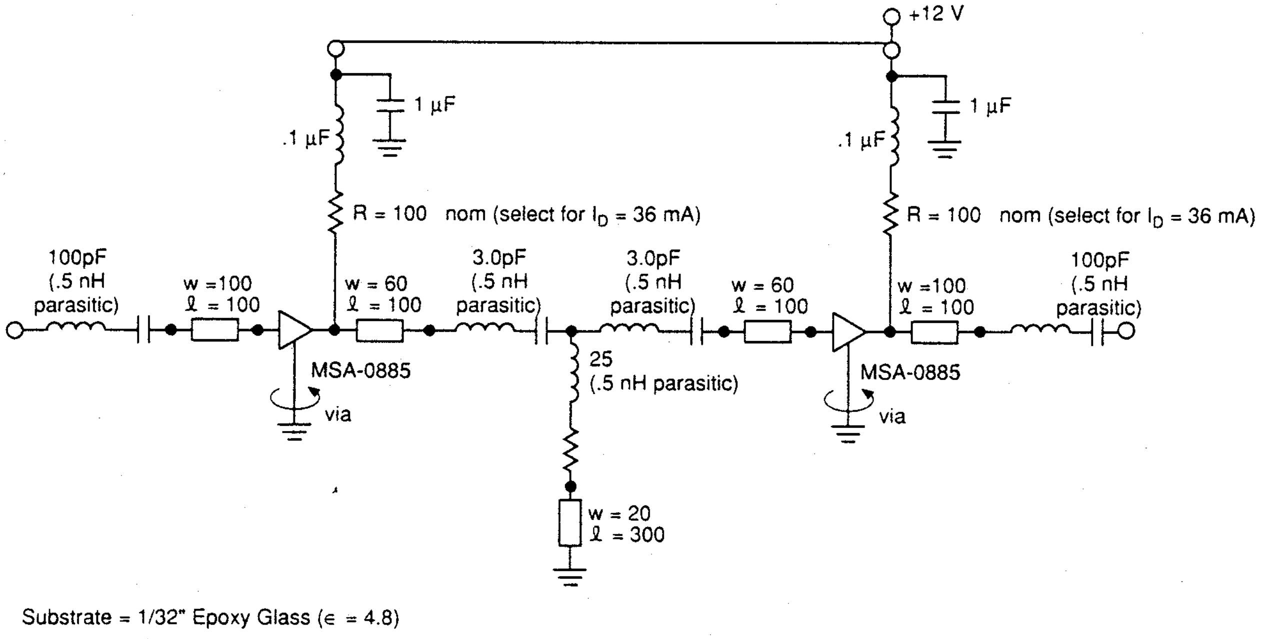


Figure 11. IF Amplifier Schematic

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