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COMPONENTS

APPLICATION NOTE 967

A Low Noise 4 GHz Transistor Amplifier Using the HXTR-6101 Silicon Bipolar Transistor

CONTENTS

SYMBOLS

$|S_{ij}|$ - Magnitude of S_{ij} where i, j equals 1,2

$\angle S_{ij}$ - Angle of S_{ij} where i, j equals 1,2

$|S_{ij}|^2$ - Power Ratio of S_{ij} where i, j equals 1,2

S_{11} - Input Reflection Coefficient

S_{12} - Reverse Transmission Gain

S_{21} - Forward Transmission Gain

S_{22} - Output Reflection Coefficient

S'_{22} - Output Reflection Coefficient with the source reflection coefficient being Γ_O

$Q(S'_{22})$ - Unloaded Quality Factor of S'_{22}

Z'_{22} - Equivalent Impedance of S'_{22}

K - Stability Factor

$G_{a(max)}$ - Maximum Available Power Gain

Γ_{MS} - Source Reflection Coefficient for $G_{a(max)}$

Γ_{ML} - Load Reflection Coefficient for $G_{a(max)}$

F_{MIN} - Minimum Noise Figure

M_{MIN} - Minimum Noise Measure

G_a - Associated Gain at F_{MIN}

R_n - Equivalent Noise Resistance

Z_{NF} - Equivalent Impedance of Γ_O

Γ_O - Optimum Source Reflection Coefficient for F_{MIN}

Γ_L - Load Reflection Coefficient for F_{MIN}

P_{1dB} - Power Output at 1 dB gain compression

P_{tune} - Input Power Level when tuned for maximum power output

η_c - Collector RF to DC Power Efficiency at 1dB gain compression

Γ_{PS} - Source Reflection Coefficient for P_{1dB}

Γ_{PL} - Load Reflection Coefficient for P_{1dB}

INTRODUCTION

A significant improvement in the producibility, consistency, noise figure and associated gain of low noise microwave bipolar transistors has been realized with Hewlett-Packard's development of a fully ion implanted device with sub-micron emitter widths. State-of-the-art noise performance is obtained with the chip mounted in the HPAC-70GT package (HXTR-6101).

The purpose of this application note is to describe in detail the design of a single-stage state-of-the-art low noise amplifier at 4 GHz. The design and construction of both the input and output matching networks of a microstrip amplifier will be described. The amplifier's 4 GHz performance is excellent, with a noise figure of 2.6 dB, an associated gain of 10.8 dB and a 4.5 dBm power output at 1 dB gain compression. The

third order intercept point is +17 dBm with an output VSWR of 1.29. An active biasing network is used for good temperature performance. Noise Figure and gain on the amplifier is presented over the temperature range of -55°C to +110°C. Although the design of theamplifier was for 4.0 GHz, the performance over the 3.7 to 4.2 GHz telecommunication band is very good.

The initial design goals are:

- Amplifier noise figure less than 3.0 dB
- Associated gain greater than 8 dB
- Noise measure less than 3.4 dB
- Output VSWR of less than 1.5:1

HPAC-70GT PACKAGE

The HXTR-6101 is supplied in the HPAC-70GT, a rugged co-fired alumina/kovar hermetic package. The unique feature of this patented package is that the closest external emitter connection on the package is the kovar top cap. The reduction in emitter inductance is a factor of two improvements over the HPAC-100. The typical value of emitter inductance to the kovar top cap is 0.09nH. This reduced inductance increases the high frequency performance of the packaged device.

The HXTR-6101 worst case thermal impedance is 250°C/W with the emitter top cap connected to a large heat sink. Use is made of the emitter top cap for both thermal and R.F. grounding.

DESIGN DATA

Plotted in Figure 1 is the typical noise figure, noise measure* and associated gain of the HXTR-6101 product as a function of collector current at 4 GHz.

From Figure 1, it can be seen that the minimum noise measure of the device is obtained at a collector current of 3 to 4 mA. However, the associated gain at noise figure is higher at 4mA, therefore a bias point of V_{CE} = 10 volts and I_C = 4 mA is chosen for low noise measure operation. At these bias conditions, the scattering, gain[1] and noise[2] parameters for the particular device used in this amplifier are:

Scattering Parameters

S_{11} = 0.552/169°
S_{12} = 0.049/23°
S_{21} = 1.681/26°
S_{22} = 0.839/-67°

Gain Parameters

k = 1.012
$G_{a(max)}$ = 14.7 dB
Γ_{MS} = .941/-154°
Γ_{ML} = .979/70°

Noise Parameters

F_{MIN} = 2.5 dB
Γ_O = .475/166°
R_n = 3.5 ohms

Using the Scattering and Noise Parameters above, the available power gain and noise contours are plotted in Figure 2. The contours are mapped onto the source impedance plane[2].

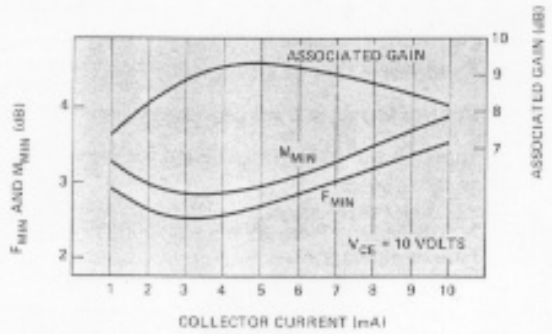


Figure 1. Typical Noise Figure and Associated Gain vs. Collector Current.

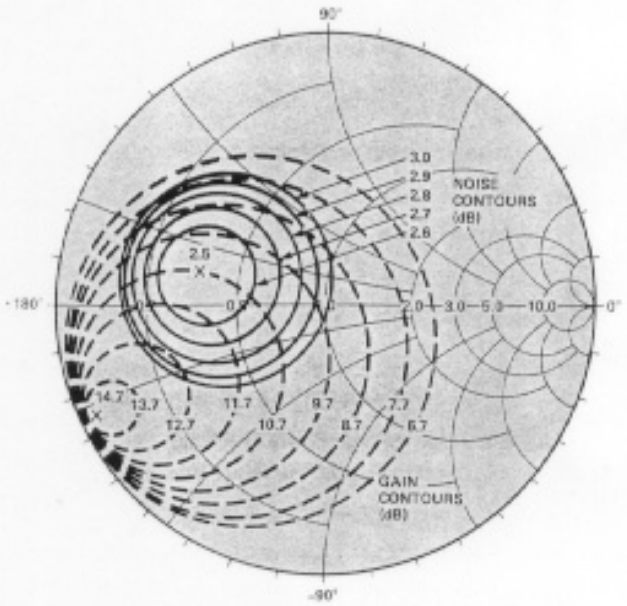


Figure 2. Noise and Gain Contours

Taking a closer look at the Noise Contours, it is seen that the optimum source reflection coefficient (Γ_O) for minimum noise figure (F_{MIN}) is not very sensitive to matching error. The diameter of the first noise contour corresponds to a change in reflection coefficient magnitude of .37 with a noise figure increase of 0.1dB. This characteristic of the HXTR-6101 is very advantageous to circuit designers tryingto match for minimum noise figure. From the two sets of contours, it appears that the associated gain at minimum noise figure will be approximately 11 dB with the output seeing a conjugate match.

Since the design goal is to construct a low noise amplifier, the optimum noise measure bias condition is selected. There is also an optimum bias condition for maximum gain and another for output power. Even at the optimum noise mea-

*The system noise figure of an infinite cascaded chain of identical amplifier stages. For further explanation, see Hewlett-Packard application bulletin #9.

$$M_{MIN} = 10 \log_{10} \left[1 + \frac{F_{MIN} - 1}{1 - \frac{1}{G_a}} \right]$$

sure bias there are trade-offs between noise figure, gain and power output due to source and load impedance.

At the optimum noise measure bias of V_{CE} = 10 volts and I_C = 4mA, the source and load reflection coefficients for lowest noise figure, maximum gain and greatest power are tabulated and plotted in Figure 3. Figure 3 is plotted for the particular device used in this amplifier design. The source and load reflection coefficients are mapped onto the source or load impedance plane.

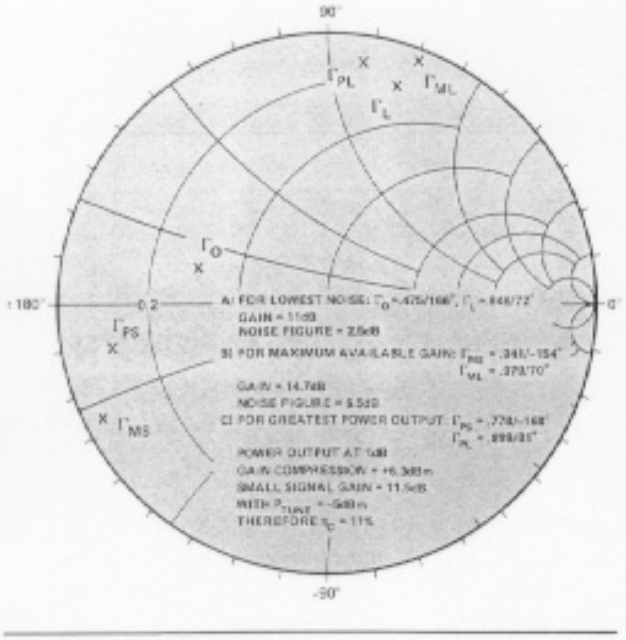


Figure 3. Matching Tradeoffs

INPUT MATCHING NETWORK

The main purpose of the input matching network is to provide the optimum source impedance for minimum noise figure. The basic design philosophy in realizing this network is:

1) Convert the optimum source reflection coefficient (Γ_O) to impedance.
2) From this impedance determine the equivalent admittance.
3) The susceptance component is realized with a short circuited eighth-wave ($\frac{\lambda}{8}$) length stub.
4) The conductance component is realized with a quarter-wave ($\frac{\lambda}{4}$) length impedance transformer.

The realization and Smith Chart mapping for this input matching network is described below and shown in Figure 4.

1) The impedance Z_{NF}, corresponding to $\Gamma_O = .475/166^\circ$ is:

$$Z_{NF} = \frac{(1 - |\Gamma_O|^2)\,50}{1 + |\Gamma_O|^2 - 2|\Gamma_O| \cos \angle\Gamma_O} + \frac{j\,(2|\Gamma_O| \sin \angle\Gamma_O)\,50}{1 + |\Gamma_O|^2 - 2|\Gamma_O| \cos \angle\Gamma_O}$$

$$Z_{NF} = 18.0 + j\,5.35$$

2) $Y_{NF} = \frac{1}{Z_{NF}} = 0.0510 - j\,0.0152$

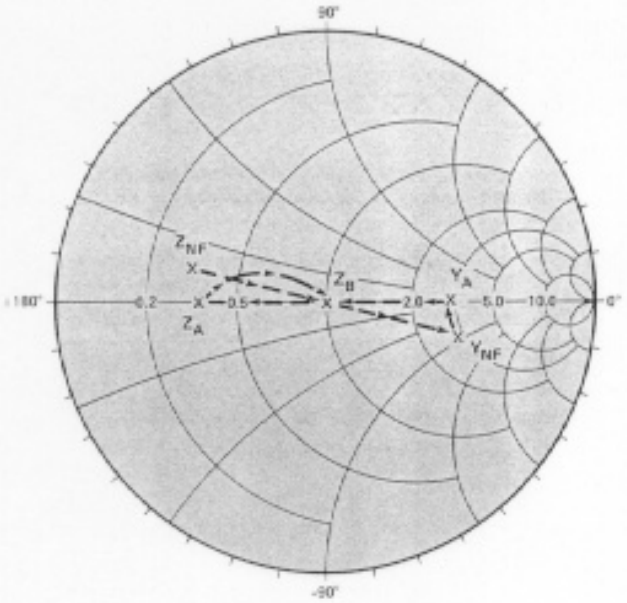
3) A short circuited stub less than a quarter-wave length long looks like a shunt inductor of impedance $Z = jZ_O \tan \beta\ell$. Hence a short circuited stub that is an eighth-wave length long looks like a shunt inductor of impedance jZ_O where Z_O is the characteristic impedance of the stub. Hence

$$Z_O = \frac{1}{.0152} = 65.8 \text{ ohms.}$$

4) Since the driving source impedance is 50Ω, a quarter-wave transformer of characteristic impedance:

$Z'_O = \sqrt{(50)\,(19.6)} = 31.31\Omega$

completes the input matching network.



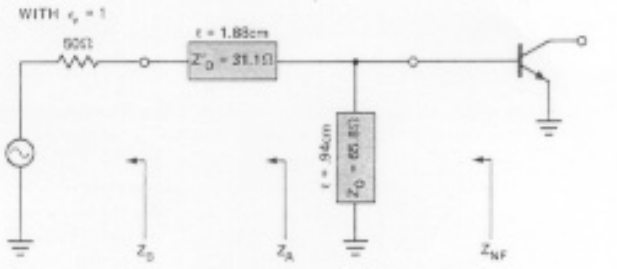


Figure 4. Input Matching Network

OUTPUT MATCHING NETWORK

With one of the design goals being an output VSWR of less than 1.5:1, the output matching network is designed to provide a conjugate match with the source impedance, Z_{NF}. The basic design procedure is:

1) Calculate S'_{22}, the output reflection coefficient with the source reflection coefficient being Γ_O.
2) Provide a conjugate match for the output with a load reflection coefficient equal to S'^*_{22}. ($\Gamma_L = S'^*_{22}$)
3) The matching section could be realized with a shunt stub and a series transformer similar to the input network. However, in order to increase the tuning capabilities of the network, an extra section of matching is used.

The realization and Smith Chart mapping of this output network is described below and shown in Figure 5.

1) From the S-Parameters on the device, S'_{22} can be calculated as follows:

$$S'_{22} = S_{22} + \frac{S_{21}\, S_{12}\, \Gamma_O}{1 - S_{11}\, \Gamma_O}$$

$$\therefore S'_{22} = .846\ \angle -72^\circ$$

Now, providing a conjugate match to S_{22}' for a good output VSWR, the load reflection coefficient (Γ_L) should be:

$$\Gamma_L = .846 \angle 72^\circ$$

2) A problem with the output is the relatively high Q. This can cause problems in supplying a conjugate load match to obtain a good output VSWR because of sensitivity to small dimensional changes. Calculating this output Q gives us,

$$Q\,(S'_{22}) = 5.65$$

With this dominant Q, the calculated 3 dB bandwidth (B.W.) is:

$$100 \times \frac{B.W.}{f_O} = \frac{100}{Q\,(S'_{22})} = 18\%$$

This bandwidth equals 720 MHz with a center frequency (f_O) of 4 GHz.

3) A 0.61 cm ($2\beta\ell = 59^\circ$) equivalent air length of Z_O=50Ω transmission line was added to the output to provide an output soldering area. The rotated output reflection coefficient is:

$$\Gamma_1 = .846/-131^\circ$$

The corresponding impedance, Z_1, is

$$Z_1 = \frac{(1 - |\Gamma_1|^2)\ 50}{1 + |\Gamma_1|^2 - 2|\Gamma_1| \cos \angle\Gamma_1} + \frac{j\,(2\,|\Gamma_1|\, S_{in}\, \angle\Gamma_1)\ 50}{1 + |\Gamma_1|^2 - 2|\Gamma_1| \cos \angle\Gamma_1}$$

$$Z_1 = 5.03 - j\ 22.6$$

$$Y_1 = \frac{1}{Z_1} = 9.35 \times 10^{-3} + j.0422$$

4) A short circuited stub an eighth-wave length long looks like a shunt inductor of admittance, $-j\ Y_O$. The purpose of this shunt stub is to tune out most of the susceptance component in the admittance Y_1. A tuning section will be added to further match the output.

A convenient characteristic admittance, $Y_O = 0.0345$ ℧ is used for the shunt stub.

$$Y_2 = 9.35 \times 10^{-3} + j\ .0422 - j\ .0345 = 9.35 \times 10^{-3} + j\ .0077$$

$$Z_2 = \frac{1}{Y_2} = 63.7 - j\ 52.5$$

5) The next element is a transformer to obtain an admittance with real part matched to the 50 ohm load. This is accomplished with an 80 ohm line 1.35 cm long. (ϵ_r=1) ($\beta\ell = 64.8^\circ$)

$$Z_3 = \frac{Z_O\,(Z_2 + j\ Z_O \tan \beta\ell)}{(Z_O + j\ Z_2 \tan \beta\ell)}$$

$$Z_3 = 39.12 + j\ 21.1$$

$$Y_3 = \frac{1}{Z_3} = .02 - j\ .0107$$

6) An open stub is chosen to provide some tuning capability. An open circuited stub less than a quarter-wave length long looks like a shunt admittance $Y = j\ Y_O \tan \beta\ell$. An open circuited stub of characteristic admittance Y_O = .039 ℧ and length 0.4 cm ($\epsilon_r = 1$) ($\beta\ell = 19.2^\circ$) is added.

It's susceptance is .039 tan 19.2° = .0136 ℧

$$Y_4 = .02 - j\ .0107 + j\ .0136 = .02 + j\ .0029$$

$$Z_4 = \frac{1}{Y_4} = 50 - j\ 7.1$$

7) Now Z_4 is matched with a transformer with a characteristic impedance of 80 Ω and length of .19 cm (ϵ_r = 1) ($\beta\ell = 9.12^\circ$)

$$Z_5 = \frac{Z_O\,(Z_4 + j\ Z_O \tan \beta\ell)}{(Z_O + j\ Z_4 \tan \beta\ell)} = 50\,\Omega$$

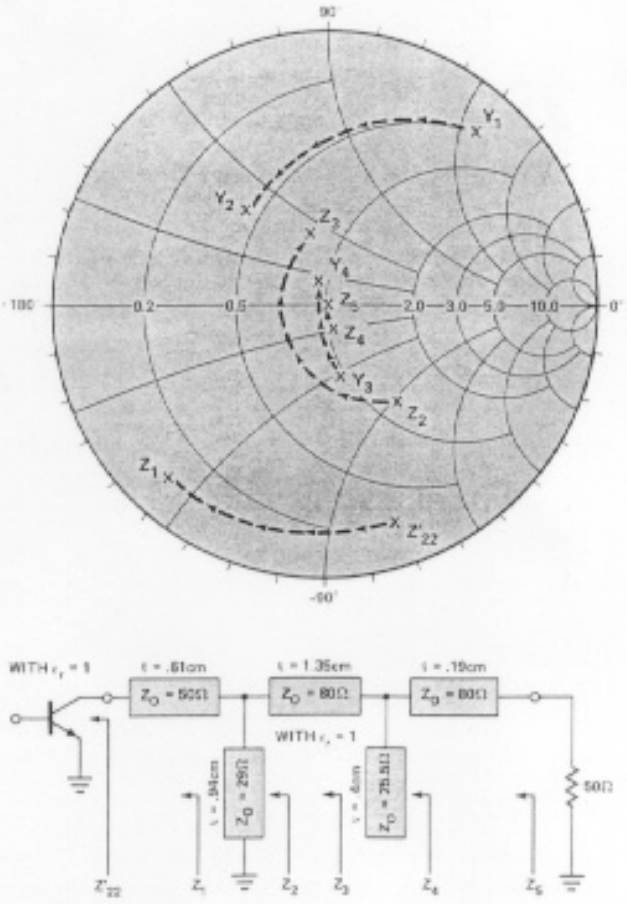


Figure 5. Output Matching Network

The output tuning section as described has the flexibility for tuning in four areas:

- Adjusting the length of the series line
- Changing the width or characteristic impedance of the open circuited shunt stub
- Modifying the length of the shunt stub
- Varying the length of the final series line

This completes the design of the output matching network.

COMPUTER SIMULATION

With the S-Parameters for the particular device used, the input and output matching networks were modeled as simulated on a circuit analysis program. The results of this simulation yield the following results:

S_{11} = .620/51.2°
S_{21} = 11.04dB/–113.8°
S_{12} = –19.67dB/–116.8°
S_{22} = .089*/–87.3

or

Input VSWR = 4.26
Gain = 11.04dB
Isolation = –19.67dB
Output VSWR = 1.20*

*The output VSWR is not 1.00 because of round off error in design.

PERFORMANCE

An amplifier was constructed using the design derived above. A comparison of the computer simulation with measured amplifier performance at 4 GHz is shown below.

Parameter	Measured Performance	Design Goal	Computer Simulation
Gain	10.8 dB	8.0 dB (MIN.)	11.0 dB
Input VSWR	3.57	–	4.26
Output VSWR	1.29	1.50 (MAX.)	1.20
Isolation	–24 dB	–	–19.7 dB
Noise Figure	2.60 dB*	3.0 dB (MAX.)	–
Noise Measure	2.77 dB	3.4 dB (MAX.)	–

*Device Noise Figure is 2.5 dB

Although the design of the amplifier was for low noise performance at 4.0 GHz, the performance over the 3.7 to 4.2 GHz telecommunication band is very good.

Figures 6, 7 and 8 show the room temperature performance of the amplifier.

Phase Linearity - Phase linearity is ±5° over the entire 500 MHz band width.

Isolation - Isolation is better than –24 dB over the entire 3.7 to 4.2 GHz band.

AM to PM Conversion - With an output power level of - 13 dBm, the input power level is referenced. At this input reference level, the input power is varied ± 10dBm. Over the 3.7 to 4.2 GHz band, the AM to PM conversion is less than 0.13°/dB.

Third Order Intercepts - With two fundamental signals injected into the input at 3.95 and 4.05 GHz, the output power level for each fundamental signal is set at 0 dBm. The third order intermodulation products are both -34 dB below the two fundamentals at the output. Therefore, the third order intercept point is + 17 dBm.

Spurious Outputs - With a 4 GHz, 0 dBm input signal injected into the amplifier, no spurious signals were detected above –60 dBm over the 2 to 6 GHz band.

Group Delay - The group delay over the entire 500 MHz bandwidth is less than .53 n sec.

Wideband gain performance is plotted in Figure 9.

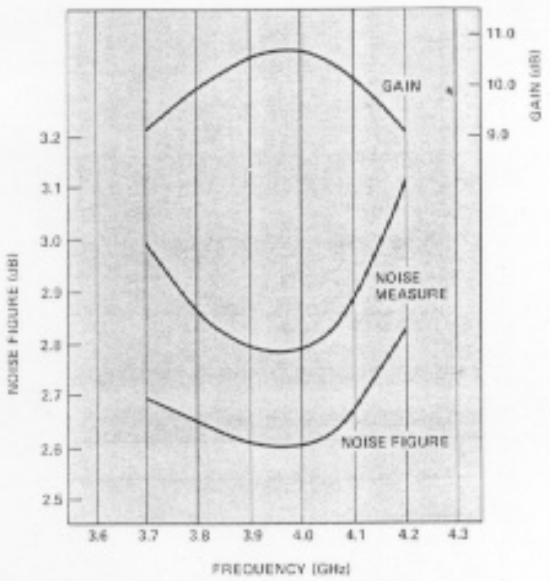


Figure 6. Noise and Gain Performance.

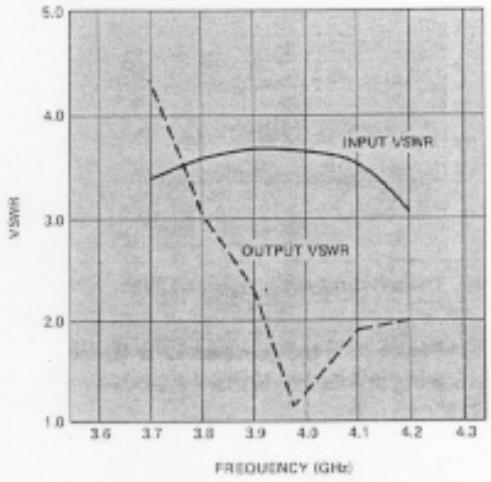


Figure 7. Input – Output VSWR Performance.

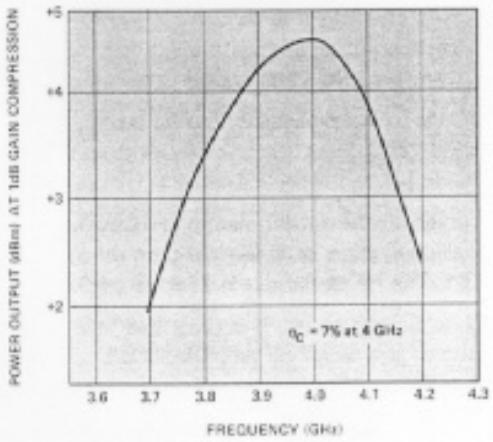


Figure 8. Power Output Performance.

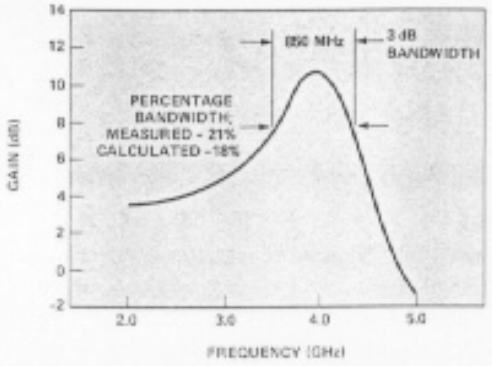


Figure 9. Wideband Gain Performance.

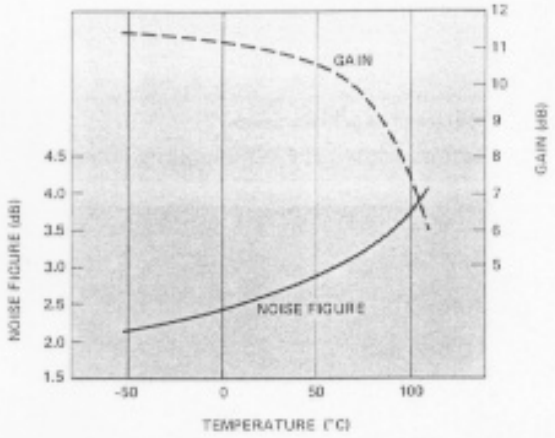


Figure 10. Temperature Performance at 4 GHz.

Plotted in Figure 10 is the gain and noise figure performance of the amplifier at 4 GHz over the temperature range of -55° C to +110° C.

CONSTRUCTION

The board material is .031" RT/Duroid 120-061 (D5880), with 1 oz copper clad on two sides. The relative dielectric constant (ϵ_r) is 2.23. Duroid was chosen because of its low loss tangent. The thickness of .031" was chosen so the emitter top cap could be soldered to the RF ground, thereby taking advantage of the low emitter inductance.

To minimize transition interactions between the series transmission lines and shunt stubs, the shunt stubs were balanced along the series transmission lines.

Some tuning on the output matching network was required. The final realization of this circuit on duroid is shown in Figure 11. The RF board size is 2 inches by 0.9 inches.

The active biasing network is described in Appendix C. A schematic of the complete amplifier and biasing circuit can be seen in Figure 12.

Pictures of the assembled amplifier can be seen in Figures 13 and 14. The amplifier draws 4.4mA from a 15 volt D.C. power supply.

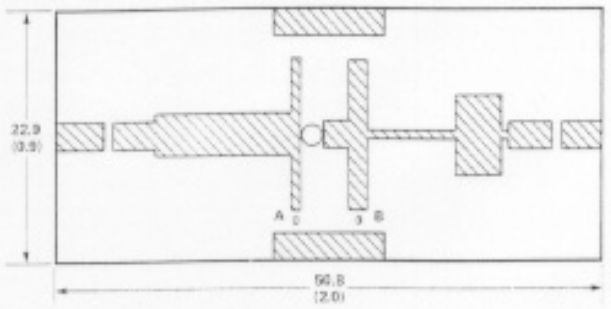


Figure 11. R.F. Board Layout.

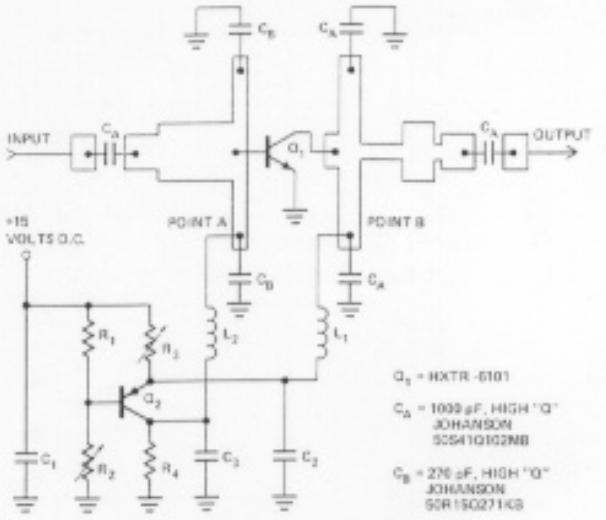


Figure 12. Complete Amplifier Schematic.

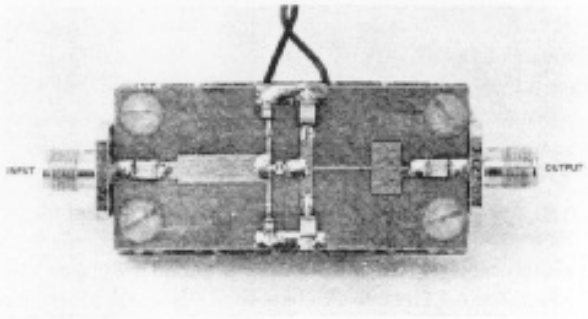


Figure 13. Amplifier – Top View.

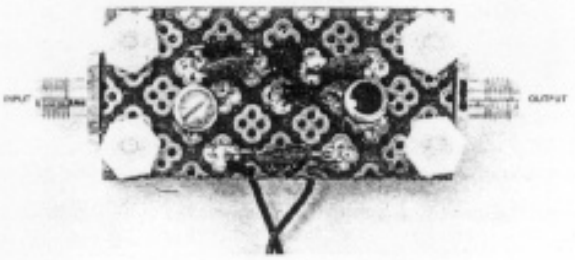


Figure 14. Amplifier – Bottom View.

APPENDIX A
SCATTERING PARAMETERS VERSUS COLLECTOR CURRENT AT 4 GHz.

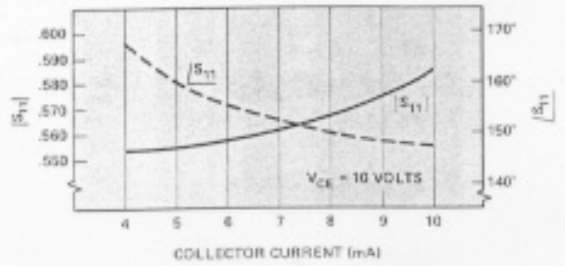


Figure A1. S_{11} – Input Reflection Coefficient.

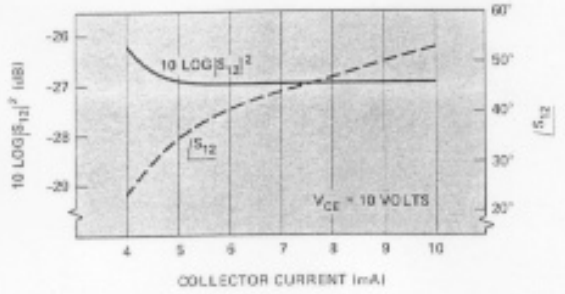


Figure A2. S_{12} – Reverse Transmission Gain.

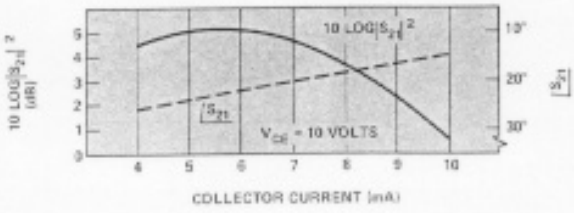


Figure A3. S_{21} – Forward Transmission Gain.

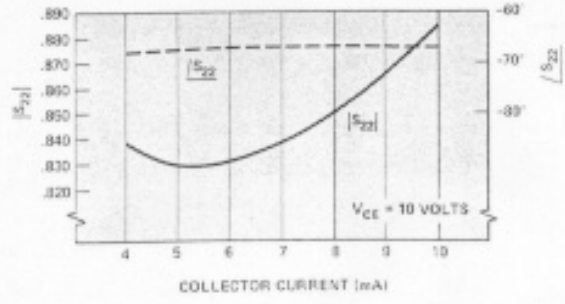


Figure A4. S_{22} – Output Reflection Coefficient.

APPENDIX B
NOISE PARAMETERS VERSUS COLLECTOR CURRENT AT 4 GHz.

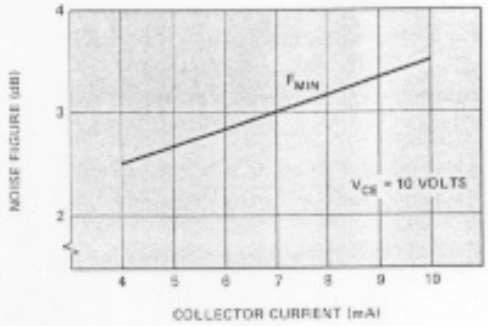


Figure B1. F_{MIN} – Minimum Noise Figure.

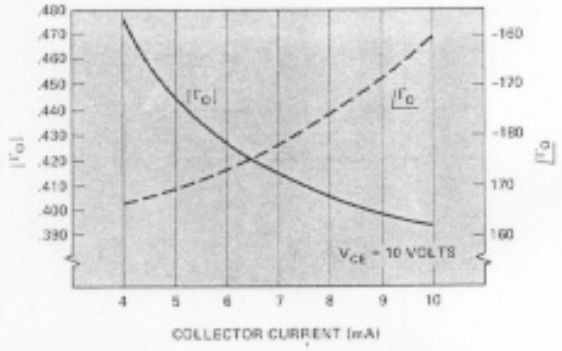


Figure B2. Γ_O – Optimum Source Reflection Coefficient for F_{MIN}.

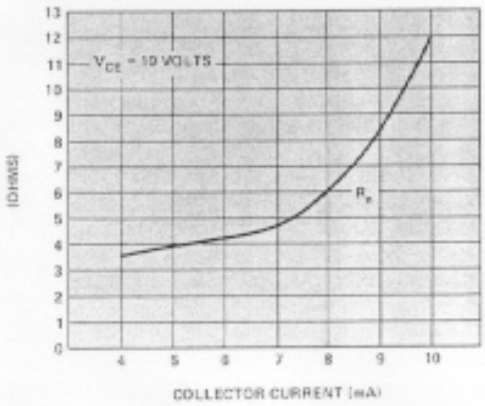


Figure B3. R_n – Equivalent Noise Resistance.

APPENDIX C

AN ACTIVE D.C. BIASING NETWORK

The purpose of a bias circuit is to hold the quiescent point constant. A resistor network could be used with good results over a moderate temperature range. For this particular amplifier an active biasing network was used to maintain a relatively constant quiescent point over a temperature range of -55°C to +110°C. The noise figure and gain of the constructed amplifier was measured over this temperature range (Figure 10).

With a power supply voltage of +15 volts chosen for the amplifier, the active biasing network is shown below along with the components used:

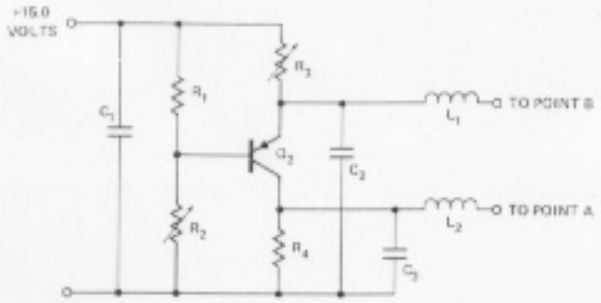


Figure C1.

Element	Value
R_1	100 KΩ, ¼W
R_2	200 KΩ, 1W, potentiometer
R_3	5 KΩ, 1W, potentiometer
R_4	2.61 KΩ, ¼W
C_1	.01μF, 100v, disc.
C_2	.002μF, 250v, disc.
C_3	.01μF, 100v, disc.
L_1	2 turns #36 enameled wire on .1" core (air)
L_2	2 turns #36 enameled wire on .1" core (air)
Q_2	$H_{FE} \geq 75$, $f_T > 150$ MHz, $BV_{CEO} \geq 30$V, $I_{C\,max} \leq 50$mA, $P_D \leq 300$ mW, PNP Silicon, Plastic.

The quiescent point is adjusted by R_2 and R_3. R_2 is adjusted to provide the proper V_{CE} voltage and R_3 is adjusted to supply the correct collector current (I_C).

Further explanation on this active biasing network may be found in Hewlett-Packard's Application Note 949-1, Page 5.

APPENDIX D

PARAMETERS AT VARIOUS BIAS CONDITIONS AT 4 GHz

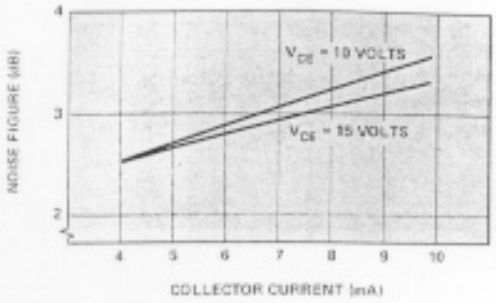


Figure D1. Noise Figure vs. Collector – Emitter Voltage.

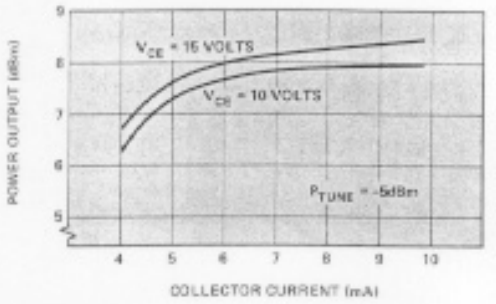


Figure D2. Power Output at 1 dB Gain Compression vs. Collector – Emitter Voltage.

REFERENCES

1. Hewlett-Packard Application Note 95-1, "S-Parameter Techniques for faster, more accurate Network Design", September 1968, Page 12.
2. Hewlett-Packard Application Note 154, "S-Parameter Design", April 1972, Pages 26 and 27.

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