HEWLETT PACKARD

APPLICATION NOTE 966

Applications of the HP HDSP-2000 Alphanumeric Display

This note is intented to serve as a design and application guide for users of the HP HDSP-2000 alphanumeric display device. The information presented will cover: the theory of the device design and operation; considerations for specific circuit designs; thermal management, power derating, and heat sinking; and intensity modulation techniques.

The HP HDSP-2000 device has been designed to provide a high resolution information display subsystem. Each character of the 4 character package consists of a 5x7 array of LEDs which can display a full range of alphabetic and numeric characters plus punctuation, mathematical and other special symbols.

Each character is 3.8mm high by 2.2mm wide with 4.5mm center to center spacing. The overall package size is designed to allow end stacking of multiple clusters to form character strings of any desired length.

ELECTRICAL DESCRIPTION

The on-board electronics of the HP HDSP-2000 display will eliminate some of the classical difficulties associated with the use of alphanumeric displays. Traditionally, single digit LED dot matrix displays have been organized in an x-y addressable array requiring 12 interconnect pins per digit plus extensive row and column drive support electronics. The HP HDSP-2000 provides on-board storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4 character display. This approach allows the user to address each display package through just 11 active interconnections vs. the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Figure 1 is a block diagram of the internal circuitry of the HP HDSP-2000 display. The device consists of four LED matrices and two 14-bit serial-in-parallel-out shift registers. The LED matrix for each character is a 5x7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. The 7 row cathode commons of each character are tied to the constant current sinking outputs of 7 successive stages of the shift register. The like columns of the 4 characters are tied together and brought to a single address pin (i.e., column 1 of all 4 characters is tied to pin 1, etc.). In this way, any diode in the four 5x7 matrices may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

The serial-in-parallel-out (SIPO) shift register has a constant current sinking output associated with each shift register stage. The output stage is a current mirror design with a nominal current gain of 10. The current to the reference diode is established from the output voltage of the brightness input buffer applied across the current reference resistors, R. The reference current flow is controlled by a switching transistor tied to the output of the associated shift register stage. A logical 1 loaded into the shift register will turn the current source "ON" thereby sinking current from the row line. A voltage applied to the appropriate column input will then turn "ON" the desired diode.

Data is loaded serially into the shift register on the high to low transition of the clock line. The data output terminal is a TTL buffer interface to the 28th bit of the shift register (i.e., the 7th row of character 4 in each package). The Data Output is arranged to directly interconnect to the Data Input on a succeeding 4 digit HP HDSP-2000 display package. The Data, Clock and V_B inputs are all buffered to allow direct interface to any TTL or DTL logic family.

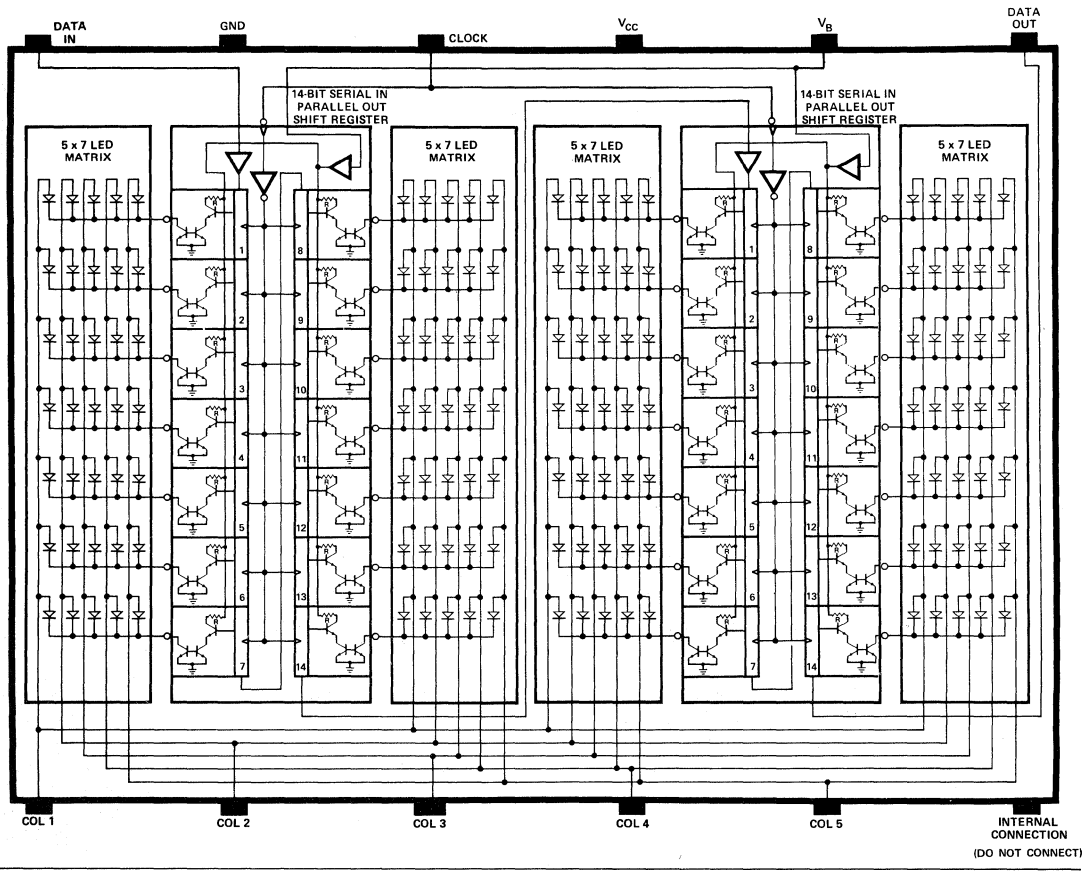


Figure 1. Block Diagram of the HDSP-2000.

THEORY OF OPERATION

Dot matrix aplhanumeric display systems generally have a logical organization which prescribes that any character be generated as a combination of several subsets of data. In a 5x7 matrix, this could be either 5 subsets of 7 bits each or 7 subsets of 5 bits each. This technique is utilized to reduce from 35 to 5 or 7 the number of outputs required from the character generator. In order to display a complete character, these subsets of data are then presented sequentially to the appropriate locations of the display matrix. If this process is repeated at a rate which insures that each of the appropriate matrix locations is re-energized, a minimum of 100 times per second, the eye will perceive a continuous image of the entire character. The apparent intensity of each of the display elements will be equal to the intensity of that element during the "ON" period multiplied by the ratio of "ON" time to refresh period. This ratio is referred to as the display duty factor, and the technique is referred to as "strobing". In the case of the HP HDSP-2000, each character is made up of 5 subsets of 7 bits. For a four character display, 28 bits representing the first subset of each of the four characters are loaded serially into the on-board SIPO shift register and the first column is then energized for a period of time, T. This process is then repeated for columns 2 through 5.

If the time required to load the 28 bits into the SIPO shift register is t, then the duty factor is:

$$D.F. = \frac{T}{5(t+T)} \; ; \qquad (1)$$

the term 5(t+T) is then the refresh period. For a satisfactory display, the refresh period should be:

$$1/[5(t+T)] \geqslant 100 \text{ Hz} \qquad (2)$$

or conversely

$$5(t+T) \leqslant 10 \text{ msec}, \qquad (3)$$

which gives

$$(t+T) \leqslant 2 \text{ msec}. \qquad (4)$$

Two milliseconds then is the maximum time period which should be allowed for loading and display of each column location. For $t \ll T$, the duty factor will approach 20%. The number of digits which can be addressed in a single string is then dependent upon the minimum acceptable duty factor and the choice of clock rate. For instance, at 1 MHz clock rate, a 100 character string of 25 packages could be operated at a duty factor of

$$D.F. = \frac{(T+t) - (\text{No. of bits to be loaded}) \times (1/1\ \text{MHz})}{5(T+t)}$$

$$= \frac{(2\ \text{msec}) - (700)\ (1\mu\text{sec})}{5 \times 2\ \text{msec}} = 13\%$$

For most applications, a duty factor of 10% or greater will provide more than satisfactory display intensity. In brightly illuminated ambient environments, a higher duty factor may be desirable whereas, in dim ambient situations, the duty factor may have to be reduced in order to provide a display with satisfactory contrast.

DRIVE CIRCUIT CONCEPTS

A practical display system utilizing the HP HDSP-2000 display requires interfacing with a character generator and refresh memory. A block diagram of such a display system is depicted in Figure 2. In explanation, assume that this system is for a four character display. Therefore, the 1/N counter becomes a 1/4 counter where N is equal to the number of characters in the string. The refresh memory is utilized to store the information to be displayed. Information can be coded in any one of several different standard data codes, such as ASCII or EBDIC, or the code and the display font can be customized through the use of a custom coded ROM. The only requirement is the output data be generated as 5 subsets of 7 bits each. The character generator receives data from the refresh memory and outputs 7 display data bits corresponding to the character and the column select data input. This data is converted to serial format in the parallel to serial shift register for clocking into the HP HDSP-2000 display shift register. In the typical system, the right most character to be displayed is selected first and the data corresponding to the ON and OFF display elements in the fist column is clocked into the first 7 shift register locations of the HP HDSP-2000. In a similar manner, column 1 data for characters 3, 2, and 1 is selected by the 1/N counter, decoded and shifted into the display shift register. After 28 clock counts, data for each character is located in the HP HDSP-2000 shift register locations which are associated with the 7 rows of the appropriate LED matrix. The 1/N counter overflows, triggering the display time counter, enabling the output of the 1/5 column select decoder and disabling the clock input to the HP HDSP-2000. The information now present in the shift registers will be displayed for a period, T, at the column 1 location. At the end of the display period, T, the divide by 5 counter which provides column select data for both the HP HDSP-2000 and the character generator is incremented one count and column 2 data is then loaded and displayed in the same manner as column 1. This process is repeated for each of the 5 columns which comprise the 5 subsets of data necessary to display the desired characters. After the fifth count, the 1/5 decoder automatically resets to one and the sequence is repeated. The only changes required to extend this interface to character strings of more than 4 digits are to increase the size of the refresh memory and to change the divide by four counter to a modulus equal to the number of digits in the desired string.

Since data is loaded for all of the like columns in the display string and these columns are then enabled simultaneously, only five column switch transistors are required regardless of the number of characters in the string. The column switch transistors should be selected to handle approxmately 110mA per character in the display string. The collector emitter saturation voltage characteristics and column voltage supply should be chosen to provide a $2.6V \leqslant V_{COL} \leqslant V_{CC}$. To save on power

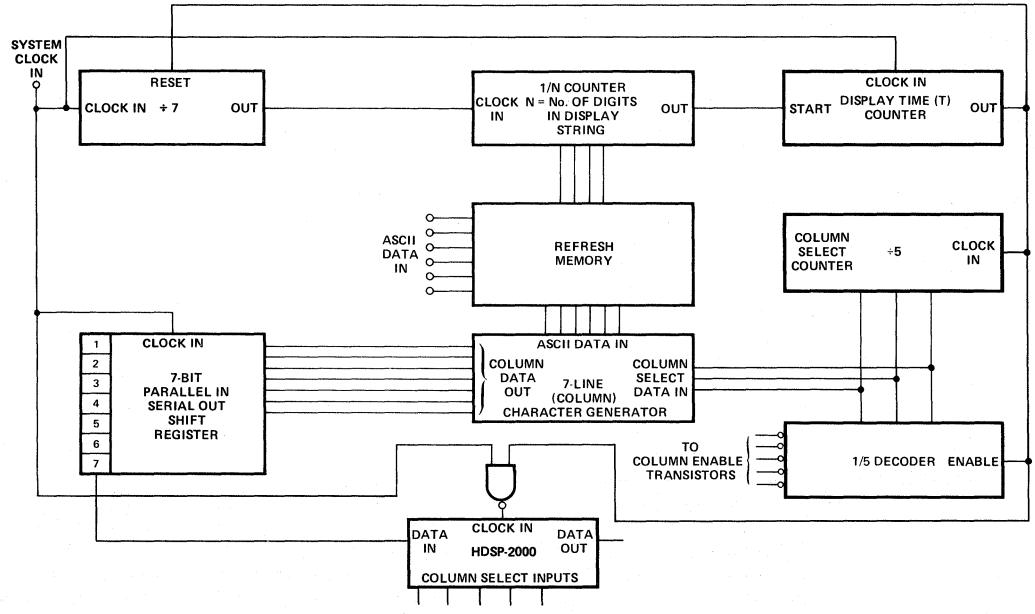


Figure 2. Block Diagram of a Basic Display System.

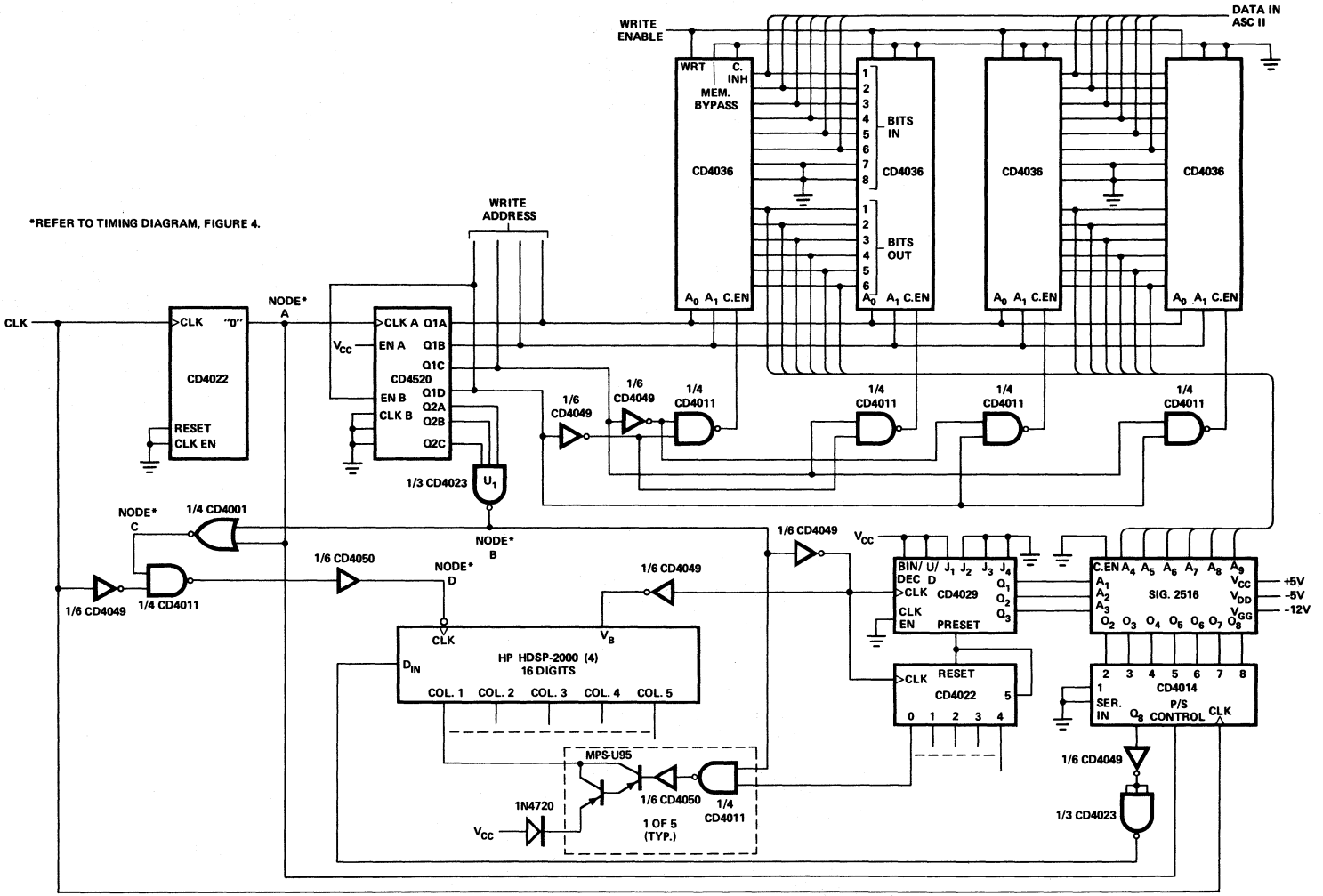


Figure 3. 16 Character CMOS Logic Interface to the HP HDSP-2000.

supply costs and improve efficiency, this supply may be a fullwave rectified unregulated DC voltage as long as the PEAK value does not exceed the value of V_{CC} and the minimum value does not drop below 2.6 volts.

Since large current transients can occur if a column line is enabled during data shifting operations, the most satisfactory operation will be achieved if the column current is switched off before clocking begins. I_{CC} will be reduced by about 10-15% if the clock is held in the logical 1 state during the display period, T.

INTERFACE CIRCUITS FOR THE HP HDSP-2000

There are many possible practical techniques for interfacing to the HP HDSP-2000 alphanumeric display. Three basic approaches will be treated here.

Instrumentation Interface Circuit

The circuit shown in Figure 3 is for a 16 character display and is designed to function primarily as a readout for general instrumentation systems. CMOS logic circuitry is utilized in this design, however, it should be a simple exercise to substitute TTL functions if CMOS is not desired. In this circuit, a CD4022 and CD4520 are combined to perform the functions of the divide by 7, divide by 16 (1/N) and display time counters as depicted in Figure 2. The timing diagram, Figure 4, demonstrates the relationship of the various critical outputs and inputs. The CD4022 actually acts here as a divide by 8 counter with the first count used to latch data into the parallel-in-serial-out (PISO) shift register and the other 7 counts shifting data out of the PISO and into the HP HDSP-2000. The CD4520 is a dual 4 bit counter wired as an 8 bit binary ripple counter. The NAND gate, U_1, establishes the ratio of loading time to display time. In this case, loading will occur once in every 8×2^7 clock counts for a period of 8×2^4 clock counts. Duty factor is then from (1)

$$\text{D.F.} = \frac{(8 \times 2^7) - (8 \times 2^4)}{5\,(8 \times 2^7)} = 17.5\% \quad (1)$$

and the refresh period is

$$5\,(8 \times 2^7)\,\tau,$$

where τ = clock period.

The four least significant bits of the CD4520 counter are used to continually address the CD4036 refresh memory. Data can be written into the desired memory address by strobing the WRITE ENABLE line when the appropriate memory address appears on the WRITE ADDRESS lines. This function can occur simultaneously with a read from memory.

Two counters, a CD4029 and a CD4022, are used for the column data generator and the column select decoder, respectively. Note that the Signetics 2516 character generator requires column select inputs of binary codes 1 to 5 instead of binary 0 to 4. For this reason, the CD4029 is preset to a binary 1 by the same pulse which is used to reset the CD4022 column select decoder. To minimize I_{CC}, the V_B terminal is held low during data load operations, turning "OFF" the current mirror reference current. The column current switch is a PNP Darlington transistor driven from a buffered NAND gate. The 1N4720 serves to reduce the column voltage by approximately 1 volt, thereby reducing on board power dissipation in the HP HDSP-2000 devices. Due to maximum clock rate limitations of the CMOS logic, clock input should not exceed 1 MHz.

32 Character Keyboard Interface Circuit

The circuit shown in Figure 5 will directly interface the HP HDSP-2000 display to most standard keyboards. Interfac-

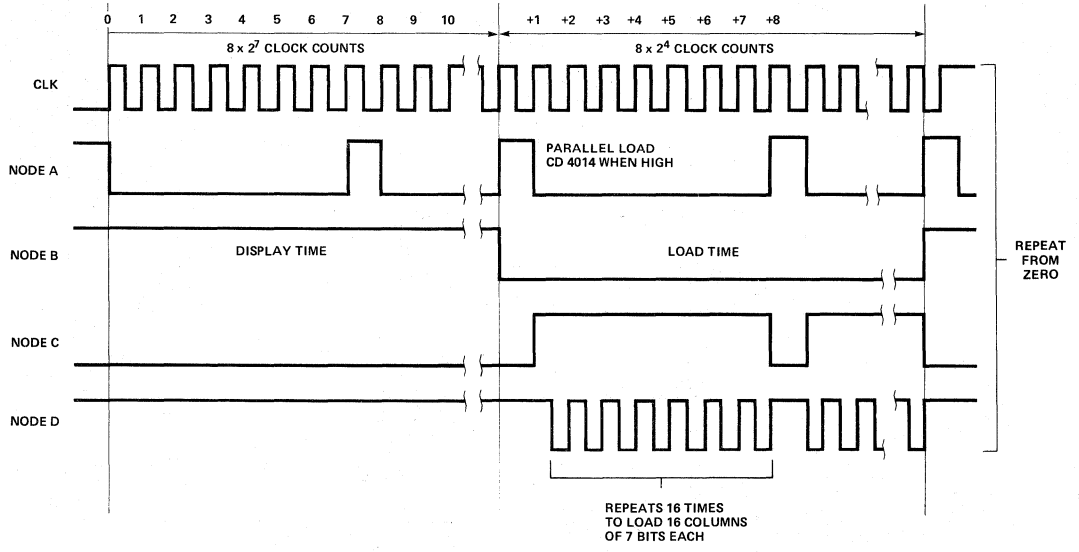


Figure 4. Timing Diagram for Display Interface.

ing to a keyboard without a "smart" system to generate some of the special functions required can result in some unique problems which must be considered. This system provides the following special features:

- Provides a cursor to indicate the position in the line of the next character to be entered.
- Blanks all data to the right of the cursor in the display.
- Provides for external display blanking and intensity control.
- Implements "Return" and "Backspace" functions.

The timing and data scan portions of this circuit are similar to those of the circuit shown in Figure 3 and will not be reviewed in detail. These portions of the circuit are enclosed in the dashed line. The major addition to the circuit which allows simple implementation of the special functions is a position counter and comparator. The position counter is an up-down counter which is preset to n-1 (n = number of characters in the display string) by "RETURN". The counter is decremented for each keystroke representing a valid display character and incremented for a "BACKSPACE" input code. A Fairchild 9324 five bit comparator compares the position counter output to the memory scan address. The memory scan begins at zero and represents the data for the right most (32nd) character in the display. The position count is indicative of the number of character keystrokes which have decremented the position counter from 31. The comparator senses two conditions of the relative values of the two counters. For memory scan equal to position count, the A=B output of the comparator will be a logical "1". For all other conditions of the two counters, A=B is a logical "0". This signal is inverted and is used to gate data from the PISO via U_1 into the HP HDSP-2000. For the condition A=B, the gating input is a logical "0" and the output of NAND gate U_2 is therefore held at a logical "1". This will cause all of the diodes associated with the character position A=B to be illuminated, thus forming the "cursor". The second condition which is sensed by the comparator is for a memory scan count less than position count, (A>B). This condition represents all character data to the right of the cursor and results in a logical "1" at the "A>B" output of the comparator. It is normally desirable for these characters to blank, hence a logical "0" should be loaded into the corresponding HP HDSP-2000 shift register locations. This is implemented by inverting the "A>B" output and applying the resulting signal to one input of NAND gate, U_1. For "A>B" at a logical "1", the output of U_1 will be a logical "1". This signal will then be inverted by U_2, causing logical "0" data to be loaded into the HP HDSP-2000 shift register for all characters to the right of the cursor. For "A=B" and "A<B", U_1 will pass inverted data from the PISO to U_2. These comparator signals are also used to control the loading of data into the proper refresh memory location. Keyboard data is initially stored in the 7475 D latches using the keyboard "STROBE" signal to trigger a one shot clock pulse from U_3. This pulse triggers a second one shot, U_4, which gates a "SET" signal to the load control flip flops, U_5 and U_6, for any valid character code. This arms the load control so that a write enable pulse will be sent to the 7489 RAM as soon as "A=B". The "$\overline{A=B}$" signal is used to prevent a second data entry from occurring during the middle of a write pulse. The write pulse also clears the load control flip-flops on the next clock cycle so that a new arriving signal can be recognized. The $\overline{Q}$ output of U_5 is also used to decrement the position counter.

The other special functions which are added to the circuit of Figure 3 are an intensity control and a blanking input. Intensity control is realized through the 74122 retriggerable monostable multivibrator, U_7. This circuit controls the time that the column select decoder is enabled during the display time, T. The display is externally blanked by holding the "RESET" input of the column select counter at a logical "0".

The circuit shown in Figure 5 is also convenient for use in instrumentation and computer readouts. In this situation, a "Busy" signal composed of $\overline{Q}$-U_2, $\overline{Q}$-U_3 and $\overline{Q}$-U_4 will allow the display interface to indicate to the driving system when data can be accepted.

Remote Display-Interface

In many systems, it is desirable to display data at multiple remote locations without having to provide the relatively complex and expensive decoding and timing scheme depicted in the previous two examples. This type of application may most often be utilized in paging system readouts, remote message displays and other systems where multiple displays would be addressed from a single central processor. The circuit shown in Figure 6 is designed to store and display a string of decoded data. The circuit requires data input from a system which can generate and serially output display and column select data — for instance, a minicomputer or microprocessor. The total number of bits of storage required (including the HP HDSP-2000 and the 5 bit column select shift register) is:

$$\text{Storage} = 35\,N + 25. \qquad (5)$$

where N = the number of characters in the display string.

The data input format should be divided into 5 equal subsets of information. Each subset should contain all of the data required to completely load the HP HDSP-2000 display string shift register (7N bits) for a given column, preceeded by a 5-bit column select code which will be shifted into the 5-bit SIPO at the HP HDSP-2000 output. The circuit has been designed to operate from two different clocks. This is important in systems where the display may be radio link addressed with the DATA ENTRY CLOCK being reconstituted from the data stream. For loading, $\overline{\text{LOAD DATA}}$ is taken low and loading can commence after $\overline{\text{READY}}$ goes low. Data is entered into the shift register through a gated input. The data string must contain the proper number of bits as defined by (5) and should be loaded in the shift register with one of the 5-bit column select codes loaded fully in the column select SIPO shift register. After loading is complete, $\overline{\text{LOAD DATA}}$ is returned high and clocking will be controlled by the DISPLAY CLOCK. The display clocking is designed to shift the stored data by 7N + 5 bits and then stop and display the shift-register contents for a period of time, T, as defined by the period of the one shot, U_1. U_1 is triggered when the clock line goes low after the synchronous counter has counted to 7N + 5. The output of U_1 resets the counter and disables the counting until the end of the period, T. The D flip-flop, U_2, insures that clock pulses to

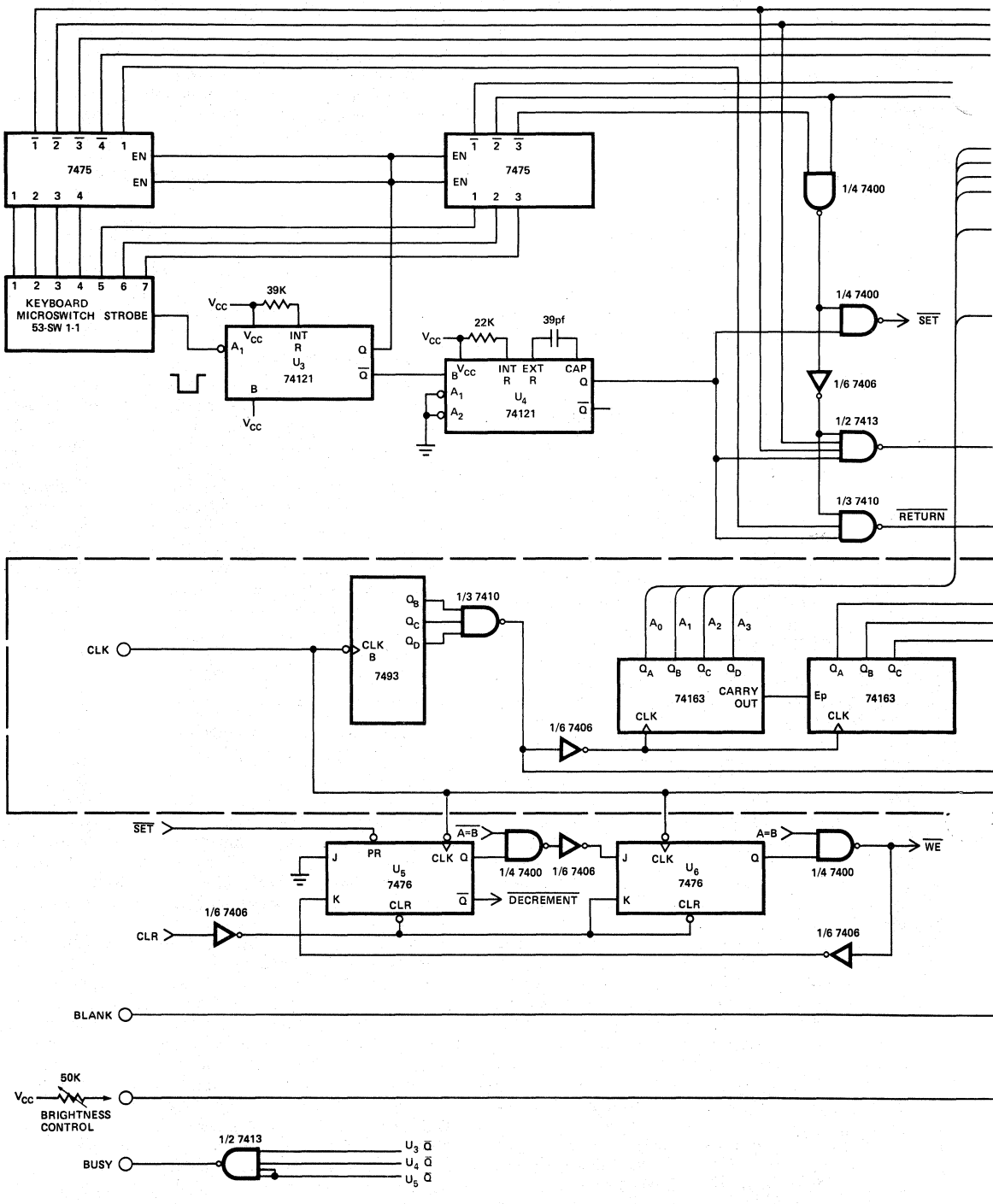
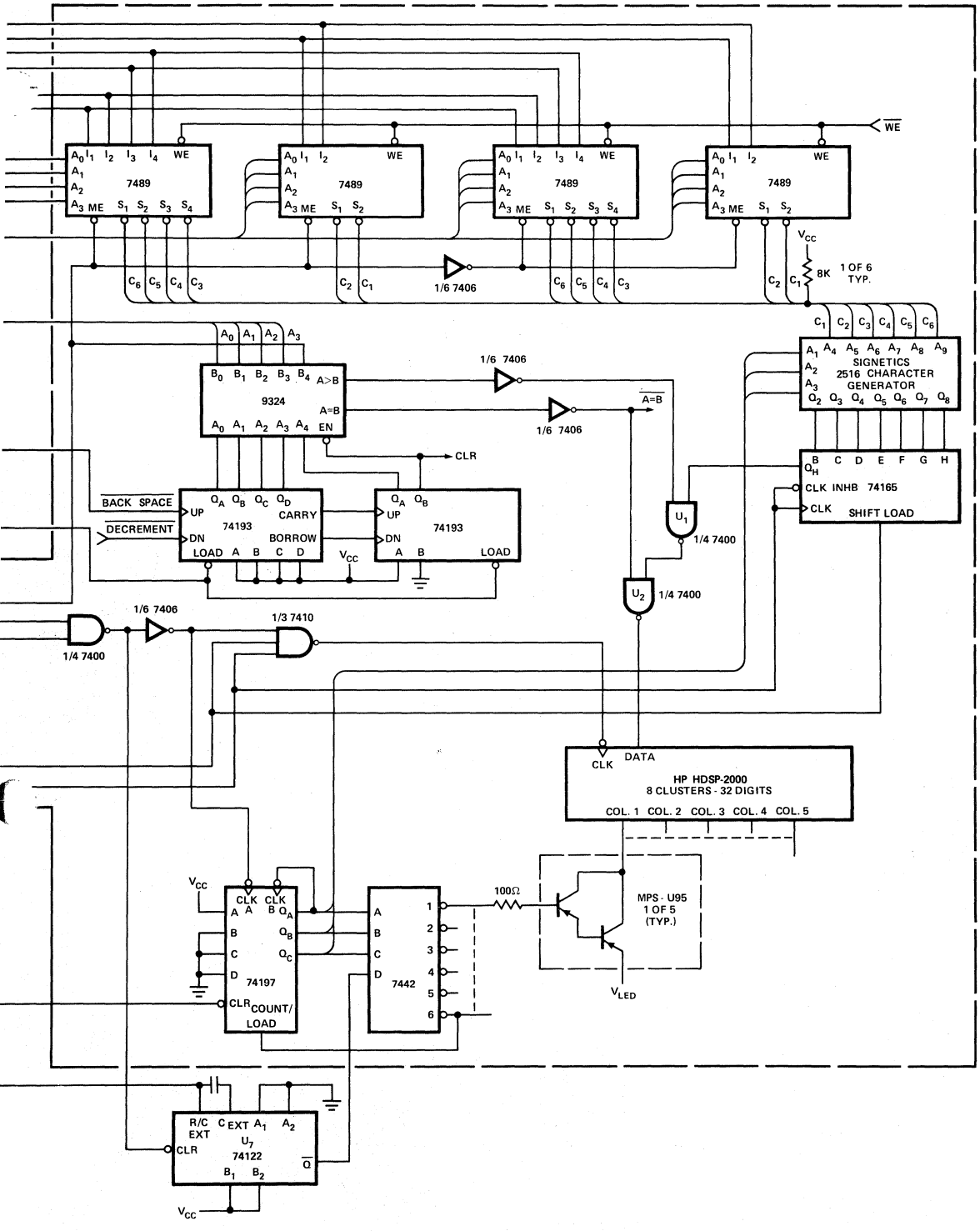


Figure 5. 32 Character Keyboard Interface Circuit.


7489
WE
1/6 7406
8K 1 OF 6 TYP.
9324
A=B
CLR
BACK SPACE
DECREMENT
74193
UP
DN
CARRY
BORROW
LOAD
1/4 7400
1/6 7406
1/3 7410
SIGNETICS
2516 CHARACTER
GENERATOR
CLK INHB 74165
SHIFT LOAD
DATA
CLK
HP HDSP-2000
8 CLUSTERS - 32 DIGITS
COL. 1 COL. 2 COL. 3 COL. 4 COL. 5
74197
COUNT/
LOAD
7442
100Ω
MPS - U95
1 OF 5
(TYP.)
74122
R/C EXT
EXT
CLR

the shift registers always start synchronous with the beginning of a full clock cycle so that erroneous clocking will not occur. U_3 is utilized to give intensity control for the HP HDSP-2000, if desired. It can be overridden by connecting the $U_{4(1-5)}$ input to the Q output of U_1 instead of U_3.

The shift register memory utilized in this circuit is only one of several forms of memory which could be chosen. Another possibility would be the use of a 512 x 1 bit or 1024 x 1 bit RAM. The counter outputs would then be used to select the RAM address.

POWER DISSIPATION/JUNCTION TEMPERATURE CALCULATIONS

The HP HDSP-2000 combines a significant amount of logic and display capability in a very small package. As such, on board power dissipation is relatively high and thermal design of the display mounting becomes an important consideration. The HP HDSP-2000 is designed to permit operation over a wide range of temperature and supply voltages. Full power operation at $T_A = 25°C$ (with $V_{CC} = V_B = V_{COL} = 5.25V$) is acceptable if the thermal resistance from pins to ambient, θ_{CA}, is no greater than 35°C/watt/cluster. This value assumes that the mounting surface of the display becomes an isothermal plane. If only one display is operated on this isothermal plane at 1.7 watts maximum, then the temperature raise above ambient is:

$$T_{RISE} = [35°C/watt] \times 1.7 \text{ watts} = 42.5°C. \quad (6)$$

If a second display is placed on this same thermal plane, with no increase in thermal dissipation capability the temperature would be doubled (i.e., 85°C) — reaching catastrophic levels very quickly. However, in most applications maximum achievable power dissipation is considerably less than the maximum allowable package dissipation of 1.7W. Calculation of power dissipation in the HP HDSP-2000 can be made using the following formula:

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) \quad (7)$$

where

$$P(I_{CC}) = I_{CC} (V_B = 0.4V) \times V_{CC} \quad (8)$$

$$P(I_{REF}) = [I_{CC} (V_B = 2.4V) - I_{CC} (V_B = 0.4V)] \times V_{CC} \times (n/35) \times 5 \times D.F. \quad (9)$$

$$P(I_{COL}) = I_{COL} \times V_{COL} \times (n/35) \times 5 \times D.F. \quad (10)$$

where

I_{CC} is measured with all S.R. stages equal to logical 1.
n = average number of diodes illuminated per character.
D.F. = Column On Time from equation (1) or the Column On Time due to pulse width modulation of V_B, whichever is lower.

As can be seen from formulas (8), (9) and (10), there are several techniques by which total power dissipation can be derated:

- Lower V_{CC} to minimum
- Lower V_{COL} to minimum
- Lower D.F.

Maximum and typical power dissipation can be calculated from the maximum and typical values of I_{CC} and I_{COL} published in the HP HDSP-2000 data sheet. While it is possible to operate the columns of the HDSP-2000 display using fullwave rectified unregulated DC, lower power dissipation can be achieved by using the regulated V_{CC} supply. Then, V_{COL} is equal to V_{CC} minus the collector to emitter saturation voltage across the column switching

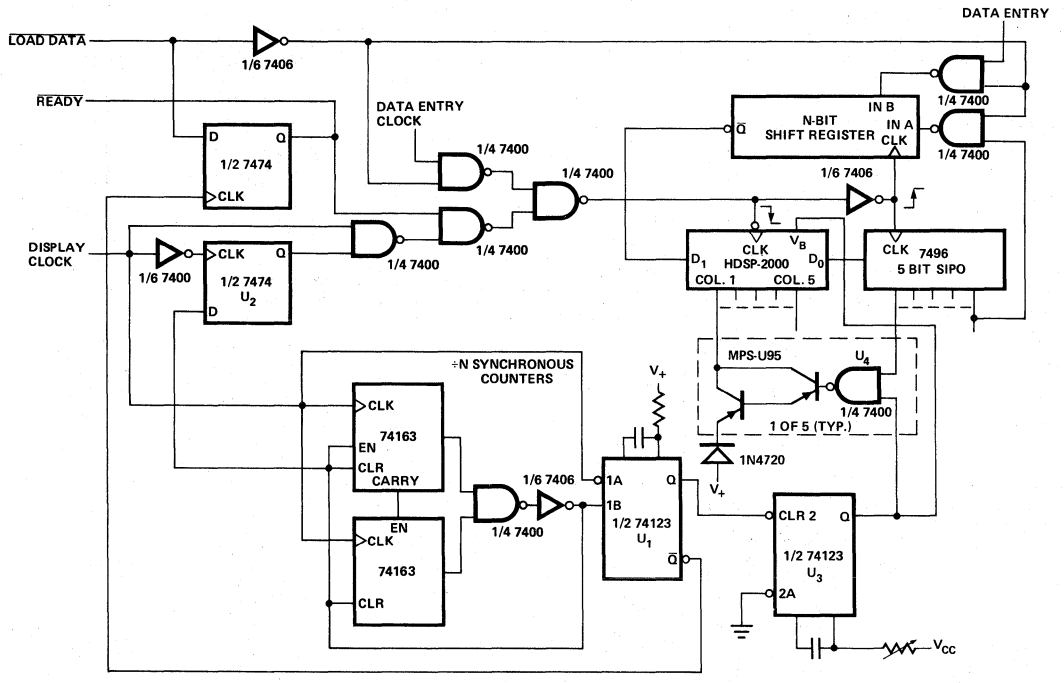


Figure 6. Display Interface Designed to Accept Decoded Data.

transistors. Since the minimum recommended V_{COL} is 2.6V, PNP Darlington transistors with a silicon diode in series with the emitter can be used to lower the power dissipation within the display. In most implementations of the ASCII character set the maximum number of diodes illuminated within a display character, n, is 21 while a typical character has 15 dots illuminated. While the maximum D.F. is 20%, in most applications D.F. $\leq$ 17.5% due to the required time to load the display. A D.F. of 17.5% represents a (7/8) ratio of display time to total time such as illustrated in the circuit shown in Figure 3. Many applications achieve a D.F. much lower than 17.5%. For example, the HDSP-2470 alphanumeric display system when configured for 40 characters has a D.F. of 11.6%.

As an example, the maximum power dissipation can be calculated for the circuit shown in Figure 3. In this circuit $V_{COL}(MAX)$ = 5.25V – 1.3V (MPS-U95 @ 1.6A) – .85V (1N4720 @ 1.6A) = 3.10V. Thus maximum achievable power dissipation can be calculated as shown below:

$$P(I_{CC}) = 60mA \times 5.25V = 315\ mW \quad (11)$$

$$P(I_{REF}) = (95mA - 60mA) \times 5.25V \times (21/35) \times 5 \times 0.175 = 96.5\ mW \quad (12)$$

$$P(I_{COL}) = 410mA \times 3.1V \times (21/35) \times 5 \times 0.175 = 667\ mW \quad (13)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 1079\ mW \quad (14)$$

Similarly, typical power dissipation can be calculated as:

$$P(I_{CC}) = 45mA \times 5.00V = 225\ mW \quad (15)$$

$$P(I_{REF}) = (73mA - 45mA) \times 5.00V \times (15/35) \times 5 \times 0.175 = 52.5\ mW \quad (16)$$

$$P(I_{COL}) = 335mA \times (5.00V - 1.3V - .85V) \times (15/35) \times 5 \times 0.175 = 358\ mW \quad (17)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 636\ mW \quad (18)$$

For operation at the maximum temperature of 70°C, it is important that the following criteria be met:

a. $T_{CASE} \leq 100°C$, where T_{CASE} = hottest pin temperature

b. $T_{IC\ JUNCTION} \leq 125°C$

Thermal resistance from junction to case, θ_{JC}, is typically 25°C/watt. Using these factors, it is possible to determine the required heat sink power dissipation capability and associated power derating through the following assumptions:

$$T_{IC\ JUNCTION} = (\theta_{CA} \times P_D) + \theta_{JC}\left(\frac{P_D - .015n}{2}\right) \quad (19)$$

$$T_{CASE} = (\theta_{CA})\ P_D \quad (20)$$

where $\left(\frac{P_D - .015n}{2}\right)$ is the power dissipated in each IC.

HEAT SINKING CONSIDERATIONS

In practice, heat sink design for the HP HDSP-2000 involves optimization of techniques to dissipate heat through the device leads. Figures 7 and 8 schematically depict two possible heat sink designs. In many applications, a maximum metalized printed circuit board such as shown in Figure 7 can provide adequate heat sinking for the HDSP-2000 display. For example, the HDSP-2416/-2424/-2432/-2440 display boards consist of

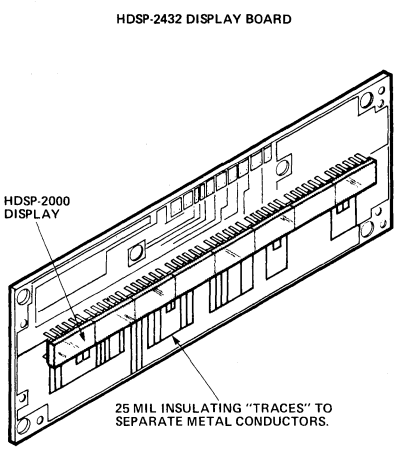


Figure 7. Maximum Metalized Printed Circuit for the HP HDSP-2000.

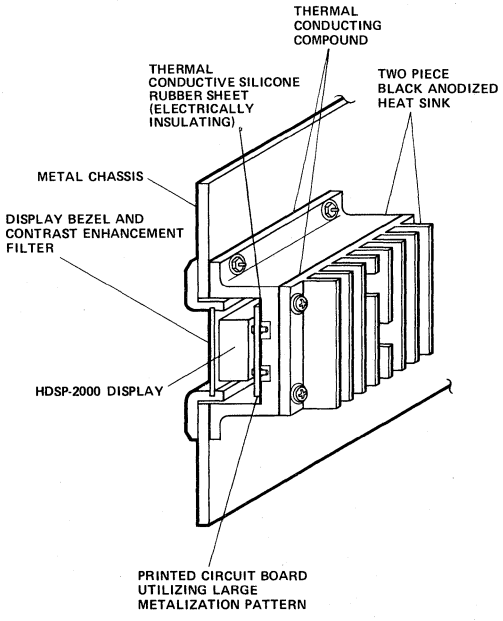


Figure 8. Two-Part Heat Sink for the HP HDSP-2000.

a 16, 24, 32 or 40 character HDSP-2000 display mounted on a maximum metalized printed circuit board. These display boards are designed for free air operation to 55°C and operation to 70°C with forced air cooling of 150 fpm normal to the component side of the board. A free air operating temperature of 70°C can be achieved by heat sinking the display. Figure 8 depicts a two part heat sink which can be assembled using two different extruded

parts. In this design, the vertical fins promote heat transfer due to naturally induced convection. Care should be taken to insure a good thermal path between the two portions of the heat sink. To optimize power handling capability, the metal heat transfer contact area between the PCB metalization and the heat sink should be maximized. A surface area of approximately 8 square inches per cluster will permit operation at 1.1 watts/cluster at the maximum operating temperature of 70°C ambient. The value of 1.1 watts/cluster is easily achieved by reduction of V_{COL} to 3 volts. Next to increasing total heat sink area, a provision for at least some forced air flow is probably the most effective means of improving heat transfer. Thermal design for the HP HDSP-2000 must be carefully considered as operation at excess temperatures can lead to premature failure.

The HP HDSP-2000 displays may also be mounted in standard DIP sockets which are cut down to accept the 6 pin devices in end-to-end strings. Another alternative for socket mounting is the stripline socket such as the Augat 325-AG1D or AMP 583773. These sockets will allow enough space bewteen the PCB and the HP HDSP-2000 to permit a heat sink bar to be inserted to conduct heat to an external sink. Most sockets add a thermal resistance of about 2°C/watt bewteen the device leads and the PCB.

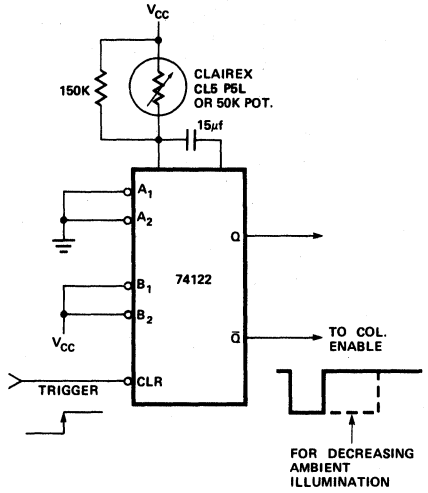


Figure 9. Intensity Modulation Control Using a One Shot Multivibrator.

DISPLAY INTENSITY MATCHING AND CONTROL

The luminous intensity of LED displays in general has a fairly wide dynamic range. If there is too great a difference between the luminous intensity of adjacent characters in the display string, the display will appear objectionable to the viewer. To solve the problem, the HP HDSP-2000 displays are categorized for luminous intensity. The category of each display package is indicated by a letter preceding the date code on the package. When assembling display strings, all packages in the string should have the same intensity category. This will insure satisfactory intensity matching of the characters. The HP HDSP-2000 displays are categorized in 8 overlapping intensity categories. All characters of all packages designated to be within a given letter category will fall within an intensity ratio of less than 2:1. For dot matrix displays, a character-to-character intensity ratio of 2:1 is not generally discernable to the human eye.

A more important consideration regarding display intensity is the control of the intensity with respect to the ambient lighting level. In dim ambients, a very bright display will produce very rapid viewer fatigue. Conversely, in bright ambient situations, a dim display will be difficult, if not impossible, to read and will also produce viewer fatigue and high error rates. For this reason, control of display intensity with respect to the environment ambient intensity is an important consideration. Figure 9 depicts a scheme which will automatically control display intensity as a function of ambient intensity. This circuit utilizes a resettable one shot multivibrator which is triggered by the column enable pulse. The duration of the multivibrator output is controlled by a photoconductor. At the end of a column enable pulse, the multivibrator is reset to insure that column current is off prior to the initiation of a new display shift register loading sequence. The output of this circuit is used to modulate either the V_B inputs of the HP HDSP-2000 displays or the column enable input circuitry. For maximum reduction in display power, both inputs should be modulated.

In the circuit shown in Figure 9, the photocell may be replaced by a 50K potentiometer to allow manual control of display intensity.

Contrast Enhancement

Another important consideration for optimum display appearance and readablity is the contrast between the display "ON" elements and the background. High contrast can be achieved by merely driving the highest possible power into the display. This, of course, is feasible in some situations as long as ambient lighting is not too intense and power dissipation is not a consideration. A much more practical technique is the use of an effective contrast enhancement filter material. The following materials, Panelgraphic Ruby Red 60 and Dark Red 63 or SGL Homalite H100-1605 and H100-1670 will all provide improved contrast for the HP HDSP-2000 display. Other good practices to enhance display contrast are to avoid PCB traces in the visible areas around the display and, if possible, the utilization of a black silk screen over the relatively light PCB areas around the display. The subject of contrast enhancement is treated in greater detail in HP Application Note 964. Microprocessor interfaces to the HDSP-2000 display are shown in HP Application Note 1001.

KEY POINTS REGARDING THE HP HDSP-2000:

- A logical "1" in the display shift register turns a corresponding LED "ON".
- Clocking occurs on the high to low transition of the clock input.
- A character generator which produces 7 bit "COLUMN" data should be utilized.
- The internal shift register is 28 bits in length.
- Each column should be refreshed at a minimum rate of 100 Hz.

The following is a list of commercially available character generators which can be used in conjunction with the HP HDSP-2000. These devices are all programmed to convert from ASCII input code to 5 sets of 7 bits each for a 5 x 7 display format. Any desired input-output coding can be utilized in custom programmed ROMs.

Manufacturer	Part Number	Typical Access Time	Required Power Supplies	Typical Power Dissipation
Texas Instruments	TMS 4100	500 nsec	±12V	450 mW
National	5241 ABL	700 nsec	±12V	
Signetics	2513	450 nsec	±5V −12V	290 mW
	2516	500 nsec	±5V −12V	280 mW
AMI	S8773B	450 nsec	+5V −12V	625 mW (max)
Mostek	2002 2302		±14V +5V −12V	320 mW 200 mW
Electronic Arrays	40105	750 nsec	±12V	430 mW
Fairchild	3257	500 nsec	+5V −12V	360 mW

Figure 10. Column Output Character Generators Suitable for Use with the HP HDSP-2000.

The refresh memory for the HP HDSP-2000 display can take any one of several different forms. The following table lists a few of the devices which the display system designer may find convenient.

Type	Organization
Bipolar RAM	Words x Bits
*7489	16 x 4
*7481A	16 x 1
*7484A	16 x 1
Fairchild 93403	16 x 4
Intel 3101	16 x 4
Intel 3104	4 x 4
MOS RAM	
TI TMS 4000 JC/NC	16 x 8
CMOS RAM	
RCA CD 4036	4 x 8
RCA CD 4039	4 x 8
National 74C89	16 x 4
Motorola MCM 4064	16 x 4
Shift Register	
TI TMS 3112	32 x 6
Signetics 2518	32 x 6
Signetics 2519	40 x 6
Fairchild 3348	32 x 6
Fairchild 3349	32 x 6

*Standard 7400 Series TTL logic parts available from most Integrated Circuits manufacturers.

Figure 11. Memory Elements Which can be Utilized in HDSP-2000 Display Systems.