

Design of a 4.9 to 6.0 GHz Two-stage Low Noise Amplifier For 802.11a, HiperLAN2 and HiSWANa Receivers Using ATF-551M4 E-PHEMT

Application Note 5091

This application note examines the design of a compact (6 mm by 15 mm) two-stage, low noise, unconditionally stable, amplifier for 802.11a, HiperLAN2 and HiSWANa receiver applications. At 5.5 GHz and biased at 3.3V and 30mA, the amplifier provides 22.2 dB gain, 1.4 dB noise figure, linear output power (P_{1dB}) of +11.5 dBm, and a third-order output intercept point (OIP_3) of +28 dBm. Its frequency coverage includes the portions of the 5 GHz spectrum currently specified for wireless local-area networking in North America, Europe and Japan:

North American 802.11a:
5.15-5.35 GHz and 5.725-5.825 GHz (U-NII bands)

European HiperLAN2:
5.15 - 5.35 and 5.470 - 5.725 GHz,

Japanese HiSWANa:
5.15-5.25 GHz

The amplifier is designed around the Agilent ATF-551M4 low noise enhancement mode pseudomorphic HEMT (E-PHEMT) in both stages. The

device is supplied in a leadless surface-mount plastic package with dimensions of 1.4 mm x 1.2 mm x 0.7 mm, and its 400- μ m gate width combines low noise figure coincident with high intercept point over the 2 to 10 GHz frequency range.

Besides having a very low typical noise figure (0.5 dB), the ATF-551M4 is specified at 2 GHz and 2.7-volt bias to provide a +24.1 dBm third-order output intercept point (OIP_3) at 10 mA drain current.

The advantage of an enhancement mode PHEMT versus a depletion mode PHEMT is that biasing the device is simplified by the fact that the enhancement mode PHEMT requires a positive voltage on the gate for normal biasing as opposed to a negative voltage for a depletion mode PHEMT. Biasing the ATF-551M4 only requires a voltage divider from the drain to supply a small positive voltage to the gate for nominal drain current.

A data sheet for the ATF-551M4 may be downloaded from: (<http://cp.literature.agilent.com/litweb/pdf/5988-9006EN.pdf>)

Low noise E-pHEMT amplifier design

To meet the goals for noise figure and gain, the drain source current (I_{ds}) of each stage was chosen to be 15 mA. According to the data sheet this value provides good IP_3 combined with a very low minimum noise figure (F_{min}). The data sheet also indicates that a 2.7 V drain-to-source voltage (V_{ds}) gives slightly higher gain and easily allows the use of a regulated 3.3 V supply.



Using Agilent Technologies *EEsof Advanced Design System* software (ADS) the amplifier circuit can be simulated in both linear and non-linear modes of operation. For the linear analysis the transistors can be modeled with a two-port s-parameter file using *Touchstone* format. File *ATF551M4.s2p* can be downloaded from the *Agilent Wireless Design Center* web site (<http://www.agilent.com/view/rf>). In addition to information regarding gain, noise figure, and input and output return loss, the simulation also provides important insight into circuit stability. Calculating the Rollett stability factor (K) and generating stability circles are both made considerably easier with computer simulation.

The ADS nominal optimization (also known as performance optimization) tool was used to aid the amplifier design. This tool can be used to modify a set of parameter values to satisfy predetermined performance goals by comparing computed and desired responses and modifying design parameter values to bring the computed

response closer to target performance. Nominal optimization is available in the ADS simulator for analog/RF systems simulation using any analysis type, such as AC, DC, S-parameter, harmonic balance, circuit envelope, and transient simulation. Goals were set for gain, noise figure and return loss over the 4.9 - 6.0 GHz bandwidth, out-of-band gain, as well as for unconditional stability from 0.1 - 18 GHz. An example of nominal optimization, *optex1_prj*, is available in Chapter 2 of the ADS help library under *tuning, optimization and statistical design*.

For the optimization tool to work at 6 GHz, accurate equivalent circuit models for the resistors, inductors and capacitors are required. The models must include package parasitic inductance, resistance and capacitance, which allows the component value to be varied over a small range using the optimization tool and accurately correlate to measured data. Examples of passive component models and ADS optimization tool terminology are shown in Fig.

1. It should be noted that each manufacturer's passive elements exhibit slightly different parasitic properties.

The demonstration board shown in Fig. 2 was developed primarily for 5 to 6 GHz applications. The demonstration board is a two layer configuration for rigidity. The printed circuit board material is FR-4 with a typical dielectric constant of 4.2 and a total board thickness of 0.052 inches. The signal layer is the top layer which is 0.010 inch thick while the bottom layer is 0.042 inch thick. The RF input and output connectors, J1 and J2, are normally designed for 0.062 inch thick printed circuit boards. The center pin is trimmed to about 0.040 inches in length and then the connectors are installed such that the center pin lays down directly on the printed circuit board with no gap between the printed circuit board and center pin. Be sure to solder both the top and bottom ground pins of the connectors to the printed circuit board.

The board utilizes small EIA 0402 (.04 x .02 in/ 1.0 x 1.5 mm, nominal) form-factor

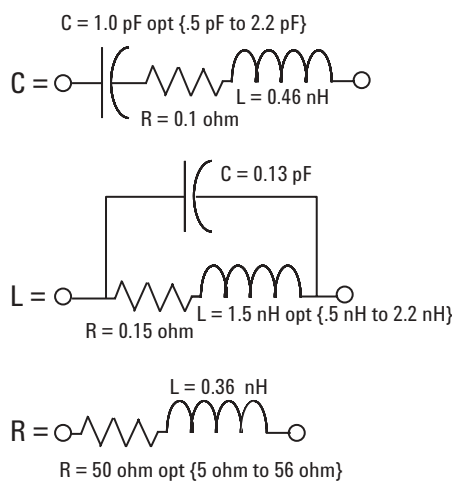


Figure 1. Passive component models and ADS optimization tool terminology

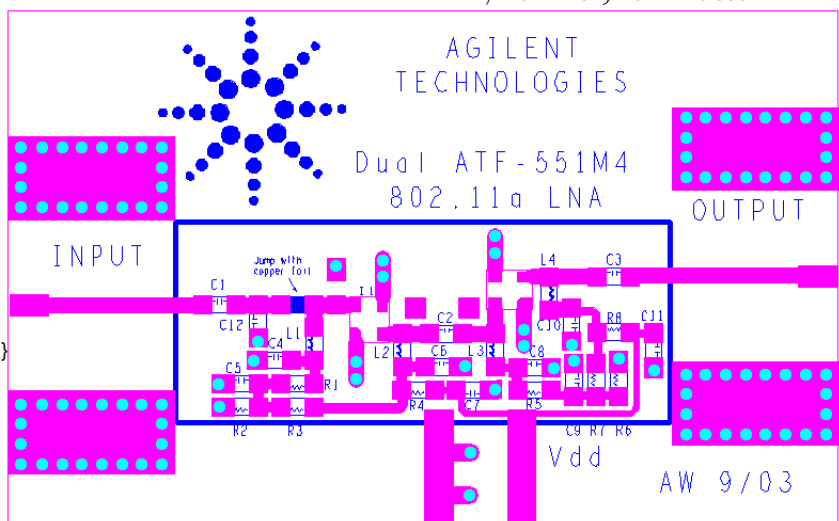


Figure 2. Demonstration Board Artwork and Component Placement

surface mount components. The use of microstrip lines in place of the 0402 inductors would reduce circuit losses but would produce a larger layout. The actual 6 mm by 15 mm area required for the circuitry is outlined in blue.

The schematic diagram of the two-stage amplifier is shown in Fig. 3. The amplifier uses a bandpass network for input matching and a high-pass network for output matching. Interstage matching is provided by a high pass network. The parts list is shown in Table I.

The input network represents a compromise between best noise figure and reasonable input return loss and consists of series capacitor C1, shunt inductor L1 and shunt capacitor C12. Note that when using the demonstration board layout shown, the mounting pads before L1 will have to be bridged with copper foil. The mounting pads are included to allow for a low-pass impedance matching network topology if desired for individual application requirements.

The output high-pass network consists of a series capacitor C3 and a shunt inductor L4. The bandpass and high-pass networks provide additional low

Table 1. Component parts list for 2 stage ATF-551M4 amplifier

C1, C4	2.2 pF Johnson 251R07C2R2BV4E
C2	0.8 pF Johnson 251R07C0R8BV4E
C3	3.9 pF Johnson 251R07C3R9BV4E
C5, C7, C9, C11	10 nF Kemet C0402C103K3RACTU
C6	1.0 pF Johnson 251R07C1R0BV4E
C8, C10	1.5 pF Johnson 251R07C1R5BV4E
C12	0.5 pF Johnson 251R07C0R5BV4E
L1, L2, L3, L4	1.5 nH Johnson L-07C1N5S
J1, J2	E.F. Johnson SMA connector 142-0701-801
R1, R5	49.9 Ω Yageo 9C04021A49R9FLHF3
R2, R6	5.1K Ω Yageo 9C04021A5101JLHF3
R3, R7	22K Ω Panasonic ERJ-2RKF222X
R4, R8	39 Ω Yageo 9C04021A39R0FLHF3
Q1, Q2	Agilent ATF-551M4

frequency gain roll-off which serves several purposes. First, enhanced rejection of lower frequency signals may decrease the susceptibility of the LNA to stronger low frequency emitters, which could drive the LNA to compression and adversely affect the in-band performance. Second, the roll-off of the low frequency gain also improves the stability of the LNA, since a low frequency gain peak is generally associated with a decreased value of K.

Since L1 is also used for the insertion of gate voltage, the inductance must be adequately bypassed at the normal operating frequency by C4.

Resistor R1 and C5 provide a good low frequency resistive termination, which enhances low frequency stability. If the value of C4 is made too large, the series-resonant frequency of L1 and C4 can often produce a low frequency gain resonance, which may prove difficult to stabilize with R1 and C5. With the help of the optimization function in ADS, values for L1, C4, and R1 can be selected for best low frequency stability. C5 is 10 nF to improve the output third-order intercept and is kept constant during the optimization process. In a similar fashion, L4 is used to apply drain voltage to Q2 and is therefore bypassed with C10. R8 and C11 provide a low frequency resistive termination.

Since the primary goal of the input network is to provide a low noise figure coincident with good S_{11} and the primary goal of the output network is to provide the desired power output with good S_{22} , the interstage network can be called upon to help flatten gain over the desired bandwidth, to decrease gain at lower frequencies and to help with overall stability. With inductors required to apply drain voltage

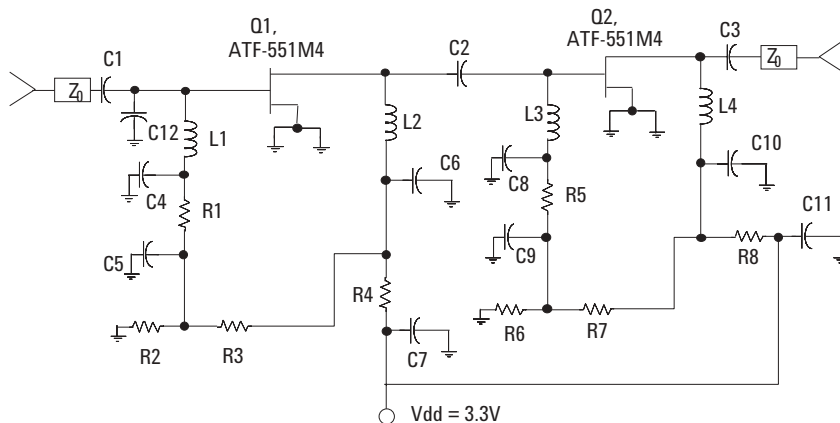


Figure 3. Schematic Circuit Using Passive Bias

to Q1 and gate voltage to Q2, and a capacitor required for DC isolation between the two stages, we have the basis for a high pass network. ADS is used to optimize this network for the various parameters. In a similar fashion, R4/C7 and R5/C9 provide low frequency bias decoupling and enhance low frequency stability.

Source Grounding

The importance of properly grounding the source terminals of the FETs cannot be overemphasized. Quite often, the designer feels that the only proper way to ground the sources is with the shortest distance possible between the device and the signal ground plane. Although the shortest length will generally provide the highest gain, some controlled amount of source inductance can be used to increase stability, improve S11 and S22 with minimal effect on noise figure and only a slight reduction in gain. In some cases where the distance between the source terminals and the ground plane is excessive, the amplifier will have uncontrollable oscillations that are most likely up in the 8 GHz and higher frequency range.

This amplifier design makes use of a small amount of source inductance in the form of a short length of microstrip between each source terminal and the plated through hole that connects the top layer etch to the signal ground plane. With any multi-layer circuit board, it is very important that the plated through holes for any top layer circuitry make contact with the ground plane directly beneath the signal layer. The plated through holes can continue on to the lower layers

but must not skip over the very important signal ground plane. Unnecessarily long grounds can cause undesired feedback and result in amplifier instabilities and oscillations.

Accurately modeling the microstrip line dimensions between each source terminal and the plated through hole and the plated through hole dimensions between the microstrip and the signal ground plane will allow the designer to use ADS to determine the optimum amount of source inductance for a given design. Since source inductance generally makes the FETs regenerative at higher frequencies and degenerative at lower frequencies, a plot of K from 100 MHz to 18 GHz will reveal an optimum amount to be used in the circuit.

Biasing

Once the RF matching has been established, the next step is to DC bias the device. A passive biasing example is shown in Fig. 3. In this example the voltage drop across resistor R4 and R8 sets the drain current (I_d), with their values calculated using the following equation:

$$R4 = R8 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{bb}} \quad (1)$$

where:

V_{dd} is the power supply voltage, 3.3 V;

V_{ds} is the device drain to source voltage, 2.7 V;

V_g is the device gate to source voltage, 0.515 V;

I_{ds} is the device drain to source current, 15 mA;

I_{bb} for DC stability is 10 times the typical gate current, 0.1 mA.

Voltage divider networks R2/R3 and R6/R7 establish the typical gate bias voltage (V_g).

$$R2 = R6 = \frac{V_g}{I_{bb}} \quad (2)$$

$$R3 = R7 = \frac{(V_{ds} - V_g) \times R2}{V_g} \quad (3)$$

The complete passive bias example may be found on page 20 of the product data sheet (<http://literature.agilent.com/litweb/pdf/5988-9006EN.pdf>). Note that there are differences between calculated values and the actual values due to the use of preferred component values as shown in Table 1.

As with any depletion or enhancement mode PHEMT, the dc parameter variation from device to device can cause the quiescent drain current to either increase or decrease from the nominal design value. Active biasing provides a means of keeping the quiescent bias point constant as dc parameters may vary from lot to lot. Active biasing also provides bias stability over temperature and is the recommended method of biasing any PHEMT device in high volume applications.

Results

The amplifier is tested at a power supply voltage V_{dd} of 3.3 V, which provides each device with a bias point of $V_{ds} = 2.7 \text{ V} @ I_d = 15 \text{ mA}$. The measured performance is compared to the simulated performance which is obtained from the device data sheet S and noise parameters. The measured and simulated noise figure is shown in Fig. 4. Noise figure is a nominal 1.4 dB at 5.8 GHz. The loss of the input microstripline has been measured at 0.15 dB, making the noise figure of the device plus the loss of the matching network around 1.25 dB. The output power at 1 dB gain compression, P_{-1dB} , was measured as +11.5 dBm. The output third-order intercept point, OIP_3 , was measured at +28 dBm.

The measured and simulated gain of the amplifier is a nominal 22 dB at 5.8 GHz. The swept gain plot shown in Fig. 5 shows moderate gain roll-off at lower frequencies. Measured and simulated input and output return loss is shown in Figure 6 and 7, respectively. The measured input return loss is greater than 10 dB over the 4.9 to 6 GHz frequency range while the output return loss measured greater than 9.5 dB over the same frequency range.

Table 2 provides a summary of the performance of the amplifier over the expected battery operating conditions. It was noted that at 3.6V, a fully charged battery, the noise figure performance was unaffected. The table also shows that as the battery voltage drops below 3V, only a small degradation in performance is observed.

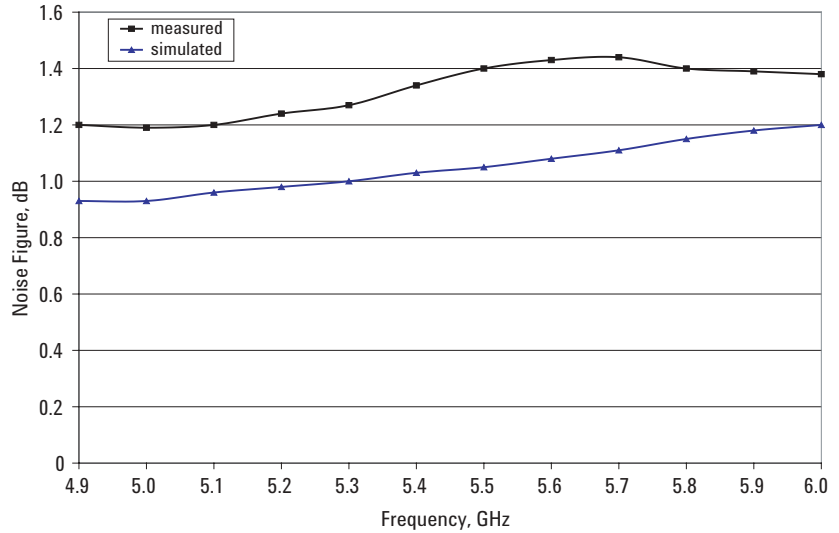


Figure 4. Measured and Simulated Noise Figure vs. Frequency

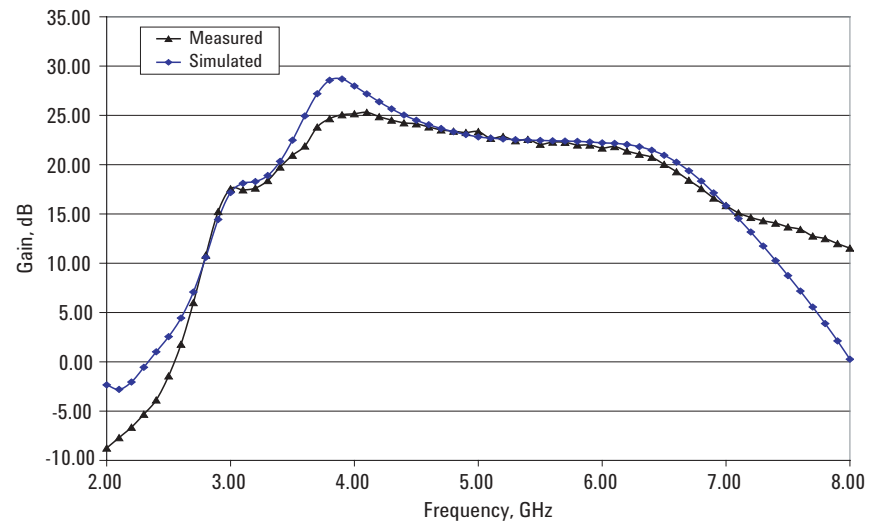


Figure 5. Measured and Simulated Gain vs. Frequency

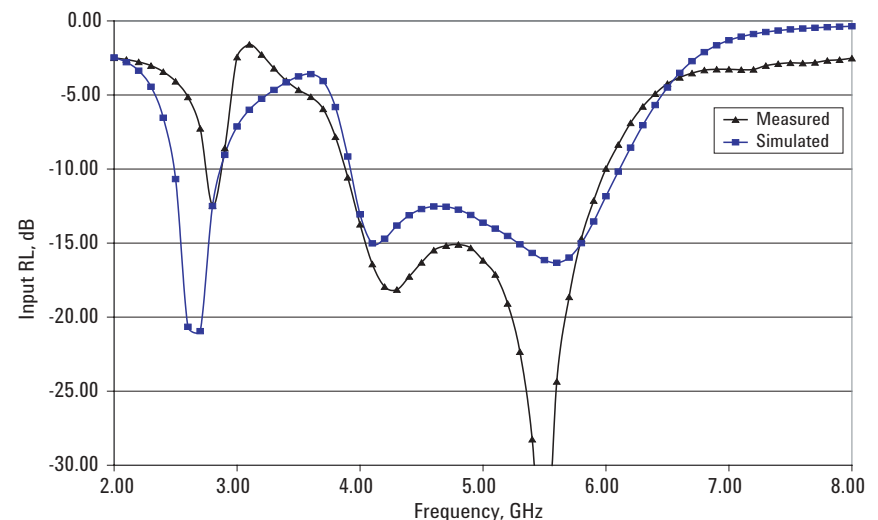


Figure 6. Measured and Simulated Input Return Loss vs. Frequency

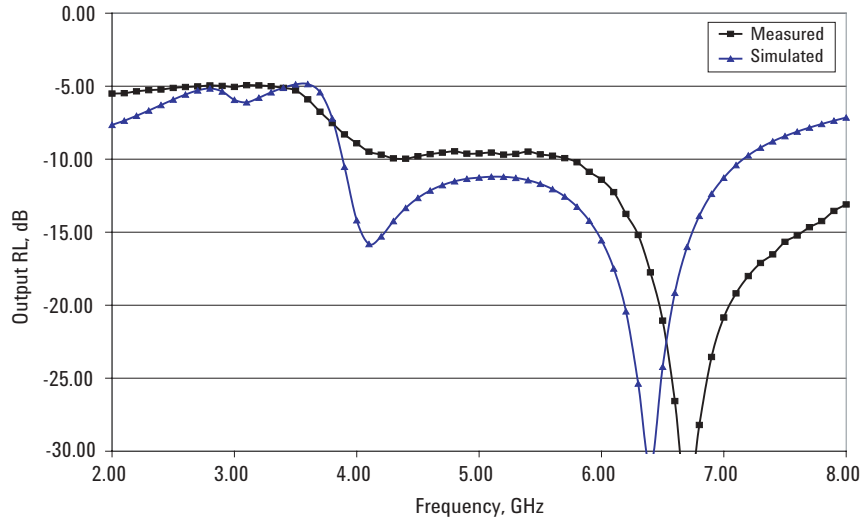


Figure 7. Measured and Simulated Output Return Loss vs. Frequency

Table 2. Summary of measured performance vs. supply voltage

	Supply, Vdd and Idd		
	3.3V, 30mA	3.0V, 23.3mA	2.7V, 15mA
Frequency, GHz	4.90		
Gain, dB	23.30	22.60	21.30
NF, dB	1.20	1.25	1.35
Frequency, GHz	5.50		
Gain, dB	22.32	21.90	21.00
NF, dB	1.30	1.37	1.45
Frequency, GHz	6.00		
Gain, dB	22.00	21.50	20.80
NF, dB	1.35	1.40	1.43

ADS Simulation Schematic

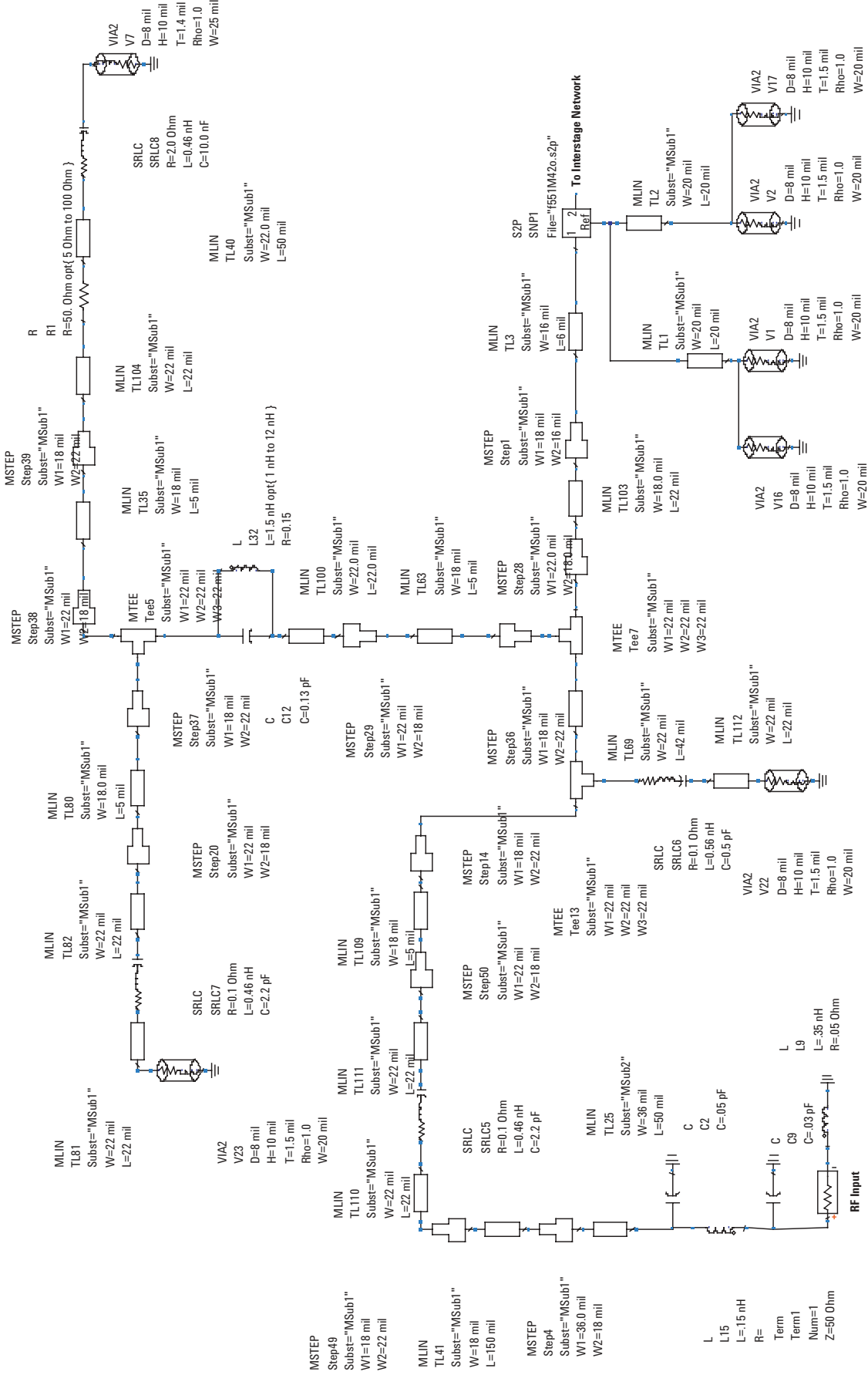


Figure 8. Input matching network. The empirically derived model for the EF Johnson end-launch SMA connector (p.n. 142-0701-801) is also shown.

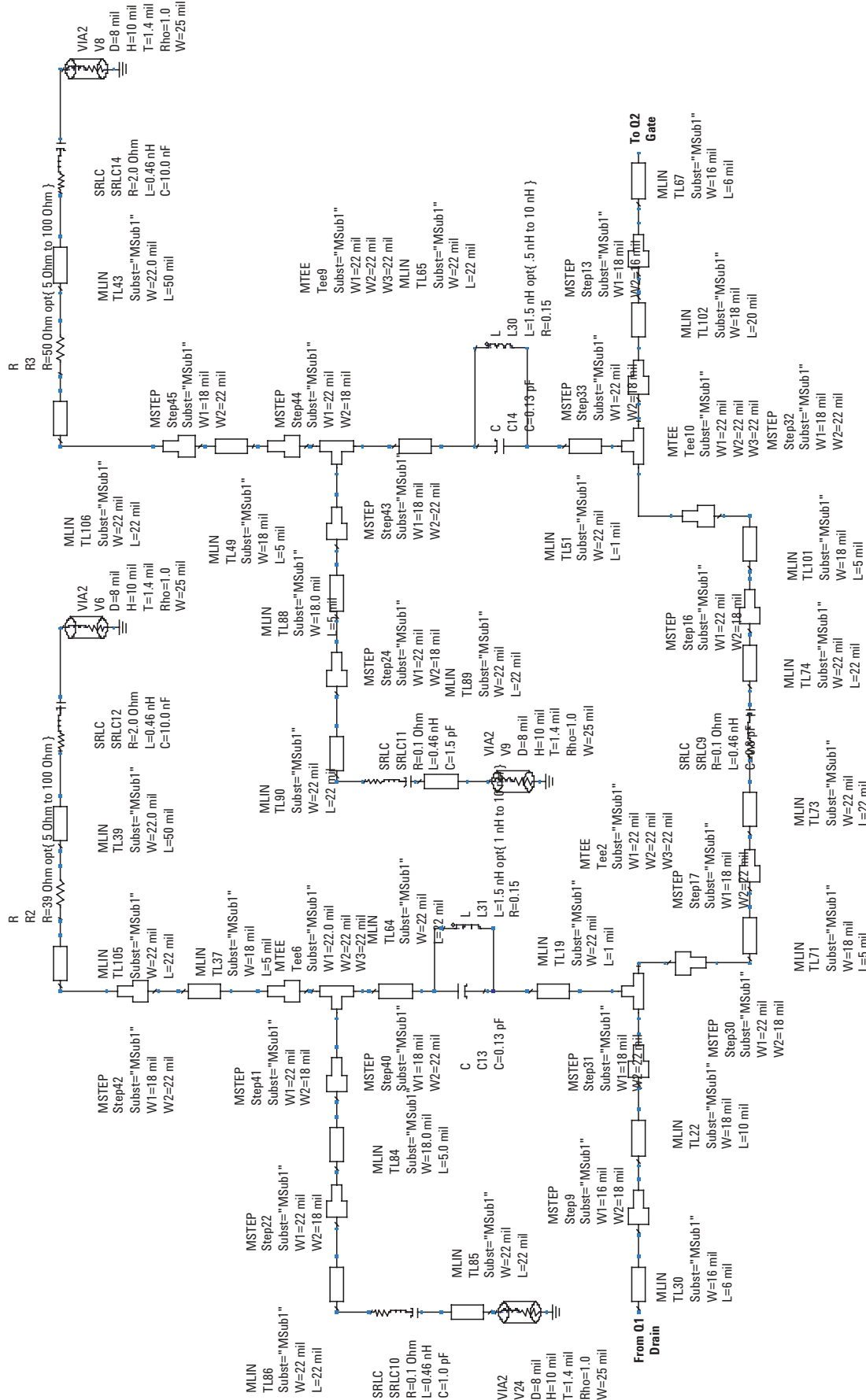


Figure 9. Interstage matching network

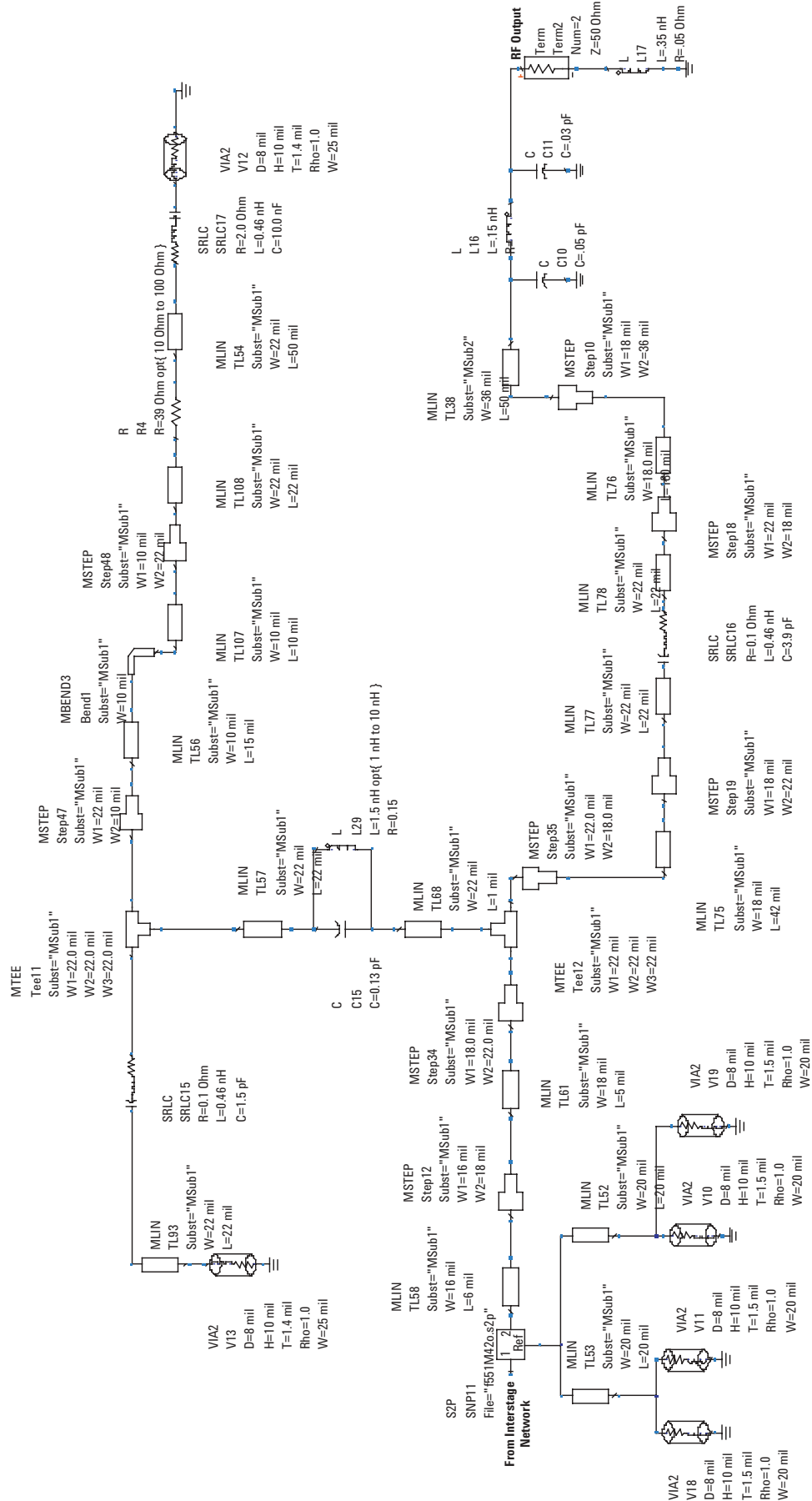


Figure 10. Output matching network. The empirically derived model for the EF Johnson end-launch SMA connector (p.n. 142-0701-801) is also shown.














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Figure 11. Optimization simulation tool with target goals from schematic window

References:

[1] Ward, A. *Agilent ATF-54143 Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package*, 2001 [Internet]. Available from: <http://literature.agilent.com/litweb/pdf/5988-9006EN.pdf>.

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