Precision Measurement of Metal Line Width in Sub-quarter Micron Interconnect Systems

Application Note 4156-11

Agilent 4155C and 4156C Semiconductor Parameter Analyzers

Introduction

The interconnect system in advanced integrated circuits that employ sub-quarter micron technologies plays a critical role in determining IC performance.

IC speed is determined mainly by transistor gate delay and the propagation delay of the interconnect system, both of which are caused by the capacitance and resistance time constant (RC) shown in Figure 1. Although transistor gate delay time is becoming increasingly short, the propagation delay of modern metal systems is becoming longer with each introduction of a new generation process. Figure 2 shows that the interconnect propagation delay exceeds the gate delay when the technology falls below 0.25 μm. This trend is a major factor in determining the speed of modern, high-speed ICs.

Narrower metal lines tend to show greater variation in overall width than the wider lines. Therefore, narrower signal lines that connect transistors have more effect on the speed variation of a high speed ICs. For this reason, it is most important to control line width in a modern interconnect system.

Measuring the width of narrow

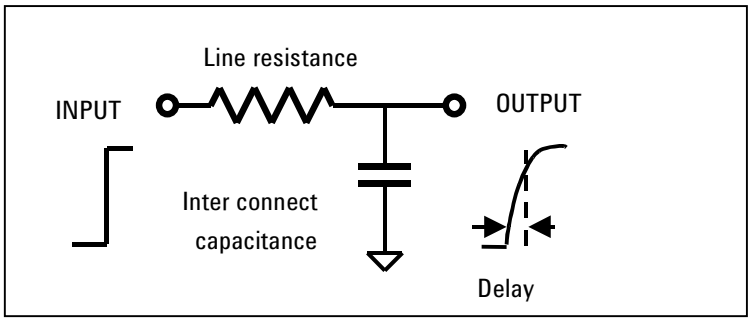

Figure 1. RC propagation delay of the interconnect system.

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lines accurately and efficiently is a current industry concern. In a sub-quarter micron regime, accurate narrow line width measurement is more difficult using traditional optical methods because the length of the light wave becomes equivalent to the minimum line width. This method, therefore, cannot provide sufficient resolution. Although a SEM has the ability to provide the required resolution, it is not a practical tool for everyday use.

An electrical approach to measuring line width is a more realistic solution, but it must be used with a care in sub-quarter micron environment.
This application note address the methods of accurately measuring narrow lines using the Agilent 4155C and 4156C semiconductor parameter analyzers.

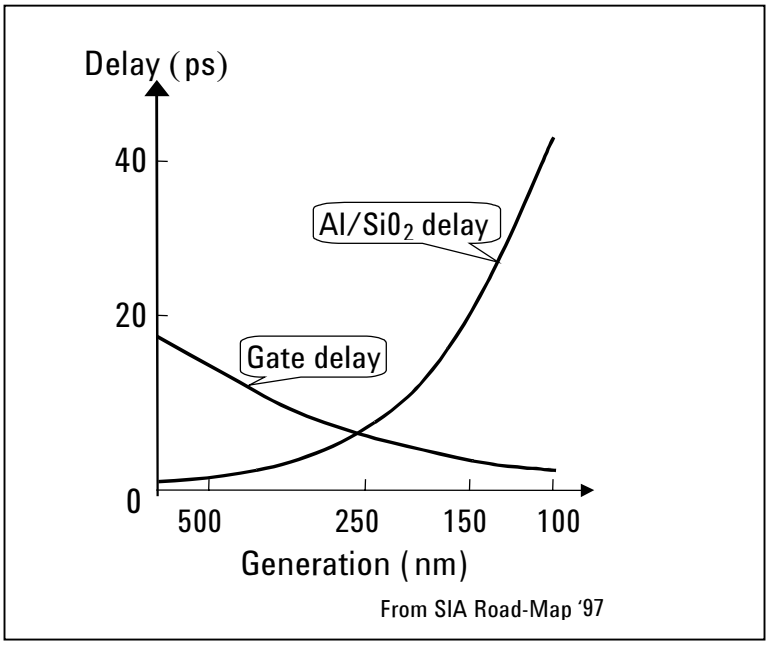

Figure 2. Propagation delay of the transistor gate and interconnect system.

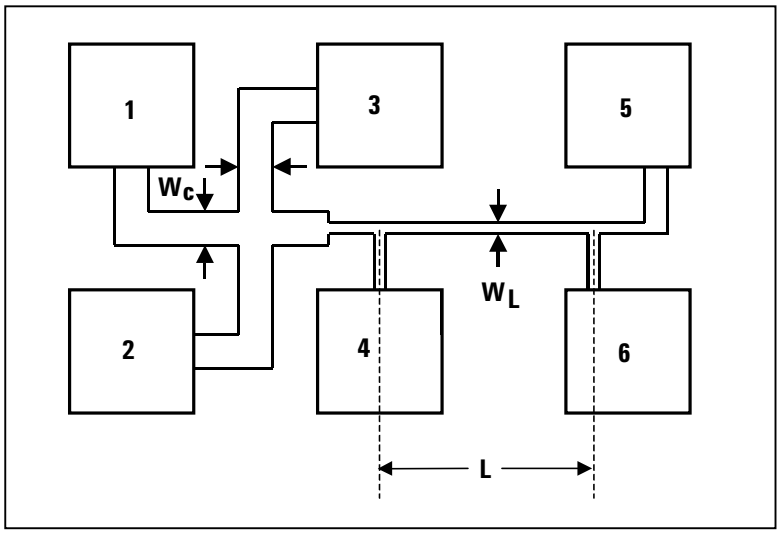

Figure 3. Example of Van der Pauw, Greek cross bridge, and straight line linear bridge combined test structure.

Measuring line width using the electrical method

Measuring line width by an electrical method requires measuring sheet resistance using Van der Pauw bridge and linear bridge test structures. The typical combined test structures for a Van der Pauw bridge configured as a Greek cross and for a linear bridge are shown in Figure 3. The theory of the sheet resistance and the line width measurement using this type of test structures is discussed in the following section.

Sheet resistance measurement

Sheet resistance is measured using the Greek cross shown in Figure 3, which is connected to pads 1, 2, 3, and 4. The current is forced between pads 1 and 2, and the voltage is measured between pads 3 and 4. Sheet resistance, Rs, is calculated as shown in Equation 1 below:

$$Rs = \frac{\pi}{\ln 2} \times \frac{V_{34}}{I_{12}} \qquad (1)$$

where :

Rs= Sheet resistance measured using a Greek cross bridge (ohm/square)
V_{34}= Voltage measured between pads 3 and 4
I_{12}= Current forced between pads 1 and 2

Sheet resistance is the resistance of a square of conductive thin film with uniform thickness. Sheet resistance depends only on the film thickness and resistivity and not on the area of the sheet, which can vary because of pattern alignment, film etching or the damascene trenching. This is an important consideration when using the Greek cross, by making the area of the Greek cross large compared to the minimum line width, because by avoiding the effects of area variations, accurate results are ensured.

Line width measurement

A simple metal line divided into square blocks is shown in Figure 4. Because sheet resistance represents the resistance of a single square sheet, the resistance of the line shown in Figure 4 can be expressed using the L/W ratio as shown in Equation 2 below:

$$R_L = Rs \times \frac{L}{W} \qquad (2)$$

where;
R_L= Resistance of linear bridge
Rs= Sheet resistance
L= Linear bridge length
W= Linear bridge width

The metal film thickness of the Van der Pauw bridge and linear bridge test structures in Figure 3 should be very similar because they are located very close each other. Thus, the line width can be measured using Equation 3 below, which is derived from Equation 2.

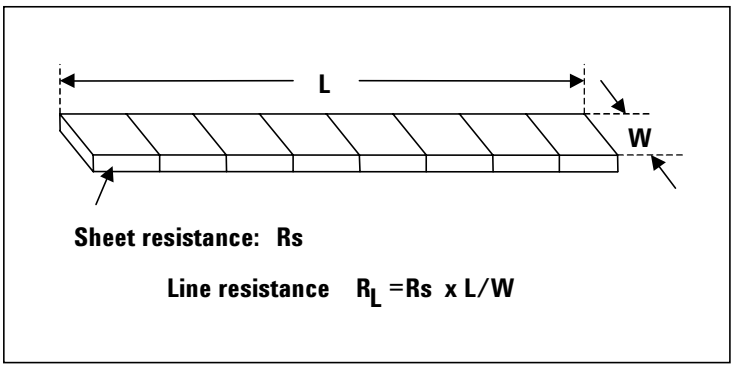

Figure 4. Metal line shown as a series of square blocks.

$$W = Rs \times L/R_L = Rs \times L\frac{I_{35}}{V_{46}} \qquad (3)$$

where;

W= Line width
Rs= Sheet resistance
L= Designed line length
R_L= Resistance of linear bridge with length L
I_{35}= Current forced between pad 3 and 5
V_{46}= Voltage measured between pad 4 and 6

By ensuring that Rs is the same in both Equations 2 and 3 above, you can solve for W.
The line length L is chosen to be much larger than process variations, resulting in an accurate measurement of line width.

Tips for accurate characterization

This line width measurement technique is simple and good accuracy can be achieved if the following error factors are eliminated during wafer testing.

1. The thickness of the metal line is not uniform in both the Greek cross and the linear bridge test structures.
2. The Joule heating increased the temperature of the bridge test structures thereby increasing resistance.
3. The offset voltage of the measurement system and test structures is not properly cancelled.
4. The measurement system does not have enough resolution and accuracy.

These four points are discussed in the following section.

Uniform metal thickness

Chemical-mechanical polish (CMP) is widely used to planarize each layer in the wafer process. In the case of copper, the CMP process tends to polish wider lines more than narrower lines, which causes wider lines to be thinner (known as CMP dishing). This results in higher than expected sheet resistance, and produces an error in calculating line width. Making the area of the Greek cross smaller reduces the

CMP dishing at the expense of increased impact of other processing variables such as etch variations etc. discussed above.

Heating of Greek cross

Joule heating associated with the smaller Greek cross is caused by the measurement current that is applied to the test structure. Joule heating increases the resistance of metal and causes an over-estimate of the sheet resistance.

At or near room temperature, the resistance of the metal line (in both copper and aluminum) changes 0.35%/$°C$. Thus an increase in temperature of 3 $°C$ will cause a roughly 1% increase in resistance and a roughly 1% error in sheet resistance. Assuming the heat flow of the test structure is straight down from the surface of the insulation layer (SiO_2) to the wafer bulk as shown in Figure 5(a), the thermal resistance is expressed as in Figure 5(b). Thia is about 0.007$°C$ /W/cm^2 for 1μm thickness SiO_2 and means if you apply 1W for a 1 square cm metal on 1μm thickness SiO_2,, the metal temperature rises 0.007 $°C$. If the area size is 10 μm square, then the metal temperature increases to 7,000 $°C$.
In this example, the test structure resistance increases by TCR x temperature change and represents a 2,450% (=0.35% /$°C$ x 7,000$°C$) increase. Of course both copper and aluminum will have vaporized before such an extreme temperature is reached.

As a more practical example in a real test environment where the target accuracy of the metal width

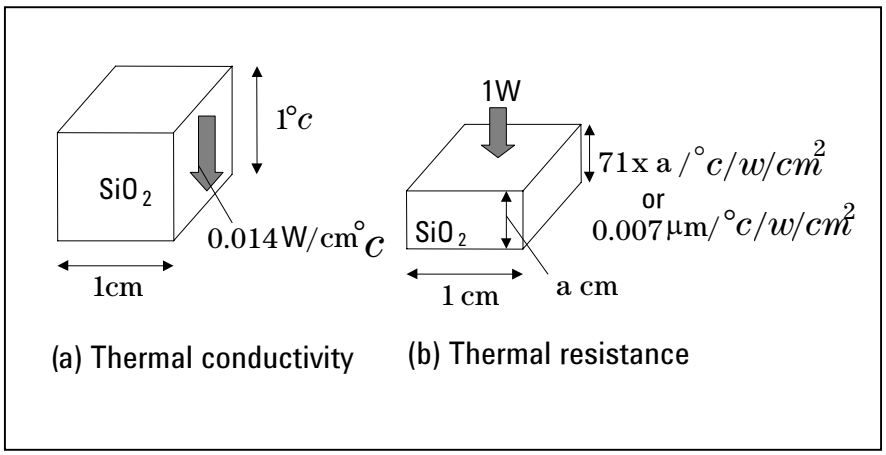

Figure 5. Illustration of the thermal property of an insulator one cm thick and one cm in area.

measurement is 1% and to support that, 0.1% accuracy or resolution is commonly required for base measurements of the resistance or the temperature.
In this case, the allowable maximum power is 0.04 mW (=1W x 0.1% / 2,450%), or the allowable temperature rise is 0.3 $°C$ (=7,000$°C$ x 0.1% / 2450%) for a 0.1% base error.
The allowable maximum power for required accuracy is generally expressed in Equation 4 below:

Pmax = 4e-6 x Error x Area/T (4)

where;
Pmax= Allowable maximum power (W)
Error= Sheet resistance error caused by self heating (%)
Area = Greek cross area (μm^2)
T= SiO2 thickness (μm)

If low-k materials are used instead of SiO_2, the temperature rises more because the thermal resistance is typically two to three times higher for these materials and lower power is required to obtain the same accuracy as compared to the SiO_2 insulator.

Accuracy of the sheet resistance measurement

Suppose the target measurement accuracy of a line width measurement is 1%, and then the required accuracy is 0.1% for both the temperature rise of the test structure and the measurement resolution.

The power applied to the Greek cross bridge is defined in Equation 5 below:

Pg = Rs/π x ln 2 x I^2

or $\frac{1}{Rs} \text{ x } \frac{\pi}{\ln 2} \times V^{\,2}$ (5)

Where;

Pg= Power applied to Greek cross
Rs= Sheet resistance
I= Current forced in Greek cross bridge
V= Voltage measured in Greek cross bridge

The approximate sheet resistance of typical 0.5 μm thickness film at room temperature is shown in the following example:
Rs - Aluminum : 53 mΩ/square /0.5 μm thickness
Rs - Copper: 34 mΩ/square/0.5 μm thickness

Because the power applied to the Greek cross (Pg) must be smaller than allowable maximum power (Pmax) that changes the sheet resistance 0.1% by Joule heating, the following equation can be delivered from Equations 4 and 5 above.

$$\frac{1}{Rs} \text{ x } \frac{\pi}{\ln 2} \times V^2$$

=< 4E-6 x Error x Area /T (6)

By solving this equation by V, the following condition can be obtained.

V =< 9E-4 x SQRT(Error x Area x Rs / T) (7)

or

$$I =< \frac{\pi}{\ln 2} \times \frac{V}{Rs}$$

$$=4E\text{-}3 \text{ x SQRT } \left(\frac{Error \times Area}{Rs \times T}\right) \quad (8)$$

Suppose the following condition is set as an example;
Area= 10μm square (100 μm^2)
T= 0.5 μm
Rs= 34 mΩ (copper)
Error= 0.1 %

The result is V =< 740 μV
or I=< 98 mA.

Because the target accuracy of measurement is 0.1%, a minimum 0.74 μV (=740/1000) resolution is required to characterize sheet resistance to 0.1% resolution.

This level of measurement is difficult to achieve using the 4155A/B and 4156A/B parameter analyzer and in order to get this resolution, a custom-built system with precision volt meter is required.

Accuracy requirement in the linear bridge measurement

The generic requirement for the linear bridge is the same as the sheet resistance measurement but is less strict.

The maximum current requirement is the same to the sheet resistance measurement. The area is replaced by the square of the line width, and the required voltage is found by simply by multiplying maximum current, resistivity and L/W ratio, as shown in the equations below.

$$I =< 4E\text{-}3 \text{ x SQRT } \left(\frac{Error \times W \times W}{Rs \times T}\right) \quad (9)$$

$$V =< I \text{ x } Rs \text{ x } L/W \text{ or } 4E\text{-}3 \text{ x } L \text{ x SQRT } \left(\frac{Error \times Rs}{T}\right) \quad (10)$$

In Equation 10, the voltage requirement comes only from the line length and not the line width. The L of the linear bridge is longer than 50 um in most cases and the minimum V can be expected to be 16.6 mV (=4E-3 x 50 x SQRT(0.1 x 0.034 / 0.5)) for 0.5μm thickness metal on 0.5 μm SiO2.
If the sheet resistance is measured accurately, the linear bridge measurement easily follows.

Solution

The voltage measurement accuracy of the new Agilent 4155C/4156C VMU is 0.2μV resolution, and maximum 10μV offset performance is suitable in this application.

At this level of low signal measurement, the following factors must be controlled to achieve the required accuracy.

1. White noise and power line noise
2. Offset and drift
3. Thermo electro-motive force (EMF)

These topics are discussed in the following section

Reducing noise

To achieve 0.2μV resolution, medium integration time is essential and long integration time is desirable in noisy environments in order to mitigate the effect of power line noise. Also minimizing the surrounding area of the two voltage measurement coaxial cables from the 4155C/4156C, by tying together, is very effective to reduce the magnetic coupled power line noise.

Compensating for offset and drift

There are following factors must be taken into consideration when measuring voltage.

1. Voltmeter offset and thermo-EMF
2. Drift of the voltmeter offset and thermo-EMF

These factors can be eliminated by performing a Zero Cancel Offset operation while devices are connected to the VMU. The drift component, however, varies by time and compensation measurement must be done while these factors are stable. The major causes of drift are a result of a change in room temperature or an increase in test structure temperature. It is, therefore, important that the measurement instrument be adequately warmed up, and the temperature of the room and the test structures kept constant.

Reducing Thermo-EMF

To compensate the thermo-EMF, the temperature of the test structure must be the same while measuring the offset voltage and resistance. As stated above, to use the cross-bridge technique requires minimal Joule heating of the test device.
A technique which reverses the current to cancel any voltage offset due to thermo-EMF is a fool-proof approach.

The reverse current method measures the resistance first in forward current force mode, as shown in Figure 6(a), and then reverses the current as shown in Figure 6(b). By subtracting the second measurement from the first and then dividing the result by twice the If (I force), you compensate for both voltmeter offset and thermo-EMF and you get the exact resistance. This technique also reduces the noise and keeps the test structure temperature stable while measuring offset voltage and resistance, with the result being better accuracy.

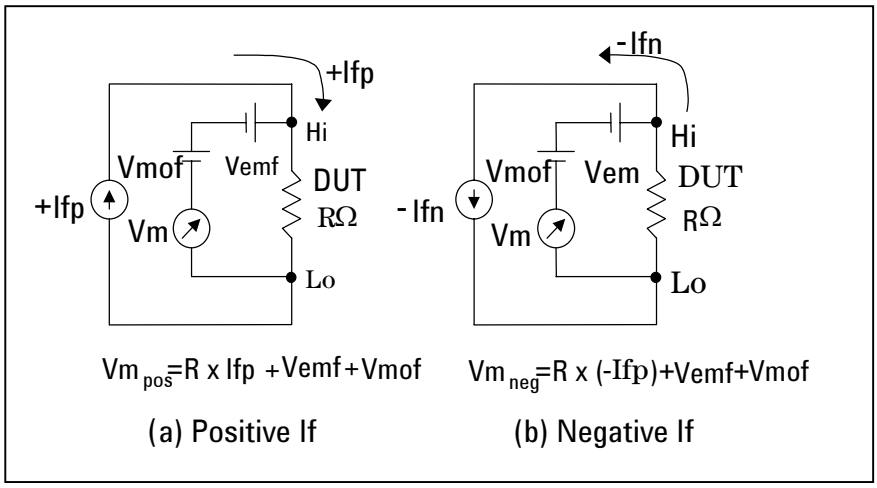

Figure 6. Vm and EMF offset can be eliminated by measuring positive If and negative If.

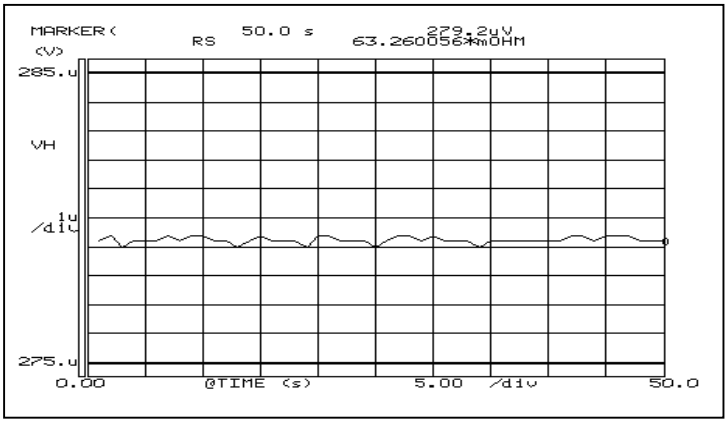

Figure 7. Noise and drift on a Van der Pauw bridge remain below 0.4 uV p-p for 50 sec with forcing current at 20mA.

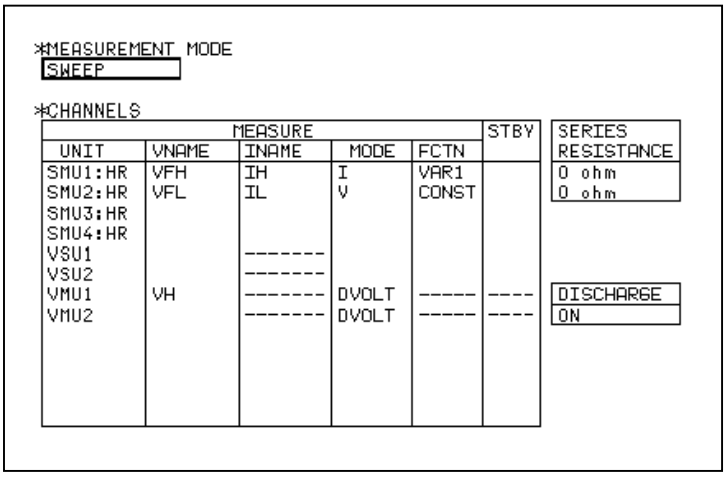

Figure 8. Channel definition setup of Van der Pauw bridge or linear bridge measurement.

An example of the noise and drift variation of the Van der Pauw bridge measurement made by 4155C/4156C is shown in Figure 7. The peak-to-peak voltage variation, including the drift, is less than 0.5μV and this satisfies the required accuracy.

Automatic cancellation of the offset and sheet resistance calculation

The 4155C/4156C can measure sheet resistance and line width automatically by using the User Function.

Examples of setting and measurement results of the Greek cross bridge made by the 4156C is shown in Figures 8 through 12.

Sheet resistance calculation using Equation 1 and elimination of the offset component shown in Figure 6 is achieved by taking the average of the absolute value of the forward and reverse measurement results using User Function line 1 shown in Figure 9.

Line width can be measured in a similar fashion by using the User Function, as shown in lines 2 through 4 in Figure 9.
RSET is the sheet resistance obtained from RS, and used in line width calculation.
LSET is a designed line length.
WIDTH calculates line width using Equation 3.

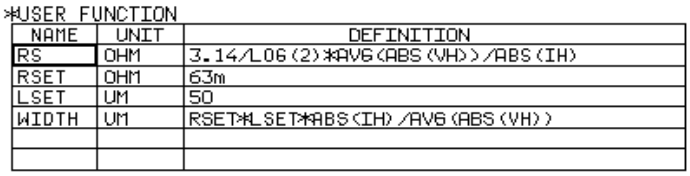

Figure 9. User Function setup for automatic parameter calculation.

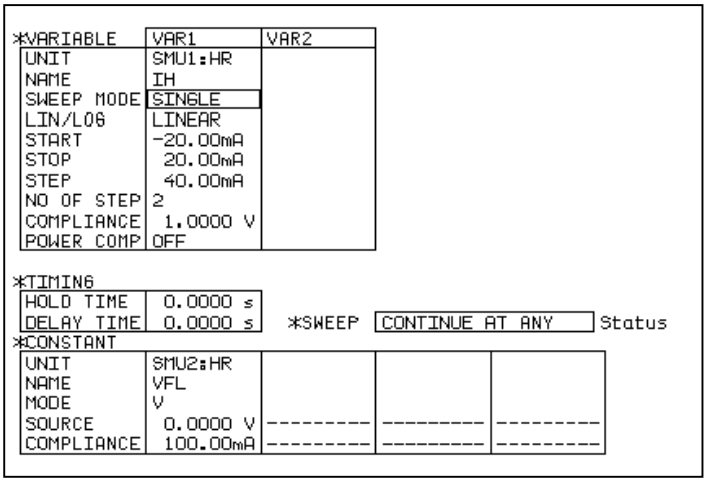

Figure 10. Sweep setup information.

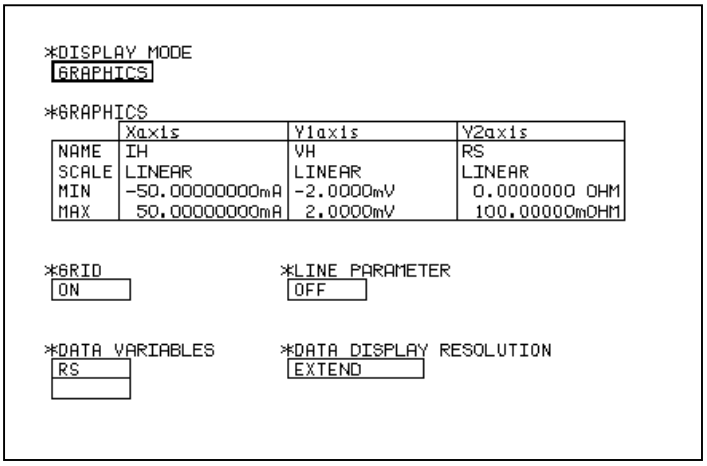

Figure 11. Display mode setup information.

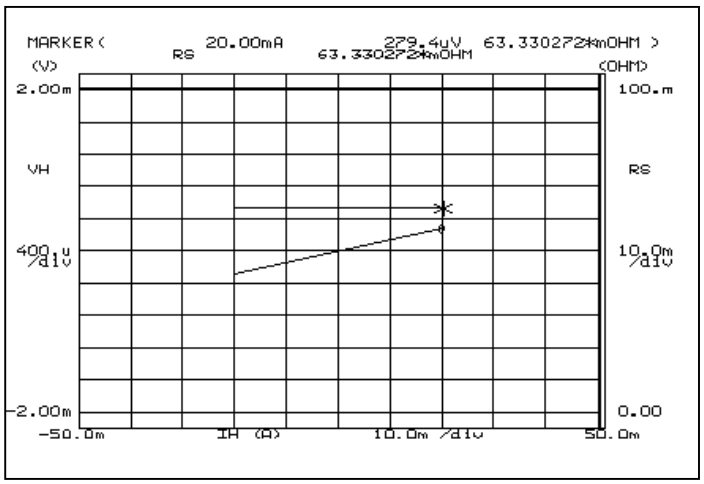

Figure 12. Graphic display of Van der Pauw bridge measurement and auto analysis display.

Conclusion

The new Agilent 4155C/4156C is suitable for precision metal line width characterization in a narrow sub-quarter micron interconnect system.

The improved VMU provides 0.2μV voltage measurement resolution and a guaranteed worst case offset stability of 10μV.

The User function provides an easy-to-use automatic analysis capability without programming.

These performance capability satisfy the requirements for precision measurement of metal line width in sub-quarter micron interconnect systems.

Reference:
ASTM Standard F1261M-95

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