Evaluation of Gate Oxides Using a Voltage Step Quasi-Static CV Method

Application Note 4156-10

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Agilent Technologies

Introduction

Capacitance versus voltage (CV) characteristics measured with the Quasi-Static CV (QSCV) method are important for device characterization. High-frequency CV (HFCV) curves do not yield knowledge about MOS oxide behavior in the important inversion regime; only QSCV curves can reveal this information. Thus, QSCV measurements are critical for the analysis of modern thin-oxide MOS processes.

The classical QSCV method uses a linear voltage ramp and calculates capacitance from the following equation:

$$C = \frac{I}{dV/dt} \quad [F]$$

However, obtaining a successful QSCV measurement using this technique usually entails some trial and error to select the proper hold time and ramp rate. In addition, the technique does not work for gate oxides thinner than approximately 40 angstroms, since at this oxide thickness the gate leakage current starts to become comparable to the capacitance current being measured.

The Agilent 4155C and 4156C use a step voltage technique instead of the linear ramp technique to obtain the QSCV measurement. In general, this method is easier and quicker to perform than the linear ramp method. Moreover, the 4155C and 4156C have a unique current compensation feature that enables the measurement of leaky gate oxides. This application note describes efficient parameter selection methods for QSCV measurements made with the 4155C and 4156C. The note details the measurement theory so you can obtain superior QSCV results as shown in Figure 1, without having to go through a tedious trial and error process.

The Voltage Step Quasi-Static CV Measurement Method

The voltage step QSCV method calculates capacitance from the differential charge required to change the capacitor voltage by an amount ΔV. The charge Q of a capacitor has the relation with an applied voltage V and capacitance C as follows:

$$Q = CV$$

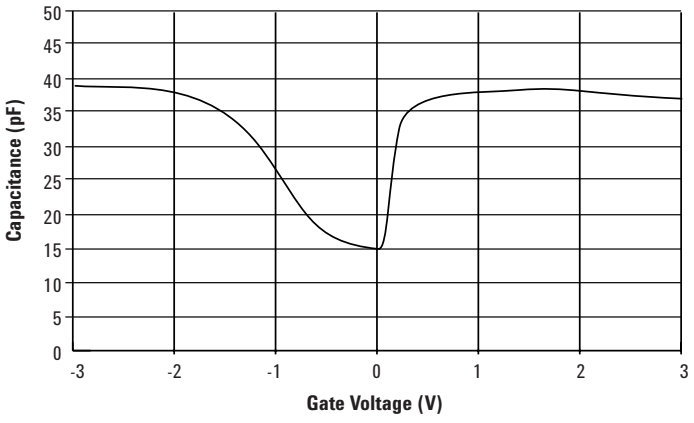

Figure 1. Sample Quasi-Static CV characteristics

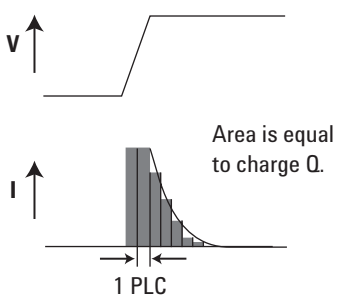

Figure 2. Rectangular approximation method used by the 4155C and 4156C

Thus, when the applied voltage changes from V_0 to V_1, the charge on the capacitor must change from Q_0 to Q_1 (assuming C is constant). That is, when the applied voltage changes by *Vstep* (=V_0–V_1), the total charge must also change by an amount ΔQ.

You can calculate this change in charge ΔQ by integrating the current i.

$$\Delta Q = \int i dt$$

The Agilent 4155C and 4156C calculate this area using the rectangular approximation method shown in Figure 2.

The width of each rectangle is equivalent to one power line cycle (PLC). Thus, the actual equation used in calculating the change in charge is:

$$\Delta Q \approx \sum I_k \bullet \Delta t_{PLC}$$

The 4155C and 4156C use two different step voltages to measure capacitance, and it is important not to confuse them. Figure 3 shows the actual voltage waveform forced on the capacitor during a QSCV measurement. The *step voltage* term determines the points along the total CV sweep where the capacitance is to be measured. The *cvoltage* term refers to the voltage step applied to the capacitor at each point along the capacitance measurement curve. Obviously, *cvoltage ≤ step voltage*.

The QSCV measurement operation is as follows:

1. After the QSCV measurement trigger, the SMU forces *start voltage*.
2. Change the output to (*start voltage+step voltage–Vq*) and wait for *hold time*.
3. Wait for *delay time*.
4. Measure output voltage V_0.
5. Measure leakage current IL_0.
6. Start the AD conversion and change the output voltage by *cvoltage*. The AD conversion continues for *cinteg*.
7. Measure the output voltage *V*.
8. Measure leakage current *IL*.
9. Calculate the capacitance over k power line cycles (PLCs) using the following equation:

$$C = \frac{\Delta Q_{Cap}}{\Delta V} = \frac{\Delta Q_{Total} - \Delta Q_{Leak}}{\Delta V}$$

$$= \frac{\left(\sum_k I_k \cdot \Delta t_{PLC}\right) - \left((0.5)(IL-IL_0)(2 \cdot cinteg - (j-0.5) \cdot \Delta t_{PLC})\right)}{V - V_0}$$

$j \in \{1, 2, 3,...k\}$ and *j* is the PLC in which the VAR1 SMU is no longer in current compliance (I compliance).

10. Change the output to (*start voltage+2_step voltage–Vq*) and wait for delay time. This is similar to the step 3.
11. Continue the steps between 4 and 10 until the last step.
12. After the QSCV sweep completes, the output voltage is changed to 0 V.

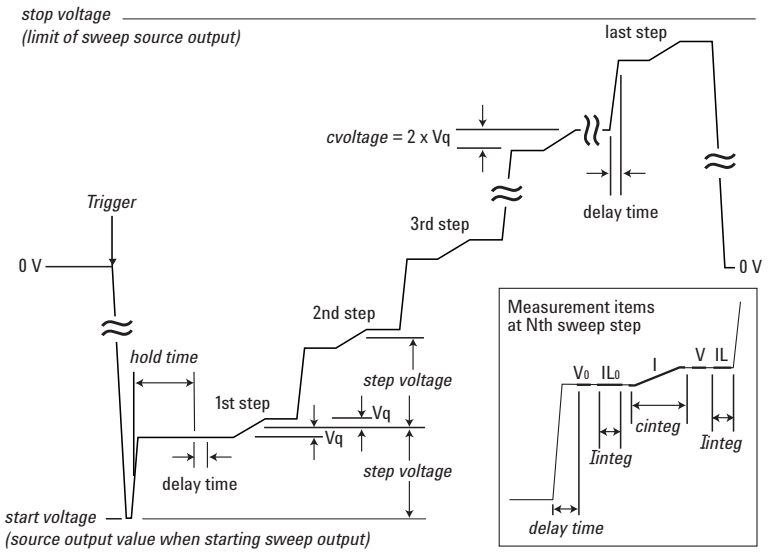

Figure 3. QSCV measurement sequence

Many parameters are necessary to define a QSCV measurement using the step voltage technique and these parameters are summarized in Figure 4.

One important case to consider is when *step voltage* is set equal to *cvoltage*. In this case, the voltage step operation is not necessary and the output voltage sequence is as shown in Figure 5 on page 4. Because in this case *delay time* can be set to zero (although it does not have to be zero), the total CV sweep time can be reduced.

Parameter Name	Description
start voltage	Start voltage of CV sweep.
stop voltage	Stop voltage of CV sweep.
step voltage	Step voltage of CV sweep.
cvoltage	Capacitance measurement voltage. This value must be less than absolute of step voltage.
hold time	Time from the start of the first sweep step to the beginning of the delay time.
delay time	Time from the start of each sweep step to the start of the measurement.
Iinteg	Integration time for the leakage current measurement.
cinteg	Integration time for the capacitance measurement.
Im range	Measurement range of an SMU used for QSCV measurements.
I compliance	Current compliance of an SMU used for QSCV measurements.

Figure 4. Parameters for QSCV Measurement

MOS Device Model for QSCV Measurement

The term MOS stands for metal-oxide-semiconductor, and you can model this structure as a capacitor. However, its capacitance characteristics depend on the applied gate voltage. The MOS structure has three states: *accumulation, depletion, and inversion,* as shown in Figure 6. Note that here a p-bulk (NMOS) structure is depicted. If the silicon is held at ground and a negative voltage is applied to the gate, the MOS capacitor will begin to store positive charge at the silicon surface. The surface has a greater density of holes than N_a (the acceptor density), and this condition is known as surface accumulation. In this condition the mobile charge on both sides of the oxide can respond rapidly to changes in applied voltage, and the device looks just like a parallel plate capacitor of thickness *Tox*. Since it is a pure gate oxide capacitance, we denote its value as *Cox*.

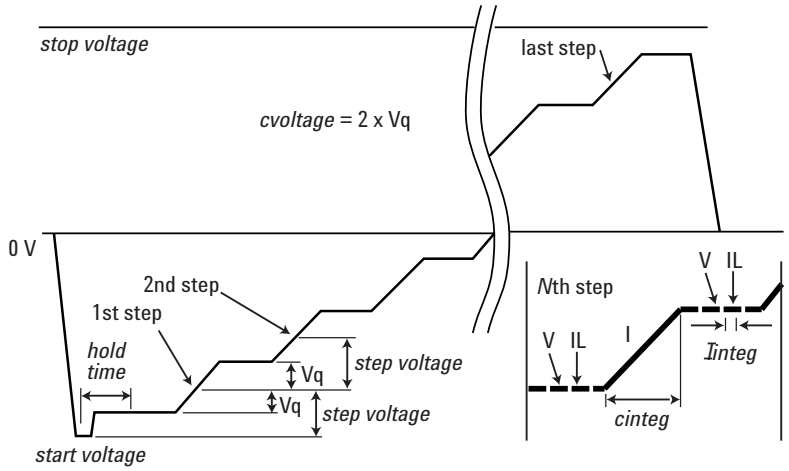

Figure 5. QSCV measurement sequence (*step voltage = cvoltage*)

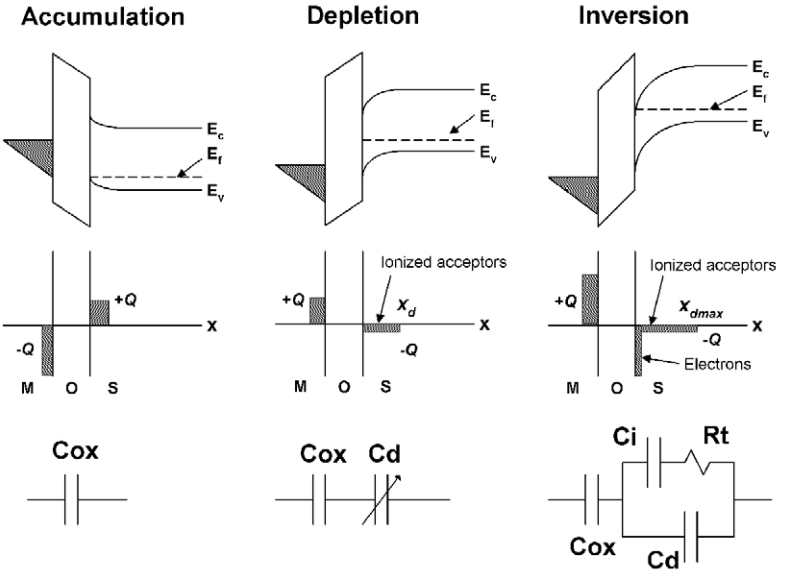

Figure 6. Energy bands, block charge models, and equivalent circuit for NMOS structure

If a positive gate voltage is applied to the gate relative to the silicon, the built-in positive voltage between the gate and silicon is increased. The silicon surface becomes further depleted of carriers as more acceptors become exposed at the surface, resulting in the condition known as surface depletion. In this condition electrostatic analysis shows that the total MOS capacitance consists of the series combination of Cox and the capacitance across the surface depletion region, *Cd*. The series combination of these two capacitors results in a total capacitance value lower than the value of Cox. Note that Cd depends upon the applied voltage.

If the positive gate voltage is further sufficiently increased, then the energy bands bend away considerably from their levels in the bulk of the silicon. The depletion region reaches a maximum width, x_{dmax}, and all of the electron acceptors within this region are fully ionized. In the surface region generation of carriers exceeds recombination, and the generated electrons are swept by the electric field into the oxide-silicon interface where they remain due to the energy barrier between the conduction bands of the silicon and the oxide. Thus, the total charge in the silicon consists of the sum of these two charges. Electrostatic analysis again shows that the total MOS capacitance can be modeled as the oxide capacitance in series with the parallel combination of the deple-

tion capacitance and the series combination of inversion charge capacitance, *Ci* and the depletion resistance, *Rt*.

In the inversion regime, the minority carrier electrons at the oxide surface can only be supplied as fast as the generation rate in the p- bulk. Thus, if an applied voltage is varied slowly enough to allow the generation rate to respond to it, then the depletion charge is not a factor in the incremental capacitance. The inversion capacitance is typically much larger than either the depletion capacitance or the oxide capacitance (i.e. Ci >> Cd and Ci >> Cox). Assuming Rt is negligible, basic circuit theory shows that in this case the total capacitance is very close to the value of the oxide capacitance, *Cox*. However, if an applied voltage is varied too quickly, then the electrons cannot respond and the depletion charge must modulate in response. The inversion charge cannot form, so once again we have the series combination of Cox and Cd.

Note that by using some means to stimulate the generation rate, you can raise the frequency at which quasi-static behavior occurs. This can be done either by illuminating the surface, or by allowing the inversion layer to make an ohmic contact to a region with which it can exchange carriers. Normally, you want to stimulate the generation rate up until the time when you actually start your QSCV measurement. This insures that the minority carriers in your MOS capacitor are fully stabilized and that your MOS device is solidly in the inversion state.

Efficient Measurement Parameter Selection

The previous sections detailed the many parameters necessary to make a QSCV measurement. This section describes efficient methods of selecting these parameters.

Step 1 – Selecting Basic Sweep Parameters

The first parameters you must select are *start voltage*, *stop voltage*, *step voltage*, and *cvoltage*.

You must start your CV sweep with the device solidly in inversion. For an NMOS device (p- bulk) this means that the *start voltage* you apply to the gate should be positive, and much greater than the equivalent NMOS transistor threshold voltage. Your *stop voltage* should be of equal magnitude and opposite polarity to your *start voltage* to insure that you measure CV through all regimes of device operation. Obviously, *step voltage* just determines the number of measurement points you take between the *start voltage* and *stop voltage* values. In general, smaller values of step voltage result in smoother curves due to the increased number of measurement points. In this example, we will sweep from *start voltage* = 3.05 V to *stop voltage* = -3.05 V, using a *step voltage* of –50 mV.

There is an obvious trade-off between *cvoltage* and *cinteg* (the capacitive current integration time). Larger cvoltage values require longer cinteg times (and vice versa), although cinteg also depends upon the noisiness of your measurement environment. In general, 50 mV is a good starting point for a value for cvoltage.

Step 2 – Determining Measurement Range

To determine the appropriate QSCV current measurement range, you should do an IV sweep measurement of the gate oxide leakage current. Use the start, stop, and step voltages determined in Step 1. Make sure you sweep in the same direction as you intend to in your quasi-static CV sweep (in this case, from positive to negative). Also note that sufficient hold and delay time must be used to allow the dielectric absorption current in the oxide and depletion layer to be removed.

Figure 7 shows a sample leakage measurement result, both with and without external illumination. A full explanation of the traces shown in Figure 7 would require too much space in this note and, in any case, is not pertinent to the selection of the appropriate current measurement range. The key point is that the large negative current spike seen in the measurement made in darkness corresponds to a point where the MOS capacitor is briefly entering a quasi-static mode of operation. Since

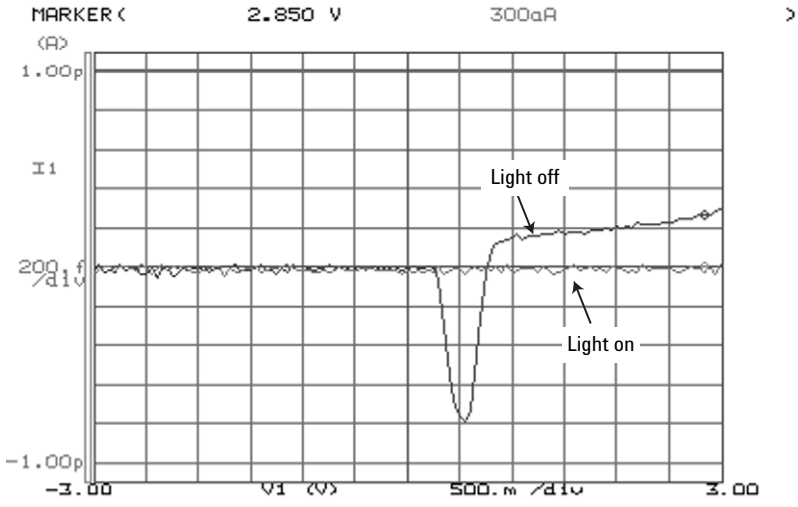

Figure 7. Leakage current of oxide with and without external illumination

this is the mode in which you want to measure, the magnitude of this spike is the important parameter. In this example, 800 fA is the maximum leakage current, so the 10 pA range can be used for the 4156C, and the 1 nA range can be used for the 4155C. Note: In general you want to select as low a current range as possible, since lower current ranges yield more accurate capacitance measurements.

Step 3 – Selecting Hold Time

The *hold time* determines how long the instrument waits before starting to make a capacitance measurement. Agilent suggests that you place the SMUs into standby mode, press the "Standby" button, and wait several seconds with some sort of minority carrier stimulation in place before starting your QSCV measurement. This eliminates the need to worry about the response time of your capacitor.
If you follow the above procedure, then the purpose of *hold time* is simply to allow you enough time to shut off your method of minority carrier stimulation before the actual start of your CV sweep. For example, if you are manually shutting off a microscope light after starting your measurement, two seconds is generally enough allowable hold time. Note: If you are not turning off your minority carrier stimulation during your QSCV sweep, hold time can be set to zero.

Step 4 – Determining Delay Time and Capacitance Measurement Integration Time

In step 3, the *hold time* necessary to match a given *start voltage* was determined. Now the appropriate *delay time* and *cinteg* time for the chosen *step voltage* must be determined. Note: Even though in this example *step voltage* = *cvoltage*, the delay time does not have to be set to zero. In this case a non-zero delay time effectively determines the delay between voltage steps.

In a case where *step voltage* does not equal *cvoltage*, you can generally set the delay time to a value of 100 ms to 200 ms and obtain a satisfactory QSCV measurement result. Exceptions to this would be where capacitors are larger than 100 pF and *step voltage* values fall somewhere between 100 mv to 200 mV. However, for most practical and modern MOS devices you would not have values larger than either of these. For the example shown, since *step voltage* = *cvoltage,* the delay time was set to zero in order to speed up the QSCV sweep.

The *cinteg* time you choose is usually the most critical parameter you must select in order to get a good QSCV curve. However, it is also one of the most difficult parameters for which to create a mechanical process to determine its value. Many parameters such as carrier lifetime, oxide thickness, and capacitor size can affect the optimal *cinteg* value. A good rule of thumb is to start with a small value for cinteg, such as 100 ms, and perform a fast sweep with some sort of minority carrier stimulation in place (usually illumination). This allows you to establish a baseline value for cinteg. You can then repeat the QSCV sweep in darkness, gradually increasing the value of cinteg until you obtain a satisfactory QSCV curve. You must be careful not to make the cinteg time longer than necessary so you do not start integrating noise and making your QSCV sweep appear ragged.
Figure 8 shows the effect on QSCV curves done in darkness with a gradually increasing value of cinteg. For this wafer and device, the optimal value of cinteg was 750 ms.

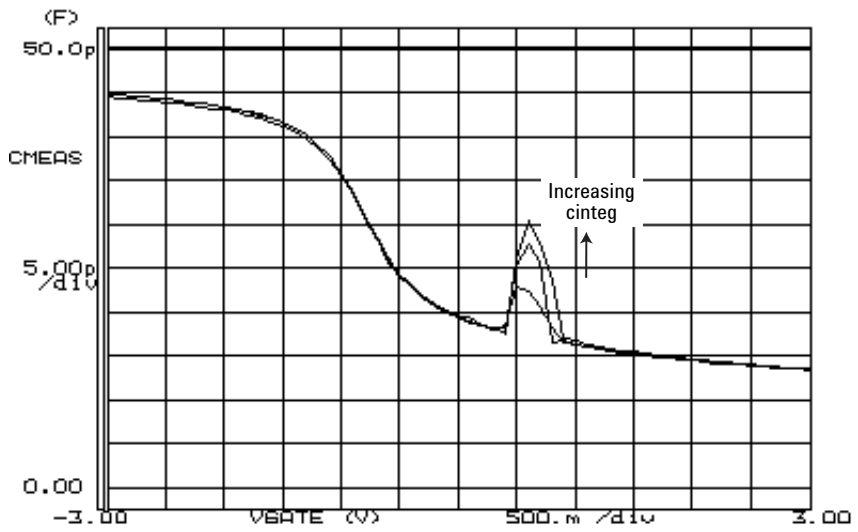

Figure 8. Effect on QSCV curve of increasing cinteg

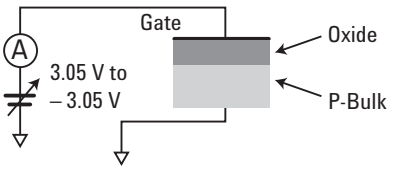

Figure 9. Circuit for QSCV measurements

Step 5 – Execution of the QSCV Measurement

In the previous sections, the appropriate parameters for the QSCV measurement were determined. This section describes how to enter these parameters into the measurement setup pages and how to execute the QSCV measurement.

Figure 9 shows the equivalent circuit for the QSCV measurement. The gate is connected to an SMU, and the bulk or substrate is connected to the circuit common.

Figure 10 shows the setup of the CHANNELS: CHANNELS DEFINITION page. The MEASUREMENT MODE field on the right of the screen is set to QSCV. SMU1 is set to be in voltage force mode (V) and assigned as the primary sweep source (VAR1). SMU2 is set to be the circuit common. Also note that the standby mode (STBY) mode for both of these sources is set to ON.

Figure 11 shows the CHANNELS: USER FUNCTION DEFINITION page set up to automatically extract and display the oxide thickness, *Tox*.

This page uses the following equation to calculate *Tox*:

$$Tox = \frac{AREA \bullet 10^{8} \bullet \varepsilon_0 \bullet \varepsilon_d}{Cox} \quad [\text{angstroms}]$$

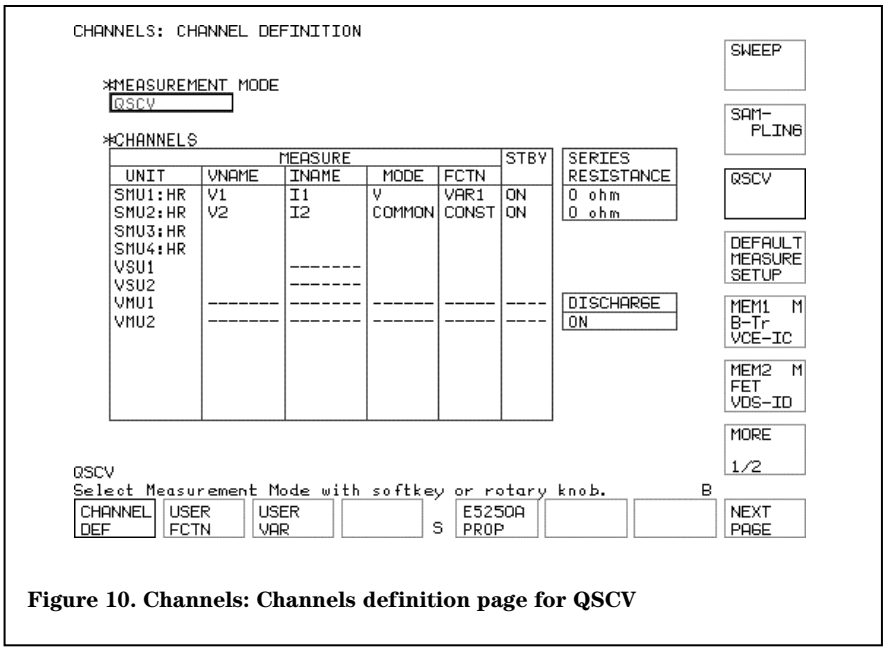

Figure 10. Channels: Channels definition page for QSCV

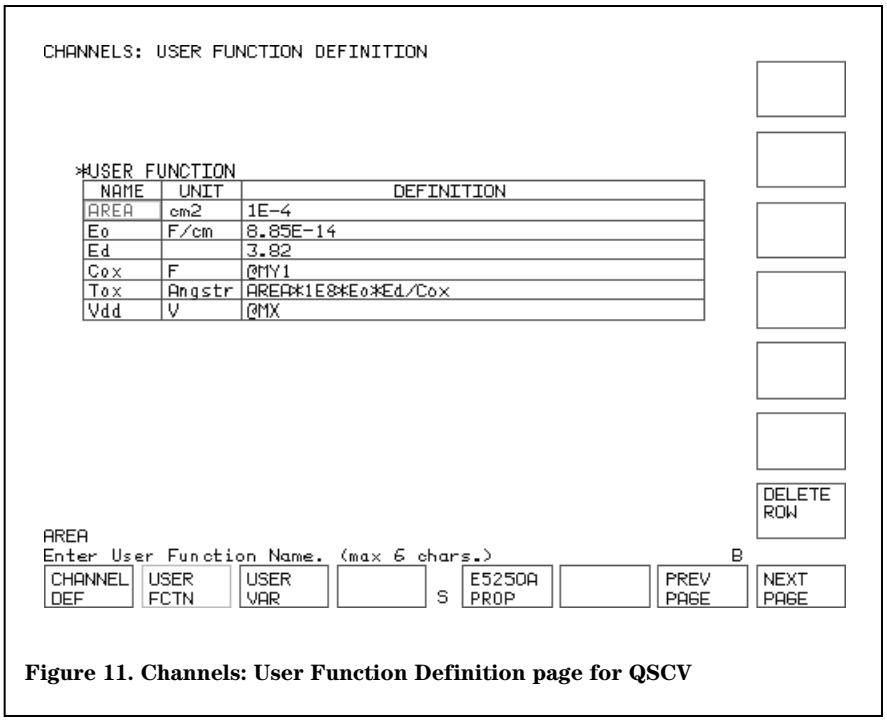

Figure 11. Channels: User Function Definition page for QSCV

Where

AREA is the capacitor gate area [cm^2];

ε_0 is the free space permittivity (8.854×10^{-14} F/cm);

ε_d is the dielectric constant of SiO_2 (3.9); and

Cox is the measured capacitance in heavy accumulation (Vg bias = Vdd) [F].

Figure 12 shows the MEASURE: QSCV SETUP page. On this page *start voltage*, *stop voltage*, *step voltage*, *compliance*, *cvoltage*, *hold time*, and *delay time* are specified. Note: The *cvoltage* is specified in the QSCV MEAS VOLTAGE field.

Pressing the "MEASURE SETUP" softkey at the bottom of the MEASURE: QSCV SETUP page accesses the MEASURE: QSCV MEASURE SETUP page, shown in Figure 13, on which *measurement range*, *cinteg*, and *Iinteg* are specified. You can also change the names of the capacitance and leakage current variables (CNAME and INAME). The *cinteg* and *Iinteg* times are entered in the QSCV and LEAK fields of the INTEG TIME, respectively. The LEAK COMPENSATION field allows you to turn the leakage compensation on or off. Finally, if you perform an offset capacitance compensation of your measurement setup, the measured value will be displayed in the ZERO CANCEL field.

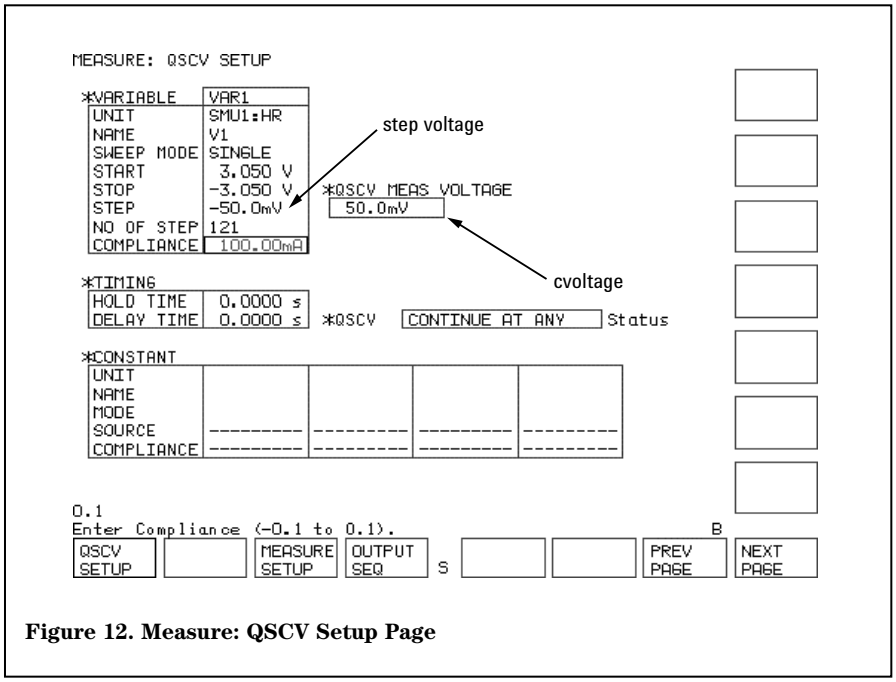

Figure 12. Measure: QSCV Setup Page

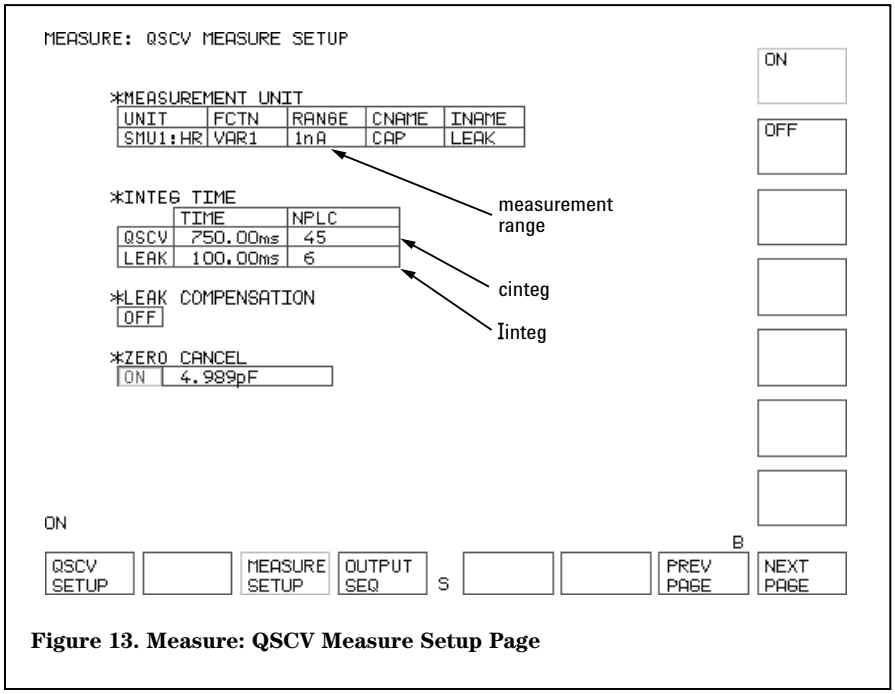

Figure 13. Measure: QSCV Measure Setup Page

Figure 14 shows an example of the DISPLAY: DISPLAY SETUP page. Here you need to define the X and Y axes for display on the graphics page. You can also specify variables (such as Tox) defined on the USER FUNCTION DEFINITION page to be automatically displayed each time you perform a CV plot.

Before performing a CV measurement, you should lift your measurement probes off of the capacitor and perform a zero offset cancel operation. This is accomplished by pressing the blank green key on the lower right portion of the instrument front panel, and then pressing the "Zero [Stop]" button in the upper right corner of the instrument Note that the word "Zero" is in green letters above the "Stop" button. The stray offset capacitance from probes, cables, etc. will be measured, and then this value will automatically be subtracted from each capacitance measurement. Please note that this operation only needs to be performed once for a given measurement setup.

Before starting the QSCV measurement you should press the "Standby" button in the upper right corner of the 4155C or 4156C in order to bias the capacitor to the voltage value at the start of the sweep measurement. You should also supply some method (such as illumination) to increase the rate of minority carrier generation. After waiting several seconds, you can push the "Single" button to start a single measurement

and quickly shut off whatever method of minority carrier stimulation you are using. In this case, the microscope light was shut off immediately after pressing the “Single” button.

You can, of course, perform the QSCV measurement with minority carrier stimulation in place during the entire sweep. In general, however, QSCV curves done with and without minority carrier stimulation are not the same. As one would expect, continuous minority carrier stimulation shifts the QSCV curve upward in the beginning of the inversion region .as shown in Figure 15. Nevertheless, since the value of the QSCV sweep is the same for both curves once you are fully into inversion, leaving some form of minority carrier stimulation in place during the entire sweep may be immaterial to you depending upon your application.

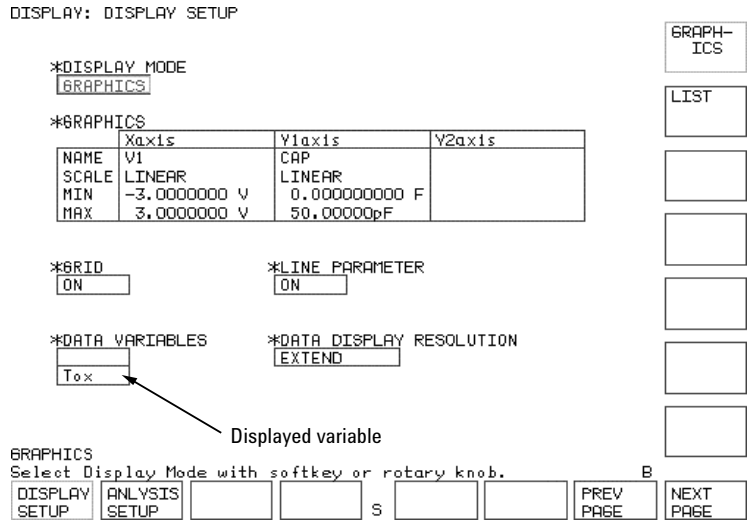

Figure 14. Display: Display Setup

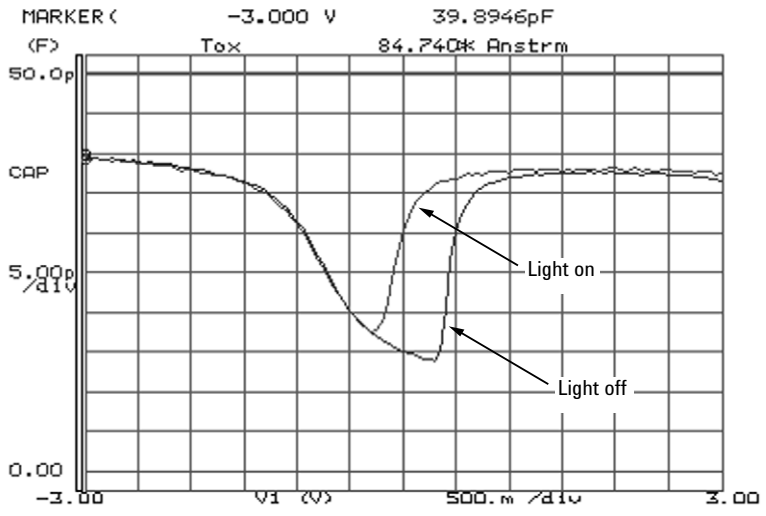

Figure 15. QSCV performed with both the light on and light off

Calculation of Semiconductor Parameters

You can use CV curves generated by the 4155C and 4156C to calculate important semiconductor parameters. The following steps outline this procedure for the sample CV plot shown in Figure 16. Note: Agilent can supply an IBASIC program that runs on the 4155C and 4156C and which automatically extracts the following parameters from a CV measurement curve.

Step 1 - Determine Nsub: Impurity Concentration of the Substrate

The following equations hold for oxides whose thickness is 40 angstroms or greater, and assume that Nsub is constant in the bulk.

$$Nsub = \frac{4 \cdot |\phi_f|}{q \cdot \varepsilon_0 \cdot \varepsilon_{si}} \cdot \left(\frac{Cs\,min}{A}\right)^2$$

$$\phi_f = \pm \frac{k \cdot T}{q} \cdot \ln\left(\frac{Nsub}{n_i}\right) \qquad \begin{array}{l} + : \text{p–type (NMOS)} \\ - : \text{n–type (PMOS)} \end{array}$$

where

ϕ_f is the Fermi potential, in Volts;

Csmin is the minimum depletion layer capacitance, in Farads;

A is the area of the poly gate, in cm^2;

n_i is the intrinsic carrier concentration per cm^3;

ε_0 is the free space permittivity (8.854×10^{-14} F/cm);

ε_{Si} is the dielectric constant of Si (11.7);

q is the magnitude of electronic charge (1.602×10^{-19} Coulomb);

k is Boltzman’s constant (1.38×10^{-23} J/K); and

T is the absolute temperature, in deg K.

The value of Csmin, which can be read directly off of the graph shown in Figure 16, shows that Csmin = 3.6826 x 10^{-11} F. Solving the above two equations iteratively using the method of successive approximations, we can determine Nsub:

Nsub = 8.3085 x 10^{16} [1/cm^3]

where

A = 0.0004 cm^2, and
T = 296 deg K.

Step 2 - Determine Vfb: Flat Band Voltage

For practical NMOS structures, a negative gate voltage is needed to produce the flat band condition. We can determine Vfb graphically by first determining the flat band capacitance, Cfb, and then reading the value of Vfb off of the CV curve.

The flat band capacitance is given by the following equation:

$$Cfb = \frac{Cox \bullet Csfb}{Cox + Csfb}$$

where

Csfb is the depletion layer capacitance under flat band conditions.

We can read the value of Cox graphically from Figure 16 by looking at the maximum value of the CV plot in the accumulation region, which is 1.0865 x 10^{-10} F. Note: This equation is just a restatement of the fact that in the depletion region the total capacitance of the MOS device consists of the series combination of the oxide (Cox) and depletion layer (Csfb) capacitances.

We can calculate the value of Csfb from the Debye length, λ, using the following equations:

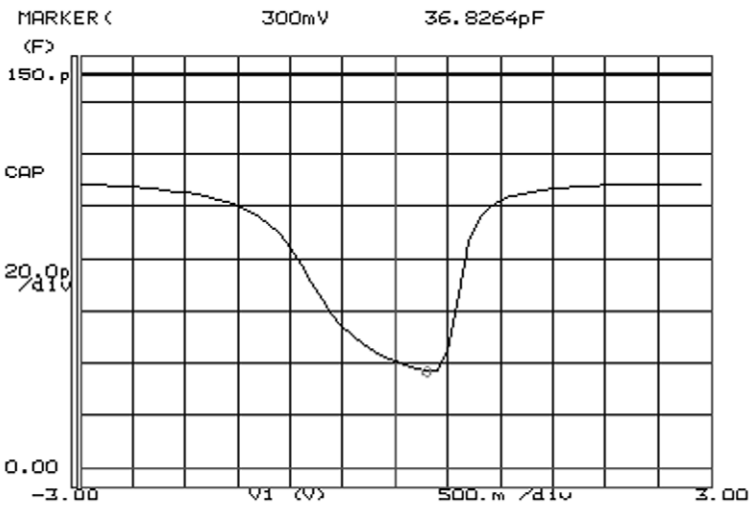

Figure 16. Sample QSCV plot to illustrate MOSFET parameter extraction

$$\lambda = \sqrt{\frac{2k \bullet T \bullet \varepsilon_0 \bullet \varepsilon_{si}}{q^2 \bullet Nsub}}$$

$$Csfb = \frac{\sqrt{2} \bullet A \bullet \varepsilon_0 \bullet \varepsilon_{si}}{\lambda}$$

Using the value of Nsub obtained in step 1, we obtain the following:

Csfb = 2.9414 x 10^{-10} [F]
Cfb = 7.9342 x 10^{-11} [F]

This allows us to graphically determine the value of Vfb to be –0.9 V.

Step 3- Determine Qss: Surface Charge Density

In the oxide layer of a practical MOS device there is a fixed surface charge. Mobil ions and ionized traps make up the surface charge, so the measured CV characteristics differ from those of an ideal MOS device. Since the surface charge depends upon the semiconductor orientation, oxidation, and annealing conditions, Qss is very important to the evaluation of wafer processes. The surface charge density is calculated from the following equation:

$$Qss = \frac{Cox}{A} \left| \phi_{MS} - Vfb \right|$$

where

Φ_{MS} is the difference in the work functions of the semiconductor (Si) and the gate (poly-Si). In this example, the following hold.

ϕ_f = 0.4066 V
ϕ_{MS} = -0.6 - ϕ_f = -1.0066 V
Therefore,

Qss/q = 1.8082 x 10^{11} [1/cm^3]

Step 4 - Determine Vth: Threshold Voltage

In theory you can calculate the threshold voltage of a MOSFET, Vth, from the following equation:

$$Vth = Vfb + \left(2\phi_f - \frac{A \bullet Q_b}{Cox}\right)$$

where Qb is the fixed charge per unit area in the depletion layer and is defined as follows:

$$Q_b = \pm q \bullet Nsub \bullet \frac{\varepsilon_0 \bullet \varepsilon_{si} \bullet A}{Cs\ min}$$

+ : n–type (PMOS)
– : p–type (NMOS)

For this example,
Q_b = -1.4976 x 10^{-7} [coulomb/cm^2]

Therefore,

Vth = 0.46466 V

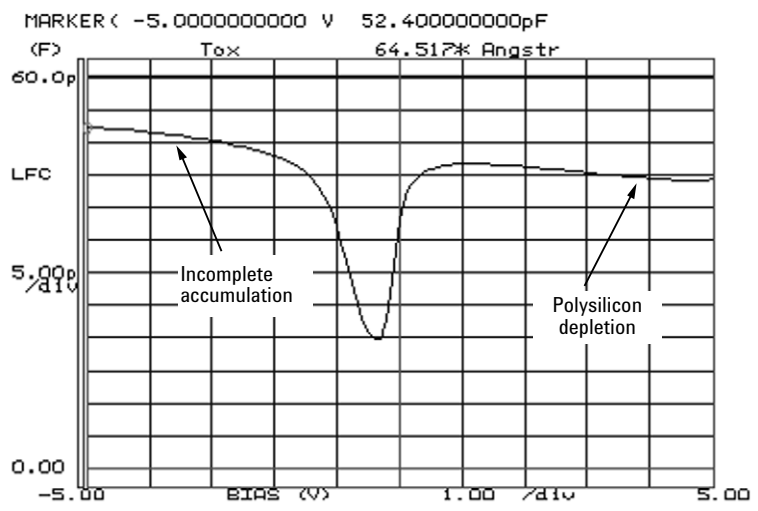

Figure 17. QSCV plot showing incomplete accumulation and polysilicon depletion

Thin Oxide Effects

Figure 17 demonstrates a major reason why QSCV analysis is important for today's thinner and more lightly doped polysilicon gate oxides. The CV curve now has a downward slope compared to the previous examples. This shape is characteristic of a thin oxide with n+ poly and a p- substrate.

In the accumulation regime, Fowler-Nordheim tunneling currents through the thin gate oxide make the CV curve slope downward and create the phenomena known as incomplete accumulation. The CV curve can never achieve a flat shape because the leakage current increases dramatically as the magnitude of the negative bias voltage is increased.

In the inversion regime, for thin oxides the polysilicon gate can start to act like an additional capacitor in series with the MOS device. This series capacitance acts to reduce the measured value on the CV curve. The amount of reduction in total capacitance depends upon the doping density of the polysilicon gate. For thin oxides, the polysilicon doping density should be above 2 x $10^{20}/cm^3$.

Leakage Current Compensation for Thin Oxide Evaluation

As gate oxides get thinner than 40 angstroms the gate leakage current generally starts to increase dramatically. This leakage current increases the error in capacitance measurements, and makes the classical linear voltage ramp method of QSCV measurement useless. However, the 4155C and 4156C possess a unique current compensation capability that can measure the capacitance of MOS devices with oxides as thin as 20 angstroms (depending upon process and capacitor area).

Figure 18 on page 12 shows simplified conceptual waveforms for the voltage step QSCV technique when background leakage current is both present and absent. Obviously in the case of leaky gate oxides, some method to remove the background leakage current component from the total measured current is necessary in order to obtain an accurate capacitance measurement. The 4155C and 4156C have a unique leakage current compensation function that removes this leakage current component. The background leakage current is measured both before and after the QSCV step voltage *cvoltage*, and this leakage current is subtracted from the current measured for the QSCV step voltage.

To enable the leakage current compensation, the LEAKAGE COMPENSATION field must be set to ON in the MEASURE: QSCV MEASURE SETUP page, as shown in Figure 13. In addition, on the same page you need to select an appropriate leakage current integration time in the LEAK field of the INTEG TIME section. Please note that once you have moved the marker into the LEAK field, you can use the rotary knob to increase or decrease the leakage current integration time, which is automatically rounded into the closest PLC multiple. In general, 16 PLCs is sufficient integration time for most QSCV measurements made in the 1 nA and 10 nA current ranges. For smaller current ranges, longer integration times may be necessary but the leakage compensation feature may not be necessary at all.

Figure 19 on page 12 shows a QSCV measurement made on a MOS device with a gate oxide slightly less than 40 angstroms. Sweeps were preformed with the leakage compensation turned on and off. As the figure shows, the leakage compensation feature is necessary to obtain a satisfactory measurement.

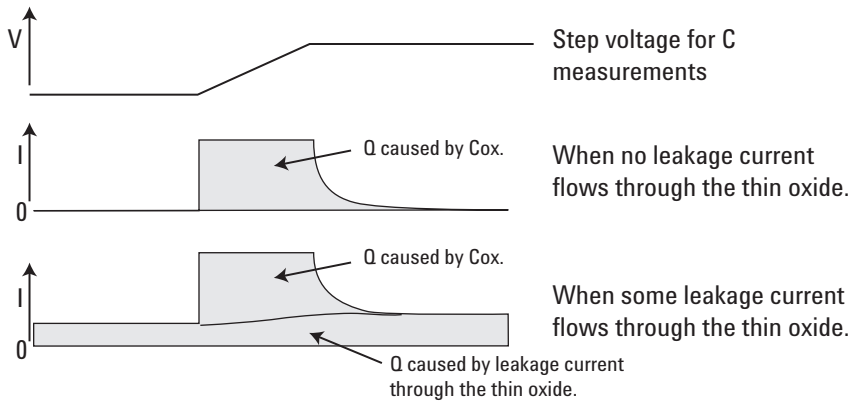

Figure 18. Simplified waveform for each capacitance measurement step

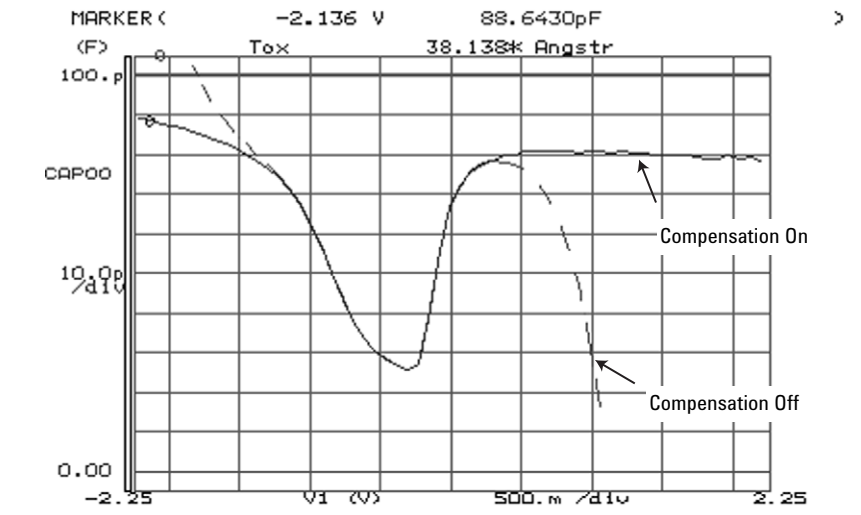

Figure 19. QSCV performed with leakage current compensation on and off

Comparison with the Linear Ramp Quasi-Static CV Method

The Agilent 4140B pA Meter / DC Voltage Source was the industry standard instrument for performing QSCV measurement (although this product is no longer sold). This was due to the 4140B's ability to create a high-quality linear analog ramp. This technique employs the following equation:

$$C = \frac{I}{dV/dt} \ [F]$$

Figure 20 shows a sample QSCV measurement sequence using the 4140B. The output voltage is changed with a constant rate (=dV/dt) to output a ramp waveform, and the current is measured at regular time intervals. The capacitance at each point can then be calculated using the above equation.

The aforementioned technique works well with thick oxide devices (>40 angstroms). However, it fails when the magnitude of the leakage current becomes a significant percentage of the capacitive current that you are trying to measure. Therefore, it is only possible to correlate the measurement results of the 4140B with those of the 4155C and 4156C on relatively thick oxide MOS devices.

To correlate QSCV measurements made on the 4140B with those made by the 4155C and 4156C, the same start, stop, and step voltages are used. The 4155C

and 4156C QSCV step voltage (*cvoltage*) is calculated by multiplying the 4140B ramp rate (dV/dt) by the 4140B integration time. The integration time of the 4155C and 4156C (*cinteg*) is set to the integration time of the 4140B. The 4155C and 4156C delay time is calculated as follows:

$$\text{delay time} = \frac{\text{step voltage} - \text{cvoltage}}{\text{dV/dt}}$$

The 4155C and 4156C leakage current compensation feature must be disabled.

Figure 21 shows the QSCV correlation of measurements made by the 4140B, 4155C and 4156C. The solid line shows the measurement results using a 4156C, and the dotted line shows the measurement results using the 4140B. The results are well correlated.

If you cannot obtain good correlation of the 4140B, the 4155C and 4156C measurement results, then the following are the most likely reasons:

- The 4140B ramp rate (dV/dt) is too steep.
- The 4155C or 4156C *delay time* or *cinteg* time is too short.
- The leakage current compensation feature on the 4155C/4156C is turned ON.
- You have specified the leakage current to be displayed, which causes the leakage current to be calculated even if the compensation is turned OFF.

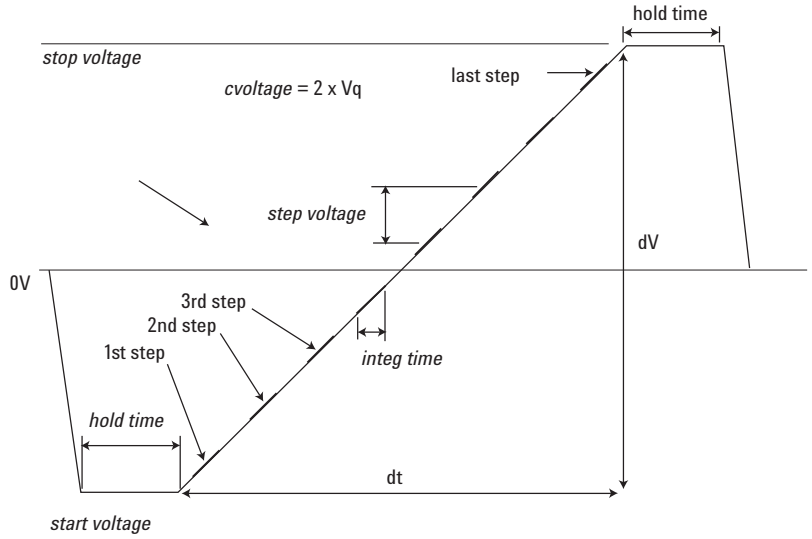

Figure 20. Classical QSCV measurement sequence with Agilent 4140B

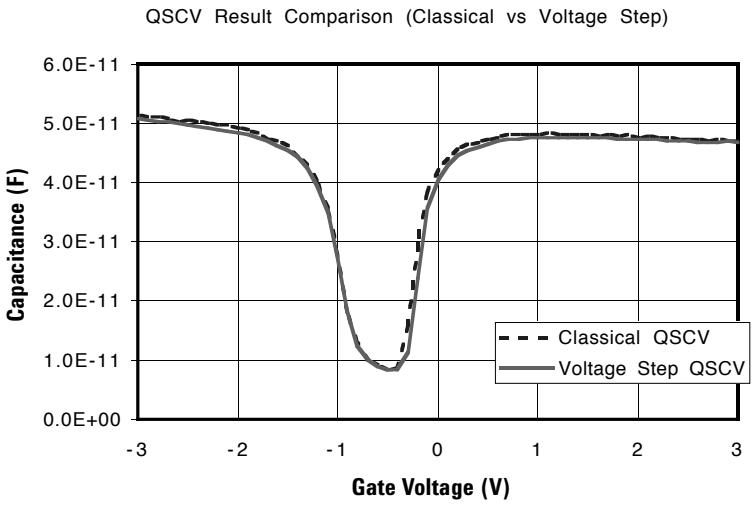

Figure 21. Correlation between classical and step voltage methods

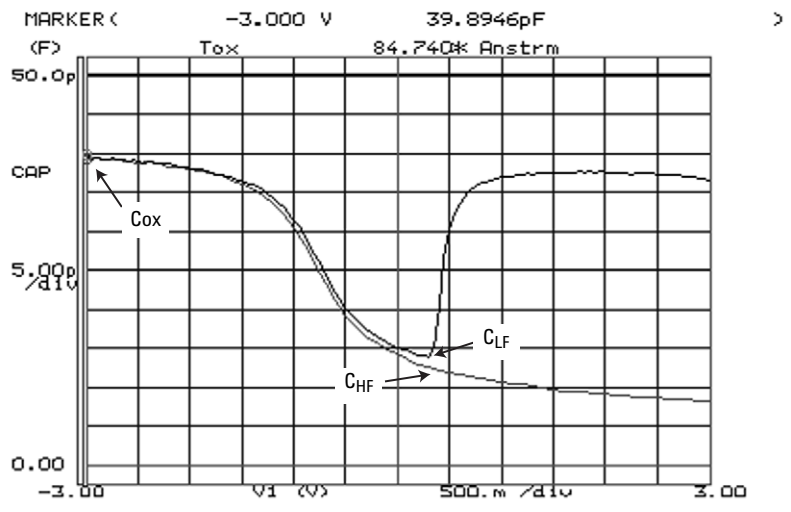

Figure 22. QSCV done on 4156C and HFCV done on 4284A

Comparing Quasi-Static and High-Frequency CV Data

The 4155C/4156C can be used in conjunction with the 4284A LCR meter and the E5250A low leakage switch to create a complete CV-IV measurement solution. The 4155C and 4156C allow you to control the E5250A switching matrix directly from the front panel. Moreover, Agilent can supply you with an IBASIC program that allows you to control the 4284A from the 4155/4156 and display resultant CV sweeps on the front panel of the instrument. This is actually the same IBASIC program that also does the semiconductor parameter analysis mentioned previously. Figure 22 shows the results of performing both a QSCV and HFCV (100KHz) sweep on a capacitor from the front panel of the 4156C.

A major benefit of combining QSCV and HFCV onto the same plot is that it enables the calculation of the surface state density, Nss. You can calculate Nss using the equation shown below:

$$Nss = \frac{C_{ss}}{A \cdot q}$$

$$= \frac{C_{ox}}{A \cdot q} \cdot \left(\frac{C_{LF}}{C_{OX} - C_{LF}} - \frac{C_{HF}}{C_{OX} - C_{HF}} \right) \quad [cm^2V]^{-1}$$

where

C_{SS} is the surface capacitance, in Farads;

C_{LF} is the minimum value of the quasi-static capacitance, in Farads;

C_{HF} is the high-frequency capacitance at the voltage corresponding to C_{LF}, in Farads;

C_{OX} is the accumulation oxide layer capacitance, in Farads;

q is the magnitude of electronic charge (1.602×10^{-19} Coulomb); and

A is the area of the capacitor, in cm^2

For the above curves the computed value of Nss is 2.55687×10^{10} $[cm^2\ V]^{-1}$.

Conclusion

The step voltage capacitance versus voltage (CV) measurement function furnished with the Agilent 4155C and 4156C enables you to obtain accurate quasi-static CV characteristics of MOS capacitors. Devices that cannot be measured using the linear ramp technique due to their thin oxides and resultant high leakage currents can be measured using the step voltage technique due to the leakage current compensation feature of the 4155C and 4156C. Where a comparison is possible, the measurement results correlate well with those obtained by the classical linear ramp QSCV measurement technique. You can also use the 4155C and 4156C to control the 4284A LCR meter, and display both QSCV and HFCV measurement results on the front panel of the 4155C and 4156C.

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