Errata

Document Title: Oscilloscope Measurements in Digital Systems (AN 223)

Part Number: 5952-2040

Revision Date: January 1974

HP References in this Application Note

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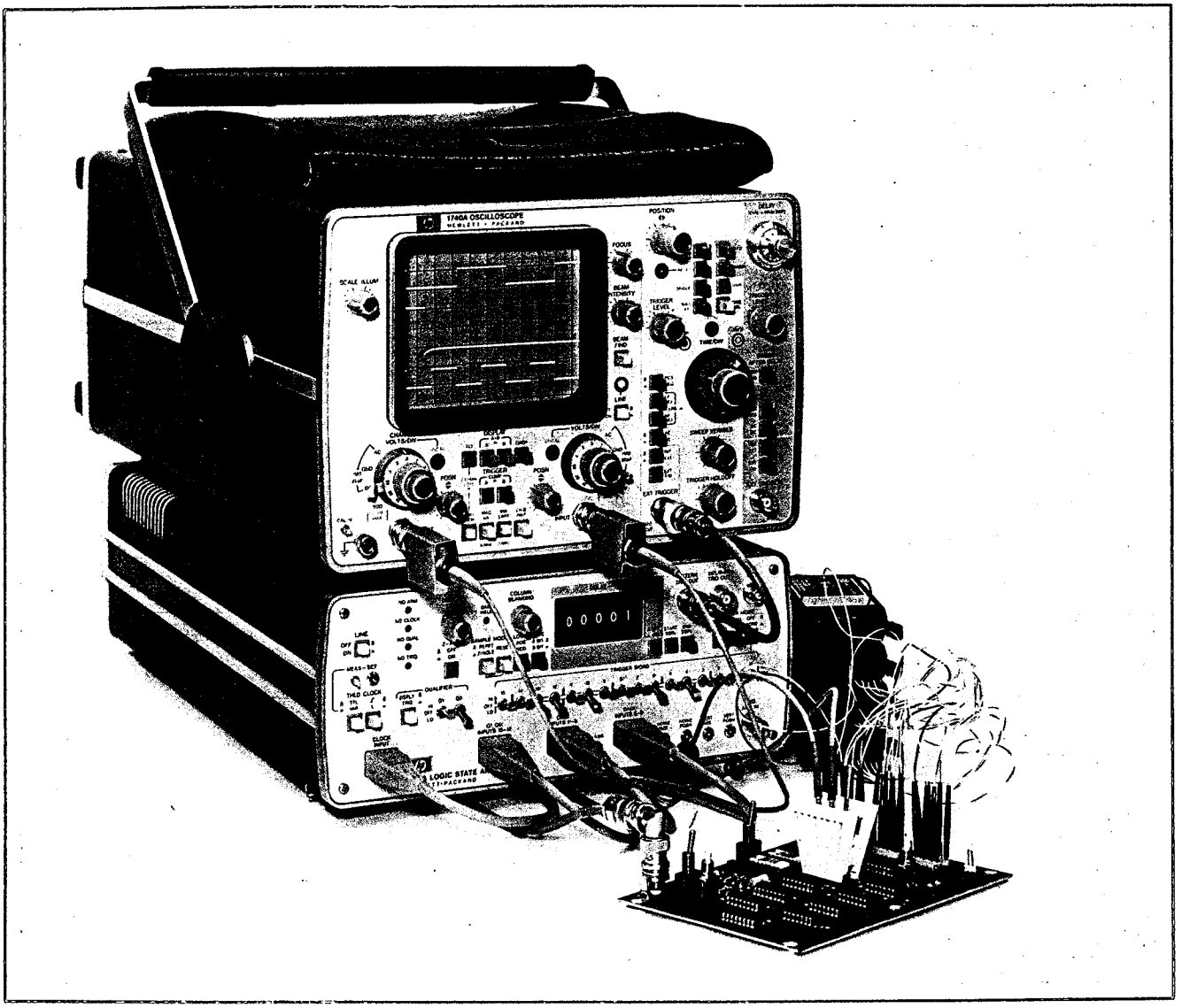
APPLICATION NOTE 223

OSCILLOSCOPE MEASUREMENTS IN DIGITAL SYSTEMS



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INTRODUCTION

The microprocessor has precipitated a rapid increase of digital systems with many new measurement problems not easily solved using only time domain analysis. Because digital designs are based on words or data on many lines that may require as many as 32 channels of simultaneous, parallel interrogation, it is best to use a Logic State Analyzer to define the problem location. After the functional problem is located, analysis of why an error occurred requires the use of an oscilloscope. By externally triggering the oscilloscope with the Logic State Analyzer trigger output pulse which is related to the time of the functional fault, it is easy to find the glitch, noise spike, timing problem, or unexpected level changes causing the problem.

Along with the microprocessor measurements, there is a need for speeding the troubleshooting of many discrete components such as those in control and input circuits. Checking the operation of three-port gates with a two-channel oscilloscope is time consuming. However, by using the HP Model 1740A or 1741A with its third channel trigger view, all three of the ports can be viewed simultaneously for a reduction in troubleshooting time.

Illustration is still the best method of explaining a measurement method. These examples consider some common problems which are often very difficult without suitable measurement capability. It should be easy to extrapolate from these examples the measurement methods that will quickly solve your particular application problem.

MICROPROCESSOR SYSTEMS

A microprocessor system usually operates at relatively fast clock speeds (1 to 10 μs) while its interaction with peripherals is usually at a very low speed (ms) or even single-shot. Therefore, measurement of these low speed signals can be enhanced by using a variable persistence storage oscilloscope for displaying the control and timing pulses of interest. Following are two examples of measurement problems that were easily solved using a Model 1600A Logic State Analyzer to trigger a Model 1741A Variable Persistence Storage Oscilloscope in a microprocessor based system.

TIMING MEASUREMENTS

The problem was to determine if a control pulse was followed by a control signal 20 μs after a key was pressed. The program dictated that key operation could not be recognized at a rate faster than once per second which made it necessary to use a storage oscilloscope in the single-shot or variable persistence mode. Furthermore, the signals were slow enough that the chop mode could be used to obtain the required timing resolution.

In setting up for the measurement, the 1600A Logic State Analyzer data probes were connected to the ROM address lines with the clock probe connected to a bit that occurred once per instruction cycle. The 1741A channels A and B were connected to the two output lines under test and the pattern trigger output of the 1600A was connected to the oscilloscope's external trigger input.

With the test setup complete, the Analyzer's trigger word was set to $0A17_{16}$ so that the desired section of the program would be accessed and trigger the 1741A at the proper time. A key was then pressed with both the program and timing signals captured at the same time. The state display in figure 1 shows

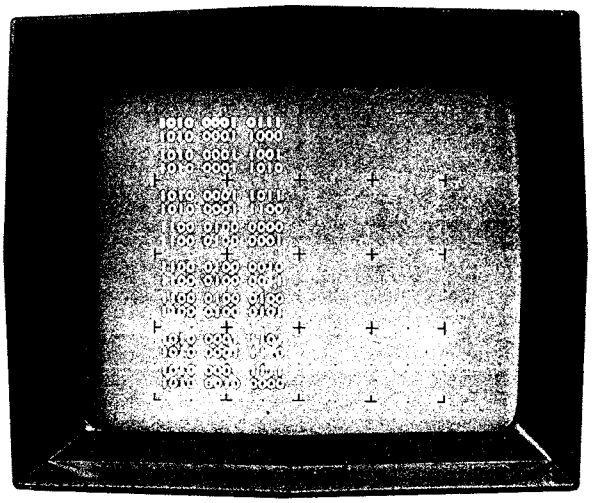


Figure 1. Logic Analyzer table display of program execution that generates a control pulse and control signals.

that the program execution follows the desired sequence from $0A17_{16}$ to $0A1C_{16}$ with a jump to $0C40_{16}$. Instruction $0A17_{16}$ to $0A1C_{16}$ generated the control pulse (top trace in figure 2) and instructions $0C40_{16}$ through $0C45_{16}$ generated the control signal (lower trace in figure 2). The oscilloscope measurement was straightforward with the display precisely showing the timing margin of 20 μs between the control pulse and control signal level change. Of equal importance, the quality of the signal transitions is also displayed.

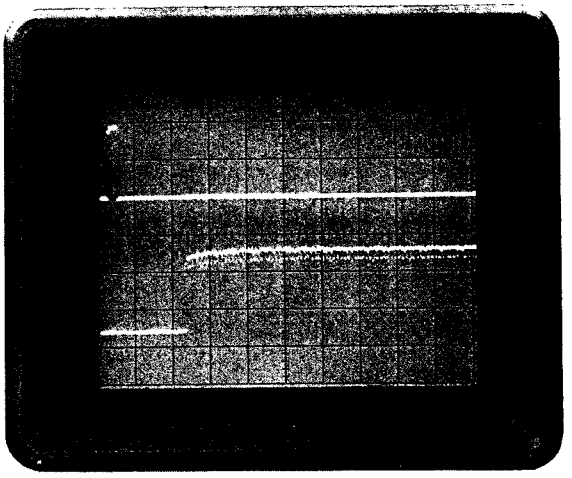


Figure 2. Single-shot, stored display of a control pulse and control signal showing 20 μs time interval. This display was externally triggered by a Logic State Analyzer at instruction $0A17_{16}$ as shown in figure 1.

CONTROL PULSE OPERATION

The problem in this example was that a measurement error occurred when an instrument's shift key was pressed. This measurement error could occur if seven pulses were not generated by the software when the shift key was pressed or could be caused by a hardware problem.

It was decided to check the program execution to determine if the write to output port instruction occurred. The Analyzer's trigger word was set to $0CF5_{16}$ which is the write to output port instruction in a loop that should occur seven times when the shift key is pressed. The test was initiated by pressing the shift key with the resulting table display in figure 3. By

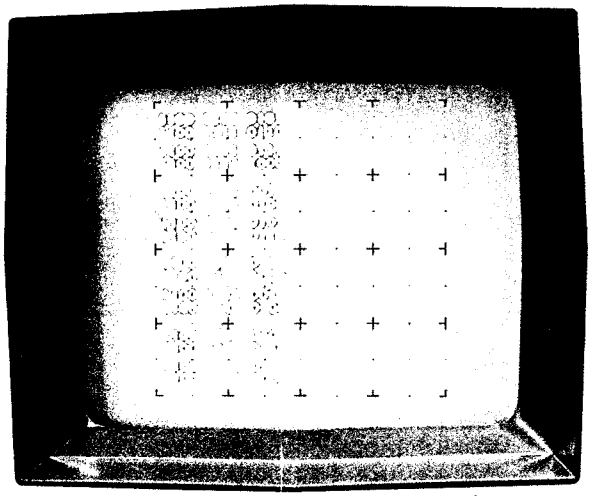


Figure 3. Logic State Analyzer table display of program execution that generates seven control pulses.

using the Analyzer's digital delay and running the test a few more times, it was determined that the program ran properly in that the write to output port instruction occurred seven times.

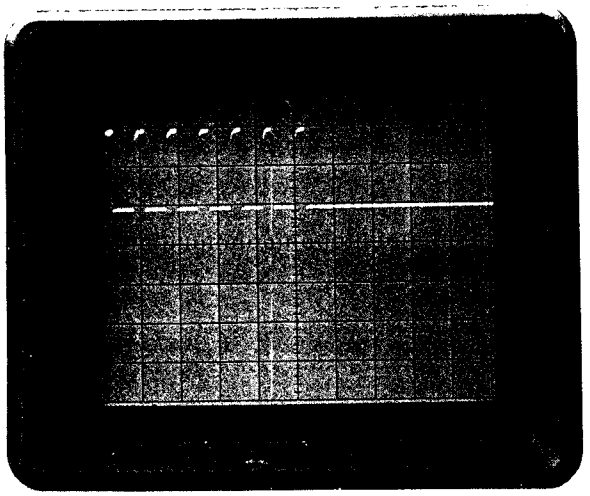


Figure 4. *Single-shot stored display of seven control pulses generated by a write to output port instruction. This display was externally triggered by a Logic State Analyzer at instruction* $0CF5_{16}$ *as shown in figure 3.*

Now the problem was to determine if the write to output port instruction was converted into seven pulses on the control line. To position the 1741A's measurement window to the proper point in time the oscilloscope was externally triggered using the Analyzer's pattern trigger output at $0CF5_{16}$. The shift key was pressed, to initiate the test, and the single-shot stored display of seven pulses in figure 4 was obtained.

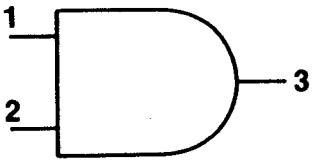
This indicated that there was a hardware problem in that the control pulses were not being read properly. After replacing the faulty component, the instrument's measurement was properly executed.

TROUBLESHOOTING GATES

A common troubleshooting problem in digital circuits is that many gates need to be checked. The major problem with gate measurements (whether they are AND, NAND, OR, etc.) is that two or more inputs and an output need to be monitored (figure 5). The usual

AND GATE

A

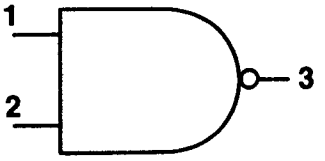


TRUTH TABLE

1	2	3
0	0	0
0	1	0
1	0	0
1	1	1

NAND GATE

B



TRUTH TABLE

1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5. Typical AND and NAND gates with their truth tables.

oscilloscope available for checking these gates is one having two channels which makes the required measurements time consuming. The Hewlett-Packard Models 1740A and 1741A Oscilloscopes can quickly solve this measurement problem with the third channel trigger view. However, in asynchronous or low speed systems the 1741A with variable persistence storage would be required. The trigger view mode can be considered to be a third channel because it displays (at center screen) the signal present at the external trigger input along with the vertical signals on Channels A and B.

To further reduce the problems of troubleshooting gates, miniature probes along with a special IC clip make it possible to connect to and monitor three

ports simultaneously. As shown in figure 6, the miniature probes fit in the HP Model 10024A IC clip and contact the IC leads and are held firmly in position, even on vertical boards.

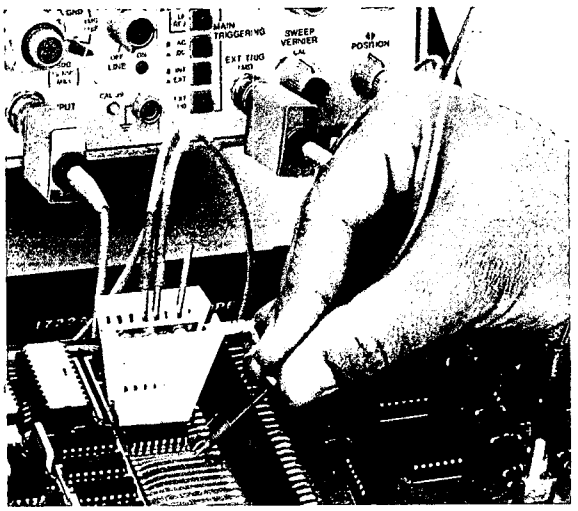


Figure 6. Monitoring signals on IC's is simplified with miniature probes and an IC clip which permit quick connection along with the convenience of being able to easily monitor more than one point at a t me.

APPLICATION

The problem that the third channel trigger view helped to solve was in the analysis of a circuit in which the periodic output contained a troublesome glitch. The output was supplied by an AND gate

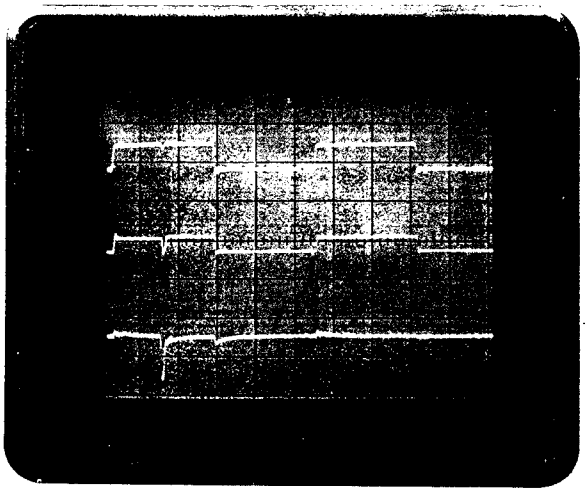


Figure 7. Waveforms on an AND gate's terminals showing a glitch condition on the output gate (center trace) as a result of a glitch on an enable line (lower trace).

(figure 5a), so the oscilloscope's vertical inputs were connected to the input lines with the external trigger input connected to the output. The resulting display, in figure 7, shows data on the top trace, the output on the center trace (trigger view), and an enable input on the bottom trace. With the time correlation between the three traces it is obvious that a glitch was being introduced on the enable line.

The enable signal was the output of a NAND gate (figure 5b) so the oscilloscope was connected to the gate's terminals. The resulting display (figure 8) shows the control inputs on the top and center traces and the output on the lower trace. Again, with the three trace time correlation, it was easy to see that a glitch was generated as a result of a race condition on the control lines. This led to the discovery that one of the control lines was connected to the wrong input signal.

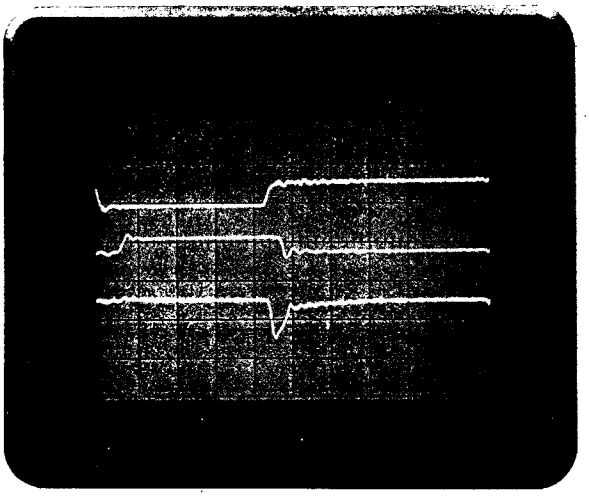


Figure 8. Waveforms on a NAND gate's terminals showing a glitch being generated on the output line (lower trace) which is caused by a race condition on its input lines (top and center traces). Third channel trigger view makes the display possible on a two-channel scope and provides time correlation between the signals.

CONCLUSION

The apparent simplicity of these measurements might tend to overshadow their significance. However, designers who have struggled to verify that output signals happen correctly as a result of program operation, will no doubt appreciate the value of these measurements. Furthermore, these mundane but often troublesome measurements should bring back to mind similar problems you have personally encountered and show the potential for saving time and/or increasing measurement capability with third channel trigger view, variable persistence/storage, and Logic State Analyzers.

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5952-2040
PRINTED IN U.S.A.