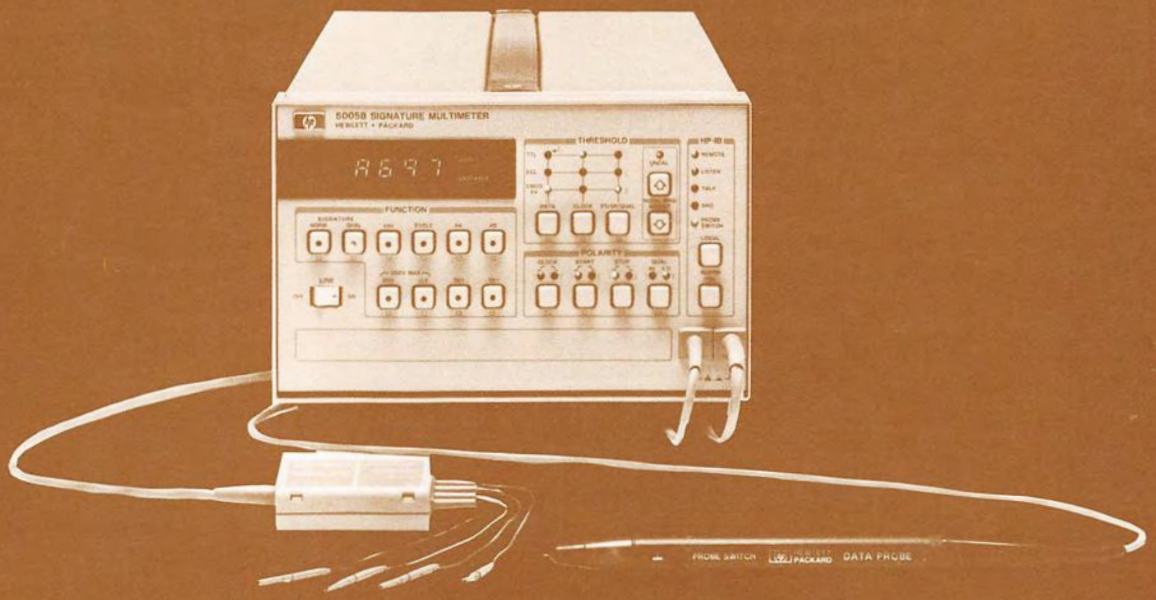
Application Note 222-12

A SIGNATURE ANALYSIS BASED TEST SYSTEM FOR ECL LOGIC



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FORWARD

ABOUT DIGITAL TROUBLESHOOTING

Microprocessors have revolutionized your product line. Your products are smarter, faster, friendlier and more competitive because they take advantage of μP-based control and computation. They are also harder to bulid, harder to test and harder to fix when they fail. Complex bus structures and timing relationships have practically obsoleted the scope/voltmeter signal tracing techniques so effective on analog products. The need to enhance the testability and serviceability of your digital products is acute. So is the need for specialized digital troubleshooting equipment.

ABOUT SIGNATURE ANALYSIS

To address these needs, Hewlett-Packard has developed the Signature Analysis technique, as well as a Signature Analyzer product line, for component-level troubleshooting of microprocessor-based products. A Signature analyzer detects and displays the unique digital signatures associated with the data nodes in a circuit under test. By comparing these actual signatures to the correct ones, a troubleshooter can back-trace to a faulty node. By designing or retrofitting S.A. into digital products, a manufacturer can provide manufacturing test and field service procedures for component-level repair, without dependence on expensive board-exchange programs.

ABOUT THIS CASE STUDY SERIES

Use of a Signature Analyzer requires that some test features be designed or retrofit into the product to be tested. This application note is one in a series of case studies aimed at assisting designers, test engineers, and others in understanding these features so that they can easily add Signature Analysis to their product. These case studies show detailed examples of these features in various digital systems based on specific microprocessors.

ABOUT THIS PUBLICATION

This is a reprint of a technical article from the Hewlett-Packard Journal. It describes how Signature Analysis testing was implemented in various circuit assemblies of the Hewlett-Packard series 64 computer. Testing the high performance ECL circuitry in the HP 3000 series 64 demanded a technique capable of monitoring signal activity at clock rates up to 25 MHz. The HP 5005B Signature Multimeter was choosen for its ability, through Signature Analysis, to provide functional GO/NO GO testing at these clock rates. This article discusses the HP 5005B implementation, the method of generating test vectors, how backtracing to component level faults was accomplished, and the resulting test reports. It is intended to share the thoughts and philosophy used in a successful application of automated Signature Analysis testing and troubleshooting.

ABOUT OTHER PUBLICATIONS

Application Note 222-0, "An Index to Signature Analysis Publications" lists all other application notes currently available in the AN 222 series about Signature Analysis. They cover a wide range of interests, from how to design or retrofit Signature Analysis into digital systems, to the cost reductions that can be expected in production test and field service by doing so. It also lists all data sheets for the complete line of Hewlett-Packard Signature Analysis products, plus other related publications about digital troubleshooting.

A Signature Analysis Based Test System for ECL Logic

by Edward R. Holland and James L. Robertson

TESTING OF LOADED PRINTED CIRCUIT BOARD assemblies is vital in the production of any computer system. For effective testing of HP 3000 Series 64 boards, a special tester was designed. This system, the Gemini Universal ECL Signature Test system, or GUEST, is able to capitalize on the HP 5005B Signature Multimeter[1] and the built-in shift string organization of the flip-flops on the boards under test (see article, page 11).

Since all ECL networks in the Series 64 must be terminated in their characteristic impedances to suppress reflections, a tester running at slow clock speeds, as most board testers do, would not detect termination and other timing problems. A tester that functions at real-time clock rates was required and the GUEST system meets that need, being able to operate at clock rates up to 25 MHz.

In board testing, a test vector is a set of input states applied by a tester to a unit being tested. Generation of test vectors for a given unit under test (UUT) is often a difficult and time-consuming operation. In the GUEST system, vectors are generated algorithmically in real time by hardware. Therefore, preparation of test programs is reduced from weeks or months to a few hours. This has made the GUEST test system a useful tool throughout the prototype design process of the Series 64. By contrast, most test systems are usable only after the design is complete and all the test vectors have been generated, a point that is reached typically very late in a project.

Computer-Driven Test System

The GUEST test system is interfaced to the controlling HP 1000 Computer though the HP-IB (IEEE 488) interface bus (see Fig. 1). The primary functions of the computer system are to initiate testing and to guide the operator in probing of a defective UUT. One computer is able to handle up to six GUEST test stations, or a combination of GUEST test stations and DTS-70[2] test stations with all stations active at the same time.

The GUEST test system is interfaced to the UUT by a personality board as shown in Fig. 2. Building the personality board for ECL boards requires simply loading wire jumpers on a universal board. There is one set of jumpers for UUT input pins and another set of jumpers for pins that require terminations.

Hardware Test Vector Generation

The test vectors used in the GUEST system are generated as a serial bit stream by a 13-bit linear feedback shift register, which produces an 8191-bit-long pseudorandom sequence (see Fig. 2). This bit stream is shifted though a 588-stage shift register on the GUEST board and then via the personality board through the shift string of the UUT. Shifting continues for 1023 clock cycles. Then on the 1024th clock cycle, all of the shift register elements on both the GUEST board and the UUT are parallel-loaded under control of the diagnostic control unit shift line. The next 1023 clock cycles then cause the data loaded in the parallel operation to be shifted out of the combined registers past the GO/NOGO point. The test runs for a total of 8,379,393 (8191×1023) shifting clock cycles so that each of the inputs to the board is driven by all of the 8191 bits of the

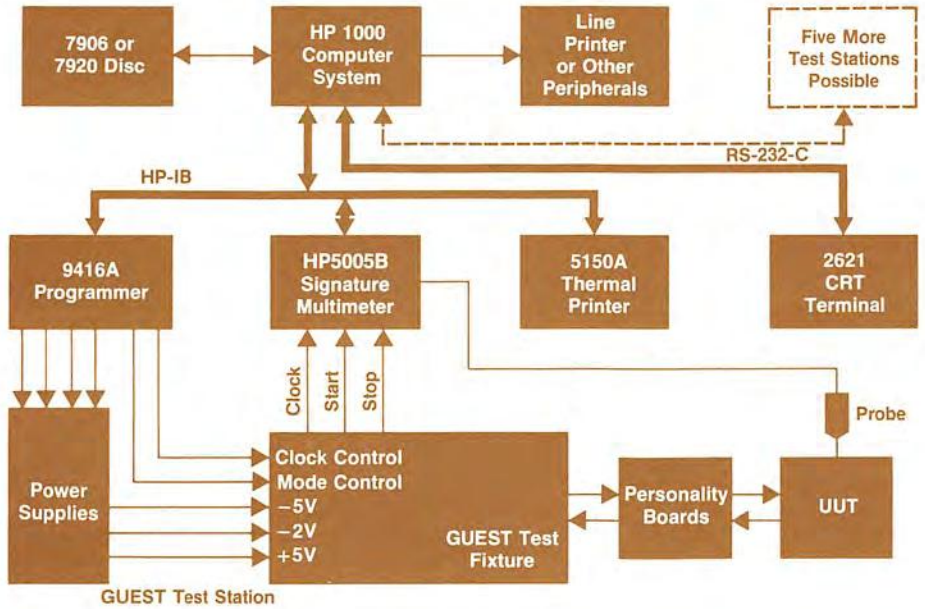

Fig. 1. *GUEST is interfaced to the controlling HP 1000 via the HP-IB (IEEE 488), and to the unit under test by a personality board.*

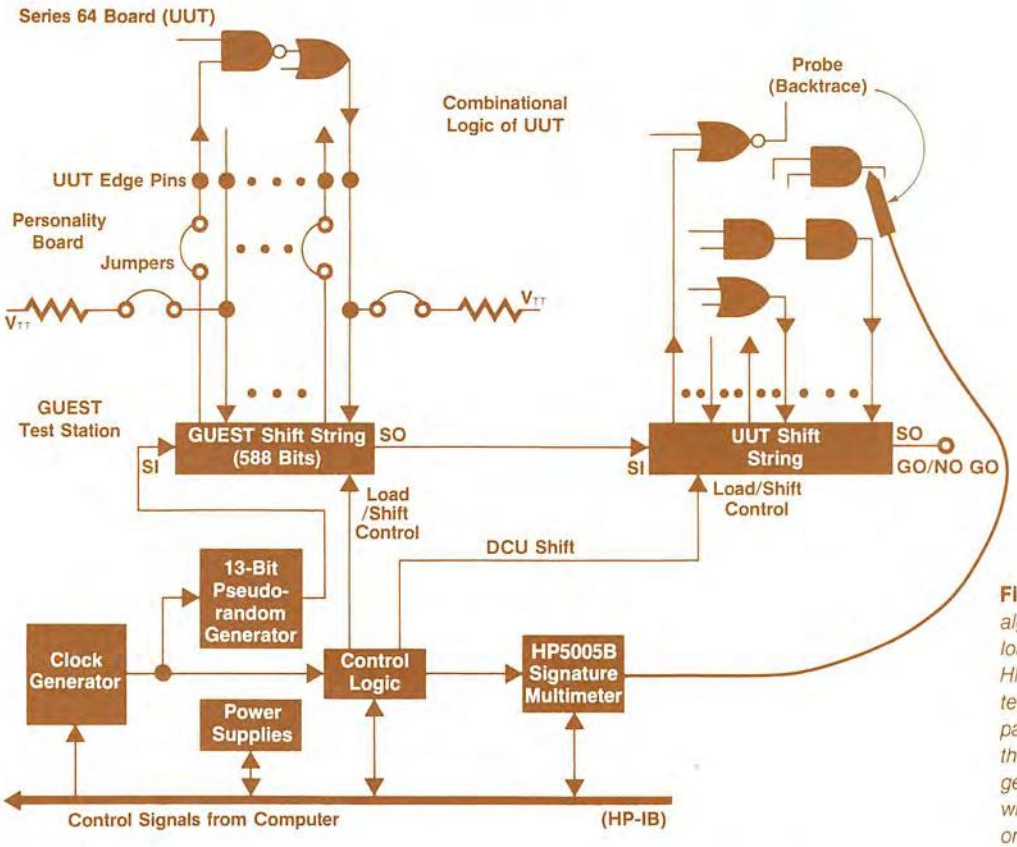

Fig. 2. *Test vectors are generated algorithmically by GUEST and loaded into the shift string of the HP 3000 Series 64 board being tested. The data is then shifted past the GO/NOGO point, where the 5005B Signature Multimeter generates a signature that tells whether or not a problem exists on the board.*

pseudorandom sequence and each output of every shift string flip-flop on the board is also driven by all 8191 bits.

Go/No-Go Testing

As the data stored in the shift registers on the 1024th clock cycle is shifted out past the GO/NOGO test point, the HP 5005B Signature Multimeter computes the signature of the data stream and the computer checks this signature against the expected signature stored for the board type being tested. Since both the GUEST and the UUT shift registers are shifted past this test point, any incorrect value from any part of the UUT causes an incorrect GO/NOGO signature. If the board passes the GO/NOGO test it is ready for installation in a system. If the board fails this test, additional testing is done on the GUEST tester.

The control logic of the GUEST tester can limit the signature analyzer to only the last N data outputs of the shift string, where N is specified by the computer. When N is the maximum value, the signature analyzer clock is always enabled and the signature depends on all bits in the shifted outputs. As N is decreased, fewer and fewer outputs enter into the signature. At some value N=n the signature will be incorrect, while at N=n−1 the signature will be found to equal the expected value. Since there is a one-for-one mapping of the value of N and a point in the overall shift string, it is possible to pinpoint the fault to an I/O pin or an input to a shift string bit on the UUT. The computer is programmed to use a binary search algorithm and takes ten signatures or less to find the correct point in the shift string to begin further backtracing.

Backtracing

While backtracing faults to the component level, the signature at each node is dependent only on combinational functions of the pseudorandom test vectors applied to the UUT input pins and shifted into the internal shift register states of the UUT. The signatures are measured by moving the signature analyzer probe to each node as guided by the computer.

Backtracing starts at the node determined by the GO/NOGO binary search. When a node is found that has an incorrect signature but all inputs affecting that node have correct signatures, the faulty node has been isolated.

Feedback Loops

To make effective use of signature analysis, all feedback loops should be broken. If a feedback loop is not broken, a bad signature anywhere in the loop causes all other nodes in the loop to have bad signatures, and fault isolation to the component level is impossible. Feedback loops are broken during backtracing by the internal UUT shift registers. This is accomplished by clocking the signature analyzer when the outputs of each shift register are dependent only on its serial input and not on its parallel data inputs. Since bad signatures cannot propagate through these shift registers, any feedback path from an output to a parallel data input is broken.

Clock and Shift Control Faults

Another complication in the fault isolation process is that of diagnosing faults in the clock and shift control circuits of the UUT. Since data in these areas is normally synchronous

Designing for Testability with GUEST

by Karen L. Meinert

The HP 3000 Series 64 and the GUEST system were designed at the same time to work together. It was discovered that certain design issues had to be considered when designing a Series 64 printed circuit assembly (PCA) if maximum GUEST testability was to be achieved.

High Fan-in

Fan-in is defined as the number of inputs to a circuit that is needed to produce an output. Because GUEST outputs only 8191 predefined test vectors, a fan-in of 14 or greater makes it impossible to sequence through all combinations (2^{14} is greater than 8191). If the fan-in is less than 10 it is safe to assume that all combinations will appear in the test sequence. Modifications to the board or the personality board can be made to assure that all combinations are tried when the fan-in is between 11 and 13. There are also several signals (mostly high, mostly low, pulse high, pulse low) available on the personality board; these can be used to drive inputs to increase a circuit's effective test vectors.

It is important that the 13 inputs to a high-fan-in circuit be driven by contiguous bits from GUEST. The bits in the shift string and on the edge connectors of GUEST are just shifted versions of the 13 bits that guarantee the 8191 test vectors. If 13 bits are selected at random, there is no guarantee that all 8191 combinations will appear.

Feedback Loops and Shift Strings

For a PCA to be GUEST-testable it is not necessary that it have shift strings (see article, page 11). The shift strings are an effective means to break up feedback loops and initialize memory elements. If no feedback loops exist on a board and memory can be initialized, there is no need for shift strings.

Nonstandard Clocking

Both the GUEST shift register and the signature analyzer are clocked on the standard system clock. If other phases or edges of the clock are used, testing problems may occur. Feedback loops are not necessarily broken if shift string registers are clocked on phases other than that used by GUEST. Also, there could be problems in getting information between the PCA and the GUEST system in time if other phases are used. In general, clocks other than the standard system clock should be avoided when designing PCAs to be tested by GUEST.

Non-ECL Circuitry

GUEST was designed to be an ECL circuit tester. To test circuits other than ECL, translator packs are used on special personality boards that adapt each tested board to GUEST. In addition, three-state buses should not be allowed to float to the high-impedance state or unstable signatures will result. The solution is to have GUEST drive the bus whenever the board is not. This is accomplished by bringing the three-state bus enable signal to an unused I/O pin on the PCA. This signal is inverted and used on the personality board to enable the translator direction (ECL to TTL or vice versa).

TTL signals can be probed by the HP 5005B Signature Multimeter, since this analyzer is capable of changing its input voltage threshold to allow for non-ECL signals. This can be done either manually or under automatic control through the HP-IB interface.

RAMs

To test a RAM completely each location must be addressed five times: once each to write one, write zero, read one, read zero, and deselect. Since GUEST outputs a total of only 8191 test vectors, RAMs larger than 1024 bits deep cannot be tested completely. To obtain known signatures on the outputs of RAMs, any location that is read must first have been written. If a location is read that has not been written, the read data is whatever was in the RAM at power-up. This is random data and therefore has a random signature. A signal called RAMINIT (RAM INITialize) is generated by GUEST to assure that all read locations are initialized. GUEST generates a pseudorandom number sequence with a length equal to half of a signature analyzer cycle. This sequence is repeated during the second half of the cycle. RAMINIT is high for the first half-cycle and low for the second half-cycle during the time that the RAMs can be read or written into. RAMINIT is used in the write enable circuitry to force a write when high and to enable reads and writes when low. In this way every location that is addressed in the first half is written with known data. When these addresses repeat themselves in the second half (they are part of the repeated pseudorandom sequence), where reads may occur the locations have been initialized, and known, repeatable signatures will occur.

Karen L. Meinert

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with the signature analyzer clock, only SA0 and SA1 (stuck at 0 and stuck at 1) signatures would be found and normal backtracing would be impossible. To isolate this type of fault, the first backtrace signature measured after the GO/NOGO test fails is at the GO/NOGO test point. A correct signature here indicates that the UUT clock and shift control circuits are functioning. If the test fails, the shift register serial outputs are probed using a binary search algorithm until a good signature is found and the following device's serial output is bad. Clock and shift control inputs to this earliest failing shift register are probed while pseudorandom data is applied to the clock and shift inputs of the UUT. If no bad inputs are found, the shift register is suspected to be bad. If a clock or shift control input fails, backtracing starts at that point, with pseudorandom data still applied to the clock and shift inputs of the UUT, and continues until the failing node is isolated.

Test Report

When the faulty node has been isolated, three additional measurements are made on the suspected node. They are: +

peak voltage, − peak voltage, and resistance to ground. A test report with information pertinent to the failing node is then printed. The failure descriptions can be: NODE MOVES, NODE STUCK, NODE UNSTABLE, or OPEN TRACE. The information on the test report can be used to further diagnose the fault (shorted nodes, open terminations, etc.).

Two assumptions made so far are that the probe has made good contact with the node being tested, and that the operator probes the correct point when prompted. This is not always the case, so provisions have been made for recovery from probing contact errors. To minimize operator misprobes, all pertinent IC pins are probed in sorted ascending order before moving on to the next IC. Thus, pin-to-pin and IC-to-IC movement is minimized. Each node is probed at least twice in different locations to diagnose misprobes or open traces. If a misprobe is discovered before it is diagnosed by the computer, the operator can ask to reprobe the point where the error was made.

Edge connector pins, resistor pins, or any other point that is difficult to locate or probe can be declared inaccessible. During backtrace, the operator will not be prompted to probe these points. When the test report is printed, any inaccessible point that could have caused the fault is listed as not checked.

Creating the Test File

Before using GUEST, a UUT test file must be created by TESTAID.[3] To use TESTAID, topology information (a description of the types and interconnections of all integrated circuits on the UUT) must be supplied by the test programmer. This data is available from the computer routing and placement program used in the design of Series 64 boards, and is converted by a utility program to the format required by TESTAID. No other input data is required for TESTAID simulation because all test vectors are generated by the GUEST hardware.

After the preliminary test file has been created by TESTAID, UUT-dependent test setup parameters need to be added (clock period, reference voltages, special node definitions, etc.). Signatures can then be added as measured from a known good UUT. The addition of all GO/NOGO signatures is automatic and requires approximately two hours run time. Backtrace signatures are added by manually probing each internal node as guided sequentially by the computer. This process also requires approximately two hours.

Once generated, the UUT test file should be verified for accuracy of fault isolation and fault coverage. Fault isolation accuracy can be verified by inserting a few known faults in critical areas of the UUT and determining whether they are diagnosed correctly. Fault coverage is verified by measuring the GO/NOGO signature repeatedly while probing internal nodes, as guided by the computer, with a special probe that forces each node both high and low. If the GO/NOGO test passes, the stuck at 1 or stuck at 0 node fault is marked as not detected. When probing is complete, the fault detection percentage is computed and saved in the UUT test file. Typical fault coverage is in the order of 99% for ECL boards.

The final step to be done when creating a test file is documentation. By entering the DOCALL command, complete documentation of the UUT test file (all node drivers, receivers, terminations, special setup, signatures, etc.) can be listed on the line printer.

Acknowledgments

The authors would like to acknowledge the creative work of Bob Horst and Rick Amerson for proposing and designing the early GUEST test system. Credit should go to Jim Tseng, Harish Joshi, and Bob Cook for the final translation of the hardware into a reliable and highly usable system. Mike Phillips deserves much credit for working out bugs in the process of personality board design and a lot of helpful feedback in the programming process. John Shing and Gary Gitzen deserve thanks for their helpfulness in making available a 5005B Signature Multimeter for use in the GUEST system.

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James L. Robertson

Jim Robertson joined HP in 1958 with previous experience as an avionics test engineer. He has been a standards lab manager and a pretest supervisor, and now works in electronic tooling. Jim is a native of Los Angeles, California and received the AS degree in electrical engineering from Foothill College, California in 1968. He is married, has two sons and two married daughters, and enjoys camping, hiking, and travel. He lives in Los Altos, California.

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Ed Holland was born in Detroit, Michigan and attended Michigan State University where he earned the BS degree in electrical engineering. After service in the U.S. Naval Reserve and work on radar and test system design, Ed continued his education at Stanford University, earning an MS degree in electrical engineering in 1960. He joined HP in 1961 and has contributed to a number of products that include the 3440, 3460, and 3462 Voltmeters, the 2114, 2115, and 2116 Computers, and HP 3000 Computers. Currently, Ed is project manager for the Series 64 CPU, cache memory, and GUEST tester hardware. He is the author of a paper on computer I/O and peripherals and is named inventor on a patent related to the basic A-to-D conversion concept used in the 3460 DVM. Ed is a member of the IEEE and the Planetary Society. He lives in Palo Alto, California, is married, and has two children. He enjoys backpacking, bicycling and sailing and works at promoting space exploration and the search for extraterrestial intelligence.

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