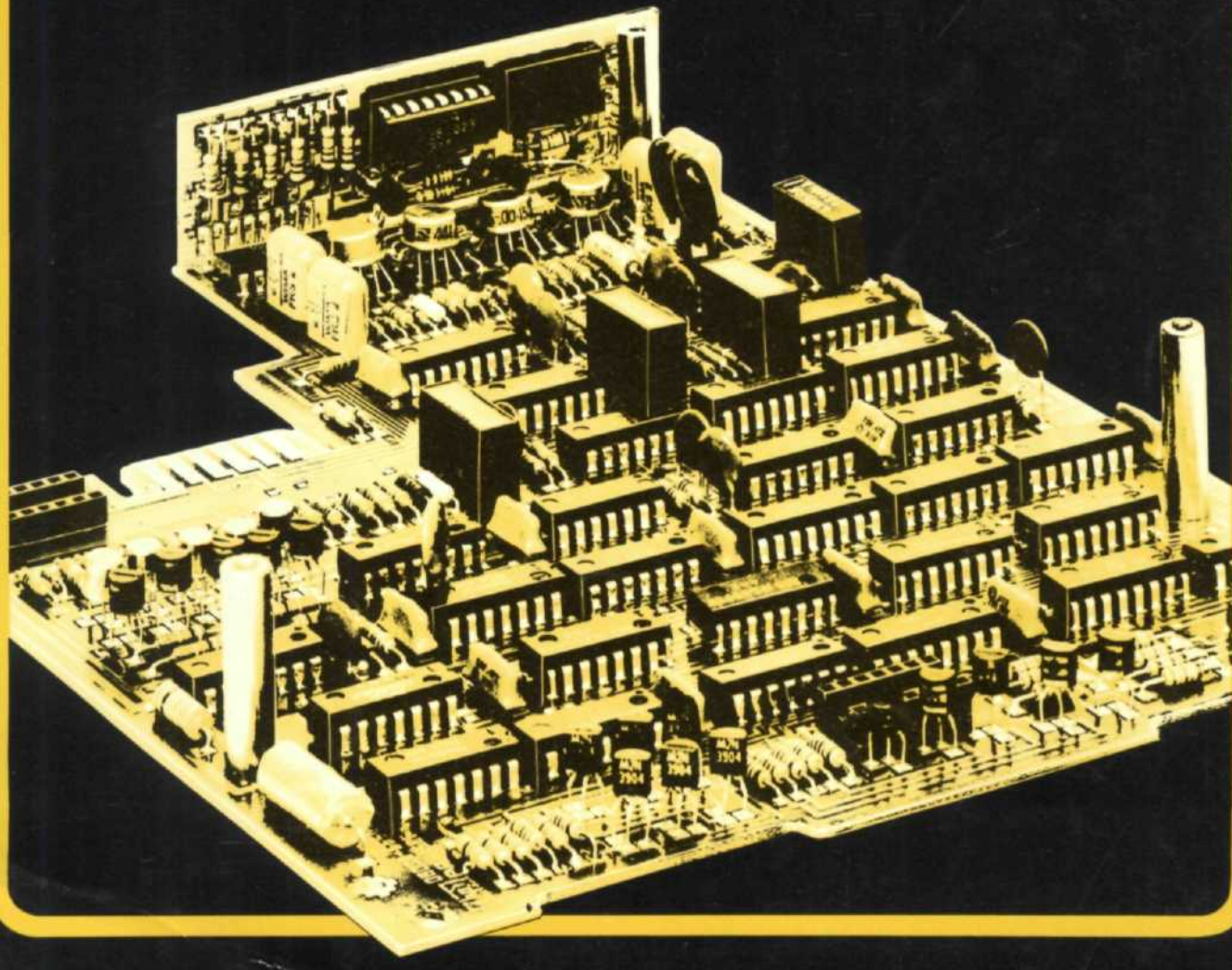
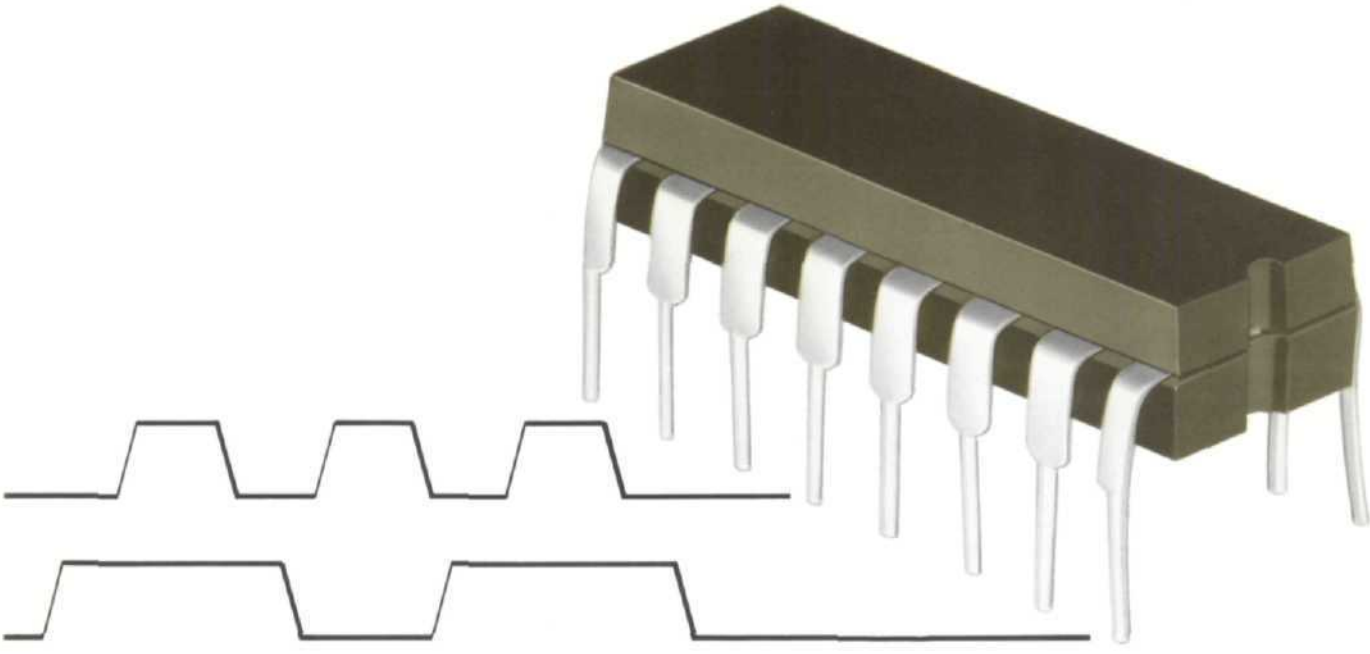
Application Note 195

# PULSE GENERATOR TECHNIQUES IN CMOS APPLICATIONS





# CONTENTS

# PULSE GENERATOR TECHNIQUES IN CMOS APPLICATIONS

## INTRODUCTION

Since its introduction at the end of the 1960's, MOS integrated circuit technology has penetrated a wide variety of application areas. One variant of MOS technology, called CMOS (or COS/MOS) logic, is rapidly gaining in popularity and has created a need for test equipment with new capabilities. A specific need is for stimulus instrumentation with which CMOS devices can be exercised in order to evaluate their performance. This application note will describe new pulse generator techniques for making the necessary measurements, as well as provide an explanation of the tests themselves and a brief introduction to CMOS technology.

### What is MOS?

The initials MOS (Metal Oxide Semiconductor) today describe any enhancement mode (a device which is normally off with no bias and has to be turned on or enhanced to cause current flow through it), insulated gate, field effect transitor. Because of its features (some unique) such as low power dissipation and low packing density, MOS is one of the major technologies for Large Scale Integration (LSI) along with ECL and TTL. The different types of MOS devices are described as follows.

### PMOS and NMOS devices

As mentioned above, the basis for all MOS devices is the enhancement mode Field Effect Transistor. FET devices were originally fabricated using an N-type substrate with two diffused regions of P-type material, the source and drain. A metallized layer separated from the substrate by a diffused layer of silicon dioxide formed the gate or control element. Figure 1 shows a cross-section of the P-channel device structure and its schematic symbol.

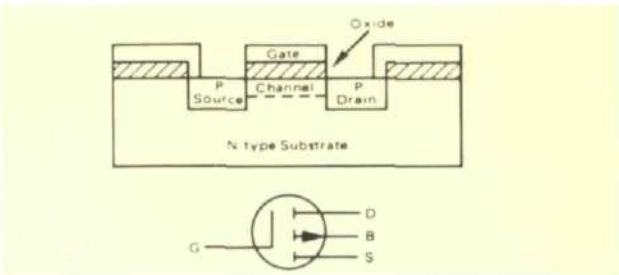



Figure 1. P-Channel Transistor (PMOS)

A voltage applied to the gate establishes a path, the channel, for hole conduction between the source and drain. Similarly, using a P-type substrate with N-type source and drain results in an NMOS transistor utilizing electron conduction after gate turn-on. Figure 2 is a cross-section of an N-channel element and the schematic symbol. Either of these FET devices can be integrated to form logic circuitry.

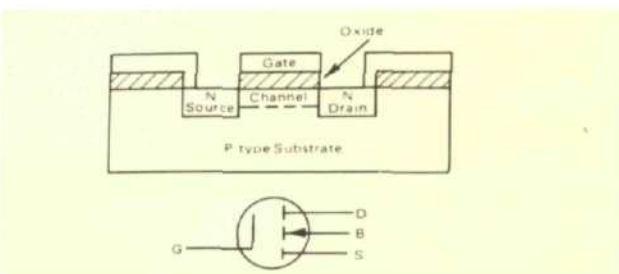



Figure 2. N-Channel Transistor (NMOS)

# CMOS devices

With the development of CMOS (or Complementary MOS), a new and very advantageous form of MOS became available to the system designer. The benefits of CMOS logic are many: low power dissipation at medium speeds, wide range of power supply voltages (3–16V), high noise immunity, high packing density, and high fan-out capability. These advantages are today offered in IC's encompassing a wide variety of basic and complex logic functions. They offer the designer complete system design freedom.

This third type of MOS integrates both N-channel and P-channel transistors in the same logic circuits. As shown in Figure 3 a complementary inverter may be formed by applying the input signal to the gates of two opposite polarity transistors.

In this circuit a low input signal means the N-channel transistor (Q1) is OFF and the P-channel device is ON. The output is shorted to the positive supply, but virtually no load current is drawn if a similar high impedance MOS gate input is used as the load. When the input signal goes high, Q1 is turned ON and Q2 is turned OFF. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the CMOS circuit occurs only during the brief transition period between logic states.

Careful device design for rapid turn-on and turn-off results in a power dissipation as low as 2 nW per gate. The high noise immunity inherent in CMOS logic is also a direct result of the complementary configuration because two separate thresholds must be crossed. The threshold region also varies directly with the power supply voltage and has its center located at typically 45% of the supply voltage.

The operating speed of CMOS circuits is at present limited to about 15 MHz. This is due to the relatively high parasitic capacitance of the silicon substrate. CMOS circuits using a sapphire substrate (called SOS/CMOS logic) are now in development which have substantially higher operating speeds because of reduced parasitic capacitances.

The three major advantages made available by CMOS technology can be summarized as follows:

- very low power dissipation
- wide power supply voltage operating range
- high noise immunity.

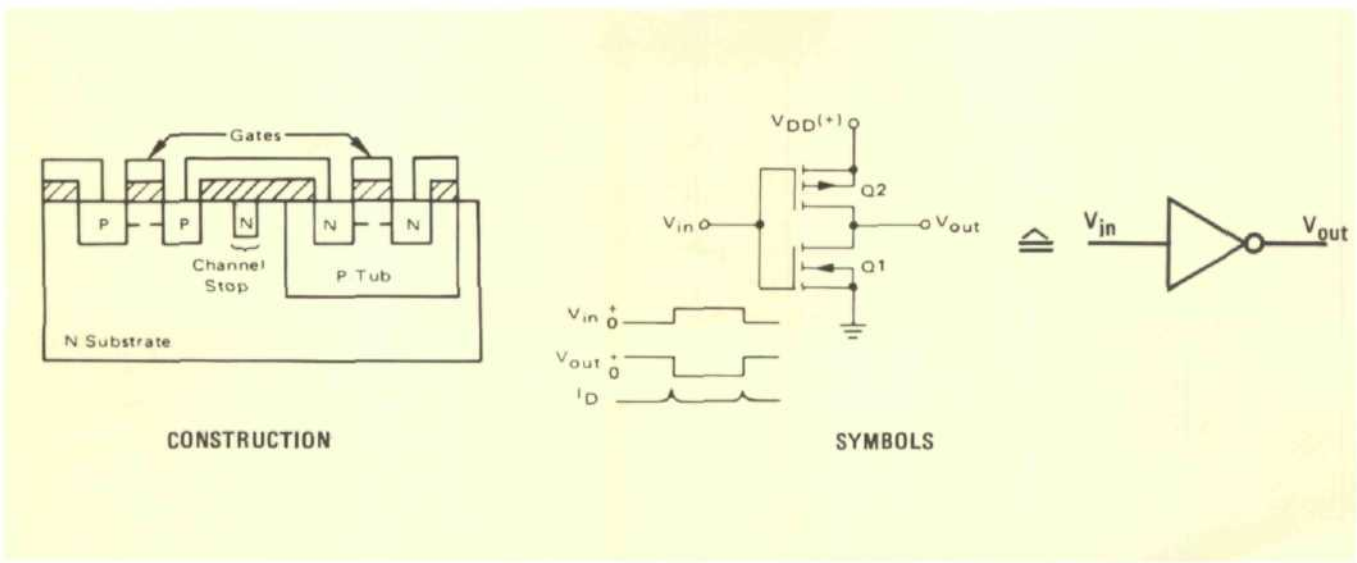



Figure 3. Typical CMOS inverter

# CMOS TEST REQUIREMENTS

Test requirements for CMOS digital devices are of two different types: functional tests and parametric tests.

Functional testing is performed to determine if the CMOS device or circuit is working on a digital (i.e., 1's and 0's) basis. Does the device correctly process digital input signals to produce its expected output signals? Does it perform according to its truthtable? Functional testing is, for example, a design engineer's first concern when turning-on and troubleshooting a new circuit design.

Parametric testing is concerned with measuring device performance in terms of nanoseconds, volts, and *milliamperes. Data sheet specified parameters such as* propagation delays, setup times, leakage current, and output voltages are typical examples of device attributes that must be measured and compared against standard values. Such testing is typically performed by IC designers and manufacturers and is often also required in incoming inspection of purchased devices.

CMOS adds an additional level of complexity to parametric testing. As the power supply voltage is varied through its allowable 3 – 16 volt range, device parameters also vary considerably. Figure 4 shows two representative characteristic curves which indicate the variations in device performance which can typically be expected. The result is that it is often necessary to perform parametric tests at several different power supply settings or even over a range of voltages.

## CMOS device parameters

The following are a selection of the most important parameters that need to be measured when performing parametric tests on CMOS devices.

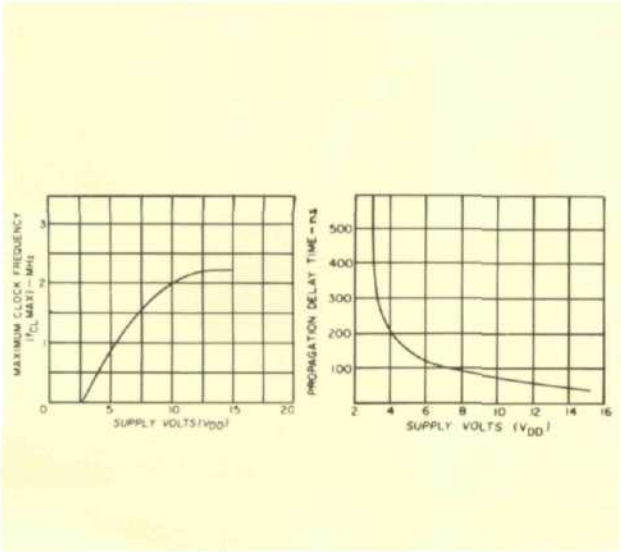



Figure 4. Influence of supply voltage variations on device parameters

## Input Voltage

The CMOS input structure requires that the signal input voltage ($V_{in}$) be limited to values between the upper and lower power supply voltages, respectively $V_{DD}$ and $V_{SS}$ (or system common). If the signal is ever greater than $V_{DD}$, the device input protection diodes become forward biased and the resulting high input current destroys the IC.

## Operating Speed

The operating speed of a logic system depends upon signal propagation delays and output rise and fall times. In the CMOS logic family these parameters are functions of output load capacitance, operating voltage, and the device temperature.

## Propagation Delays

Propagation delay pairs, $t_{PLH}$ and $t_{PHL}$ are usually specified on all data sheets. $t_{PLH}$ is the time required for a signal to propagate through the device and raise the output node with its associated capacitance from a low to high level. $t_{PHL}$ is the delay through the same path but for an output change of logic high to low. For non-synchronous circuits, the delay is measured from the input signal edge to the resulting output signal edge (50% points). For synchronous circuits, which have a clock signal, the delay is measured from the active clock edge to the resulting edge on the output signal (again, 50% points).

An increase in load capacitance lengthens the transition time which increase the propagation delay. Propagation delay also increases with temperature. An increase in the supply voltage reduces propagation delay.

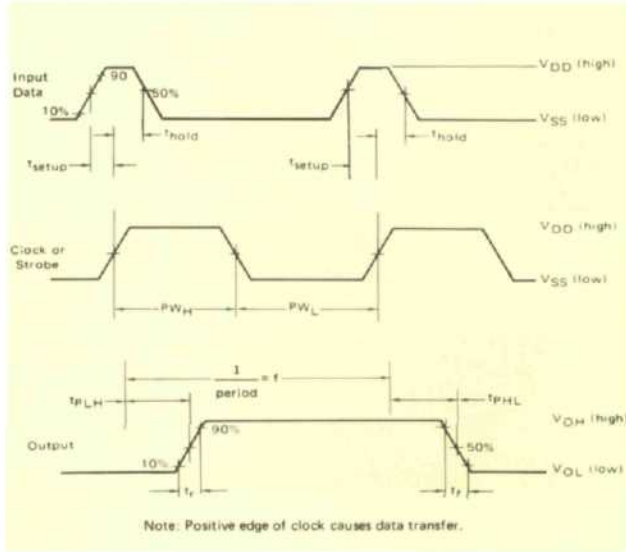



Figure 5. Circuit Waveshapes and Timing Parameters

## Minimum Clock Pulse Width

Minimum clock pulse widths, $PW_{Lmin}$ and $PW_{Hmin}$, as with propagation delays, can be specified in pairs although one or the other is often omitted. $PW_{Lmin}$ and $PW_{Hmin}$ refer respectively to the minimum widths of the low and high portions of the clock pulse. The specification is primarily a measure of how fast information can be shifted in a synchronous circuit without circuit malfunction. Pulse widths may also be specified for non-synchronous circuits such as non-clocked RS flip-flops and latches.

## Maximum Clock Frequency

The maximum clock frequency is the maximum rate at which information can toggle or transfer through a synchronous circuit without the circuit malfunctioning. Above this frequency, the circuit propagation delays become comparable to the reciprocal of the clock rate so that information may be improperly entered into the various clocked devices. The reciprocal of the sum of the low and high minimum pulse widths equals this frequency: PRF max = $1/(PW_{Lmin} + PW_{Hmin})$. Thus only two of the three parameters are usually specified.

## Maximum Input Rise and Fall Times

Input rise and fall time specifications describe the maximum, or slowest, input signal transition times at which an integrated circuit will properly function. These are most often given for the clock input of edge triggered devices, such as flip-flops, shift registers, and counters. Above maximum limits, transitions become so slow that data in the synchronous circuit may react with data in the previous stage rather than properly toggle to the next state.

## Minimum Setup Time

Minimum setup time is the length of time which information must be present on the data inputs of synchronous devices before the clock (or strobe) signal occurs. If the setup time is too short, data may be incorrectly entered into the device. The time is measured between the 50% points of the data and clock input signal edges.

## Minimum Hold Time

Minimum hold time is normally specified in conjunction with setup time. It is the length of time which data inputs must remain steady after occurrence of the clock edge. Again, it assures correct data entry into synchronous devices.

**NOTE:** This application note is concerned with pulse generator testing techniques. Discussion is thus focused mainly on dynamic parameters, or those having to do with timing and frequency considerations. Measurement of static voltages and currents is a separate problem and is not discussed.

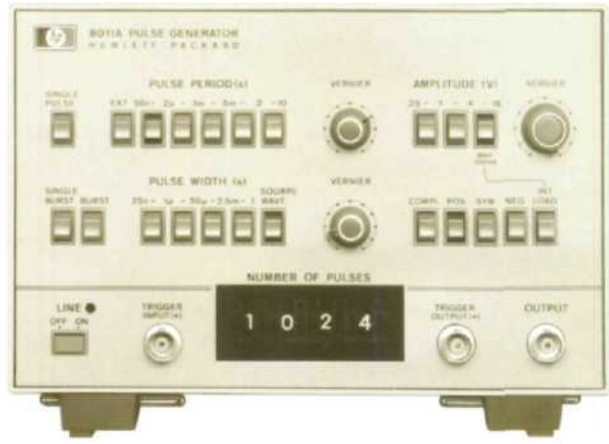



Figure 6. Pulse Generator 8011A

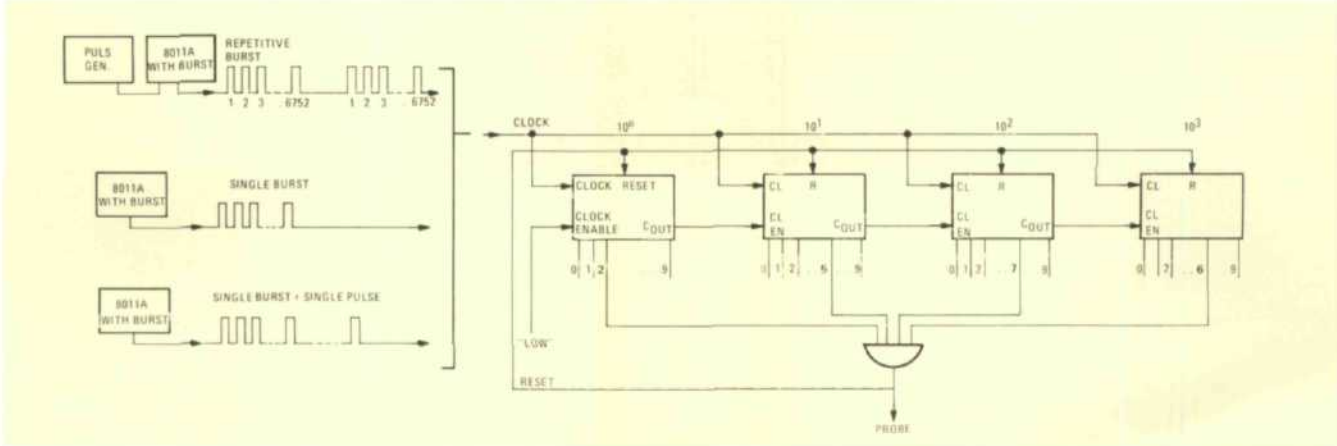



Figure 7. Burst Operation and Example

# FUNCTIONAL TESTING

As mentioned previously, test requirements for CMOS devices are of two different types:

1. Functional Tests
2. Parametric Tests

Functional testing is described in the paragraphs below. Parametric testing will be covered in the following section.

During functional testing, proper digital performance of the device-under-test is checked under a given, fixed set of operating conditions. Power supply voltage, input signal transition times, clock pulse width, and set-up times, for example, are all held constant during the test. The device or circuit is checked to see if it does work under the given conditions as opposed to finding out **how** it works and the effect of varying the conditions.

A typical example of functional testing is the work of a circuit design engineer to put together circuits comprising 30 – 50 IC's to perform a particular logic function. His concern is troubleshooting his design to remove mistakes he may have unintentionally designed in. Most often his requirement is for a basic pulse generator with variable amplitude and repetition rate to use as a clock source for his logic system. In addition a simple counted burst capability is also very useful to him. With it he can check blocks of logic by clocking to a specific point in the logic sequence and checking to see if the proper state has been reached.

Other areas concerned with functional testing include printed circuit (PC) board testing and incoming inspection testing of integrated circuits. Here the need is often for multichannel word generation to supply patterns to the multiple inputs of the devices under test. Still, however, the pulse response requirements of the stimulus signal are simple when a functional test is to be performed.

A listing of the requirements for a pulse generator capable of supplying signals for functional testing is as follows.

1. Repetition rate to 10 or 20 MHz
2. Single Channel
3. Variable output amplitude to 16 volts
4. Fixed pulse transition time $\leq$ 10 nS
5. 50 Ω Source impedance.

A pulse generator, for example, which fulfils the above requirements is the Hewlett-Packard model 8011A (see figure 6). It also includes other capabilities valuable in CMOS functional testing and two of these are discussed below.

## Interface

Proper interface to the test device requires a generator with a selectable, 50 Ω or high impedance, source impedance. Minimum reflections are achieved by back terminating with 50Ω in the generator when driving high capacitance loads. When the load capacitance is small, the generator should be operated as a current source (high output impedance) and a 50Ω termination should be used at the load.

## Pulse Burst Testing

Functionally testing counters, shift registers, memories or circuits built from these devices often requires the capability to supply a burst of an exact number of pulses to the test circuit. Model 8011A includes this capability in its option 001. The number of pulses desired, from 1 to 9999, is set into thumbwheel switches and upon triggering is delivered to the test circuit.

The burst can be started in one of two ways: by external electrical trigger or by pressing a pushbutton. At the end of a burst, extra pulses can be generated individually by pressing another pushbutton. Circuits can thus be clocked to a desired state at their operational clock rate and then analyzed under static conditions.

Figure 7 illustrates such an application. The circuit is a frequency divider and could represent a portion of some larger, more complex circuit. The circuit is comprised of 4 decade counter/decoders and should produce one high-going pulse at the AND gate output for each 6752 input clock pulses. The circuit is checked as follows.

A burst of exactly 6751 pulses is supplied to the clock line of the circuit. The AND gate output is then logic probed and an additional clock pulse delivered by pressing the 8011A's SINGLE PULSE button. The AND output should *pulse high briefly and return low* as the 6752nd clock pulse is delivered. Repetition rate or other pulse parameters can be varied and the test repeated. The pulse burst length is independent of other pulse generator settings and thus remains constant.

# PARAMETRIC TESTING

Parametric testing, in contrast to functional testing, is performed to determine how a device or circuit operates under given conditions and how it reacts if the conditions are changed. This requires, naturally, more detailed control of the test pulse shape and, therefore, a more complex test setup. Typical environments for parametric testing are manufacturing tests or component evaluations performed on integrated circuits.

The first step in expanding a functional test to a parametric test could be to investigate the dependence of the device operation on its clock input risetime. In practice when the IC is part of a larger circuit, actual input risetimes are limited by stray capacitance on signal nodes. Longer effective delays through the device result, and system maximum operating speed is reduced (see Figure 8). In testing to determine the magnitude of this variation, the effect of stray capacitance is best simulated by varying the rise and falltimes of the generator driving the clock (or other) input of the device.

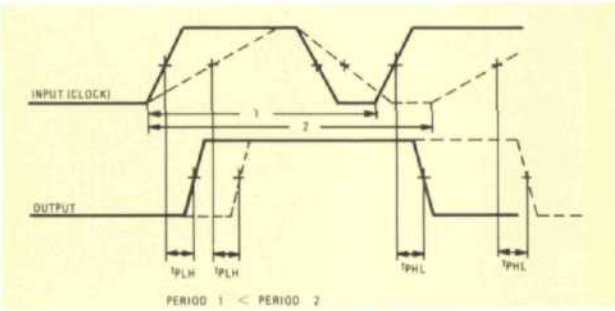



Figure 8. Influence of Transition Time on Pulse Period

An instrument particularly well suited to the needs of CMOS parametric testing is the Hewlett-Packard model 8015A pulse generator. It includes two variable rise and falltime outputs in addition to a number of other CMOS oriented capabilities and will be used as the example stimulus source in the applications which follow.

## Level Tracking

CMOS integrated circuits are specified to work properly over a power supply voltage range of 3 – 16 volts. Parameters, however, such as propagation delay and setup times are directly dependent on the power supply voltage. Thus for a true representation of device parametric behavior, parameters must be measured over a range of power supply voltages. Input signal amplitudes, which should equal the supply voltage and must never exceed it*, must also be varied concurrently with the power supply.

Level tracking capability (option 006 for model 8015A) simplifies this testing requirement and eliminates the danger of destroying the IC. Level tracking permits controlling the pulse generator output levels with an external control voltage, which is normally the device power supply. Signal levels automatically track the power supply voltage and device safety and proper input levels are ensured.

Figure 9 shows the connections between pulse generator, device-under-test, and power supply. The level tracking inputs are connected directly to the pulse generator's output amplifiers. The DUT (device-under-test) is protected even if the power supply is switched off.

## Direct Output Amplifier Access

Direct access to the pulse generator's linear output amplifiers (option 004) permits the pulse generator to be used as a level converter. TTL signals or low level word generator outputs may be amplified to CMOS compatible levels.

* *As briefly described earlier, CMOS integrated circuits are rapidly destroyed if the input signal level is ever greater than the power supply voltage. Device manufacturers go so far as to recommend disconnecting all low impedance test equipment from the device under test before switching off the power supply in order to avoid this danger.*

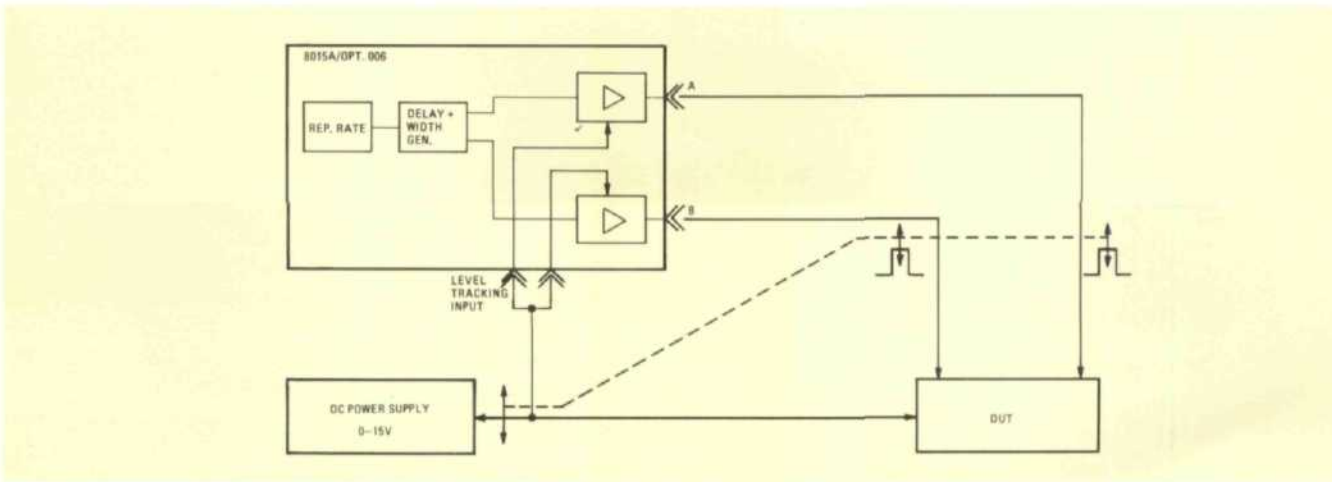



Figure 9. Level Tracking with the Device Power Supply

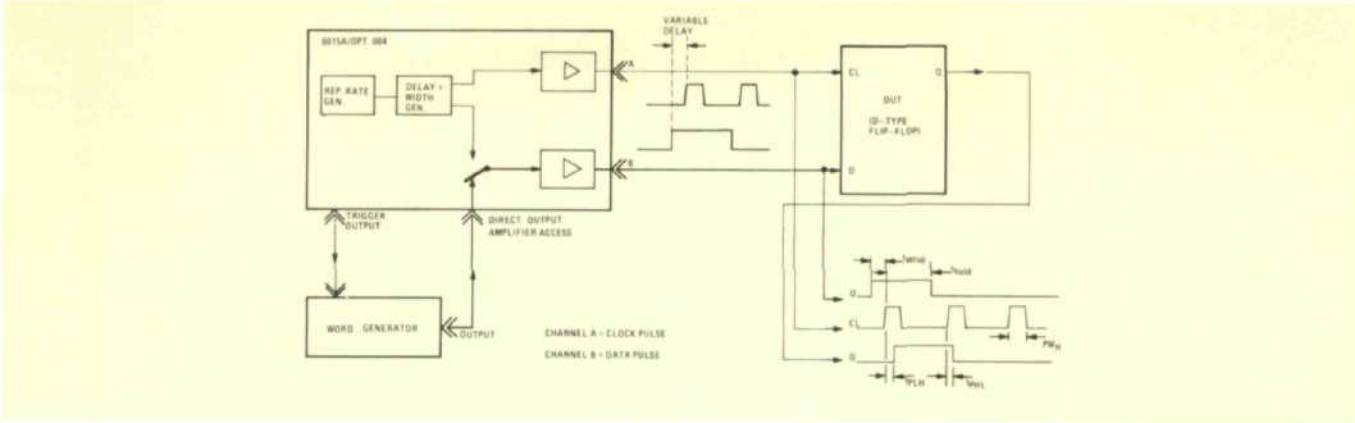



Figure 10. Direct Output Amplifier Access

As shown in Figure 10, a major advantage of using direct amplifier access is that two signals with a defined time relationship to each other are provided. One channel can be used as a clock signal and the other as data information. This configuration (figure 10) allows extremely convenient measurements of setup time, hold time and propagation delay.

Delay between the two channels is inserted using the normal pulse generator delay controls. Minimum setup time of the DUT can be measured by decreasing the delay between the clock pulse active edge and data pulse leading edge until a point just before the Q output disappears. The delay then present equals the minimum setup time and can be determined from the scope display.

Propagation delay is measured between the clock pulse active edge and the Q output leading edge. Minimum hold time is measured by decreasing the width of the word generator pulse (or increasing clock delay) until a point just before the Q output of the device disappears.

The word generator provides the advantage that the clock pulse parameters, particularly its width, can be adjusted independently of the data pulse. Device minimum clock pulse width sensitivity can thus be simply measured by decreasing the clock width until the output disappears.

## Two-Phase Clocking

A requirement of some CMOS circuits (and many PMOS devices) is multiple input clock signals. Figure 11, for example, shows 2-phase non-overlapping clock signals required by a CMOS shift register and other dynamic MOS devices.

Two-phase signals for IC driving or testing purposes are easily generated using model 8015A's capability for interchannel delay. Pulses with the proper amplitude, repetition rate, pulse width, and transition times are first set up in each of the generator's channels. Selecting B DELAY mode of operation, interchannel delay is inserted between the two outputs using the generator's delay controls. The proper phase relationship is easily achieved.

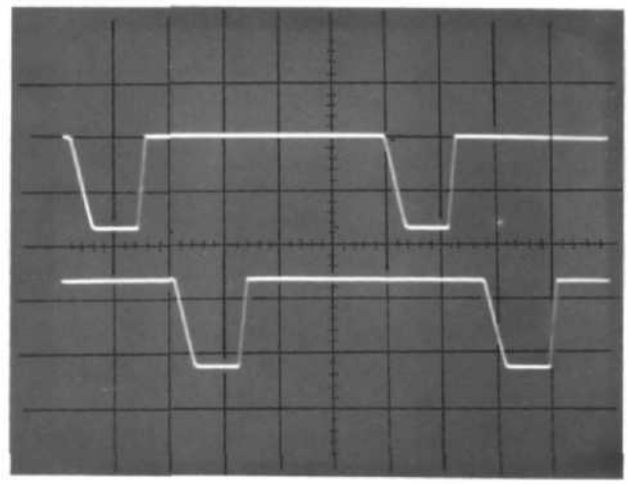


Figure 11. Two-phase clock signals required by dynamic shift registers. For proper shifting operation the pulses must be non-overlapping.

A further facility allows the A and delayed B channel signals to be added. Three level signals are thus generated, as shown in figure 12. These signals are often useful in other applications such as charge coupled device (CCD) testing or for simulating special codes. The signals may be generated in any of four formats by selecting different combinations of the NORMAL/COMPLEMENT switches. In addition the A and B pulse levels can be independently defined by the separate pulse amplitude controls.

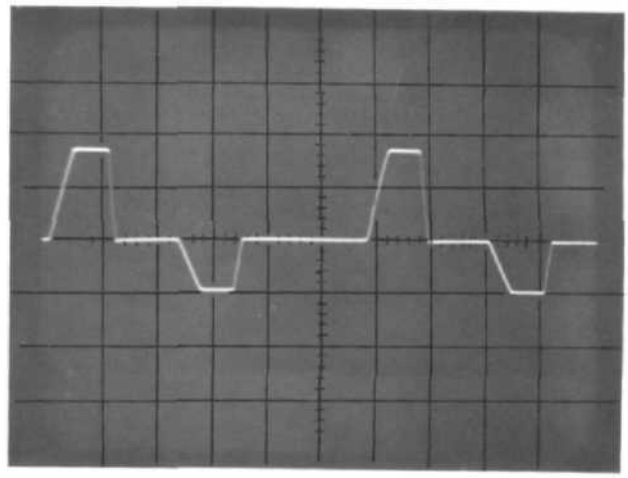


Figure 12. Three-level Signals

# PARAMETRIC TEST SET

All of the capabilities introduced above can be combined into a single test set. This configuration can perform tests of all dynamic CMOS parameters over the full range of operating voltages. The typical IC testing example shown below is intended to illustrate the application of the test set as well as summarize and conclude this application note. The device chosen is a CMOS 64 bit static shift register.

*The following parameters will be measured:*

- Minimum Setup and Hold Times
- Propagation Delay
- Minimum Clock Width
- Maximum Clock Rate
- Effect of Power Supply Variations
- Parameter Dependence on Clock Pulse Transition Time
- Correct Shifting Operation

The test set is comprised of the following instruments:

**Pulse Generator:** HP Model 8015A with

- Counted Pulse Burst (Option 002)
- Direct Output Amplifier Access (Option 004)
- Upper Output Level Tracking (Option 006)

**Word Generator:** HP 8006A

**DC Power Supply:** 0–15 volts

**Oscilloscope:** 4 channel

Figure 13 shows the complete parametric test set. The pulse generator is the master instrument. Its trigger output clocks the word generator thereby synchronizing the two instruments. The word generator output is amplified in one of the pulser's channels to the same levels as the second channel. Channel delay enables specific time relationships between the two channels, and level tracking keeps the signal amplitude always equal to the power supply voltage.

Measurement of minimum setup and hold times, propagation delay, and minimum clock pulse width has been described earlier.

To measure maximum clock rate all parameters are first set to minimum or worst case values. Pulse repetition rate is then increased until just before the output pulse disappears.

Device parameters on IC data sheets are typically given for a particular power supply voltage and not specified at other voltages. Still, testing over a range of voltages is often quite useful. If the CMOS IC is, for example, to be part of a battery-powered instrument, it enables the

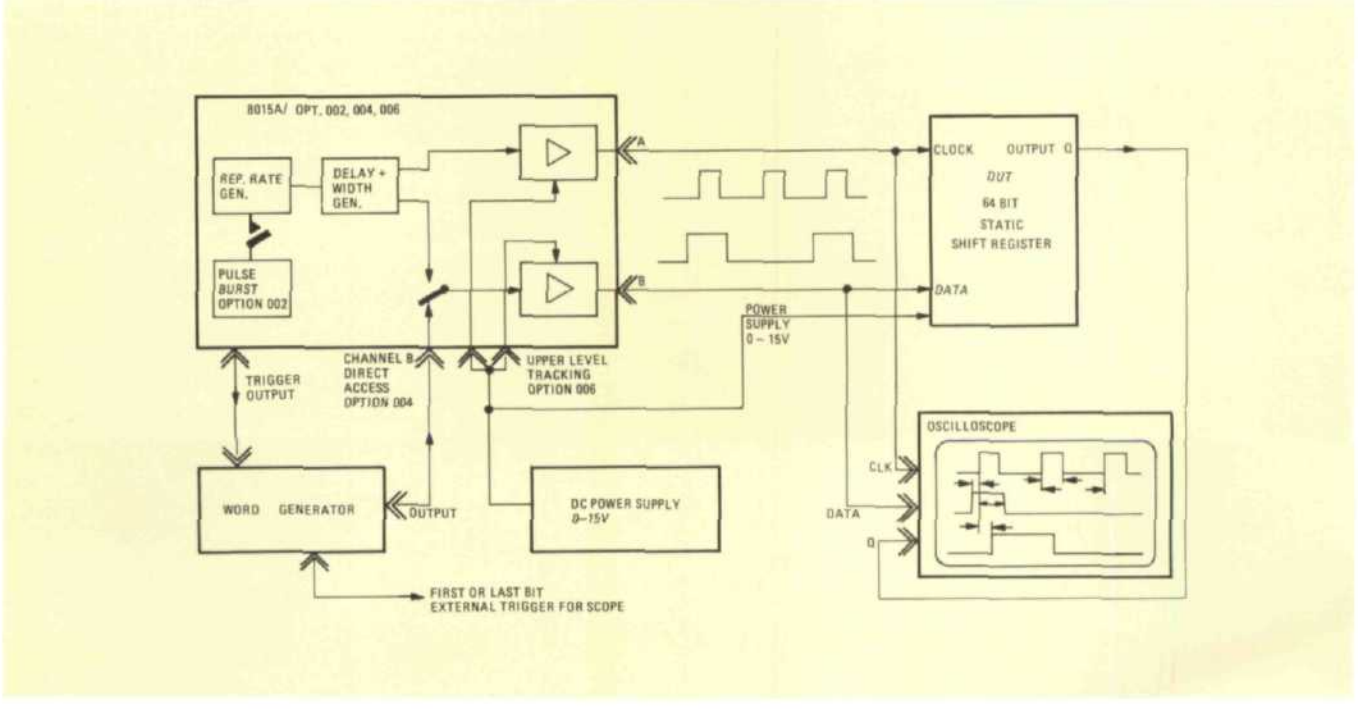



*Figure 13. Block Diagram of Complete Parametric Test Set*

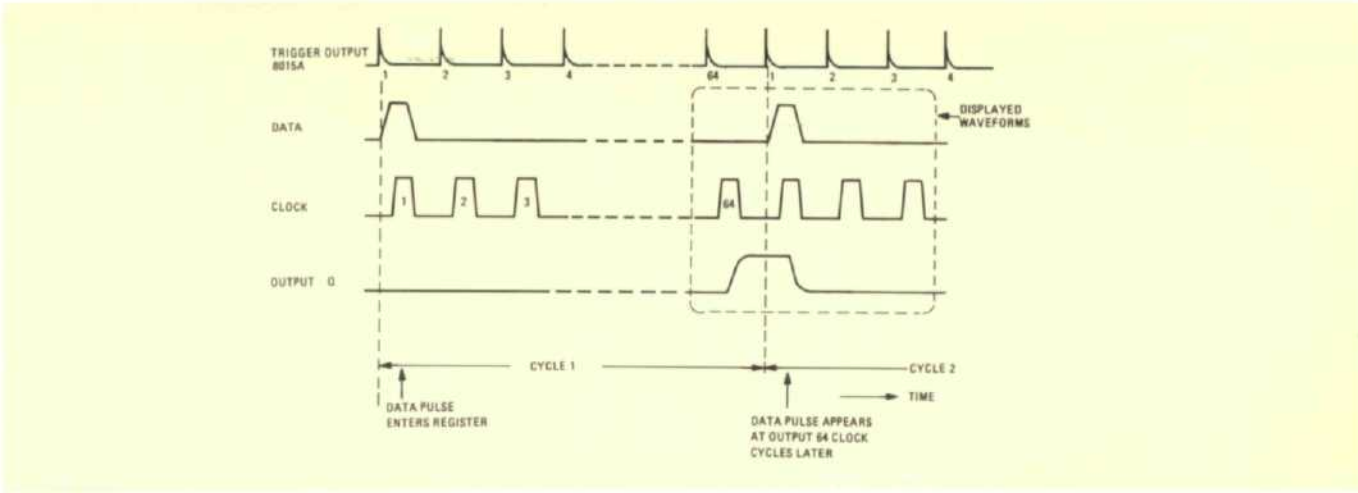



Figure 14. Shift Register Timing Relationship

design engineer to assess circuit performance at different battery voltages. This check can be carried out very simply. The power supply voltage is adjusted up and down and the parametric tests repeated.

Varying the pulse generator rise and falltimes allows investigation of the dependence of parametric performance on stray circuit capacitance. The designer thus gains an understanding of how his device will behave in the less than ideal environment of a real circuit.

A final test is of the dynamic length and operation of the shift register. It is performed with a pulse burst. The test could be a simple functional test to find out if the register is working properly. Alternatively it could form part of a parametric test in which the pulse burst is carried out with worst case parameters to check the register at its operating limits.

The word generator is set to produce a single 32 bit word (64, 16 or 8 bit words will also work). The word data is set to a one in the first bit and zeroes in all remaining bits. The pulse generator is set to deliver a burst of 64 pulses, and the burst is triggered either electrically or manually. If the shift register is working properly, the logic low level at the Q output should change to a one at the end of the burst. If an additional clock pulse is then delivered, the Q output should return to the low state.

Figure 14 shows the timing relationship between clock, data, and register output pulses. The first register outputs do not appear until 64 pulses after the start of the test.

Figure 15. Photograph of Complete Parametric Test Set

HEWLETT hp PACKARD

For more information, call your local HP Sales Office or East (301) 948-6370 • Midwest (312) 677-0400 • South (404) 436-6181 • West (213) 877-1282. Or write Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. In Europe: Hewlett-Packard S.A., P.O. Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. In Japan: Yokogawa - Hewlett-Packard, 1-59-1, Yoyogi, Shibuya-Ku, Tokyo, 151.

5952–6289

Printed in West Germany, June 1975