Errata

Document Title: Functional Analysis of Intel 4040 Microprocessor Systems (AN 167-16)

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HP References in this Application Note

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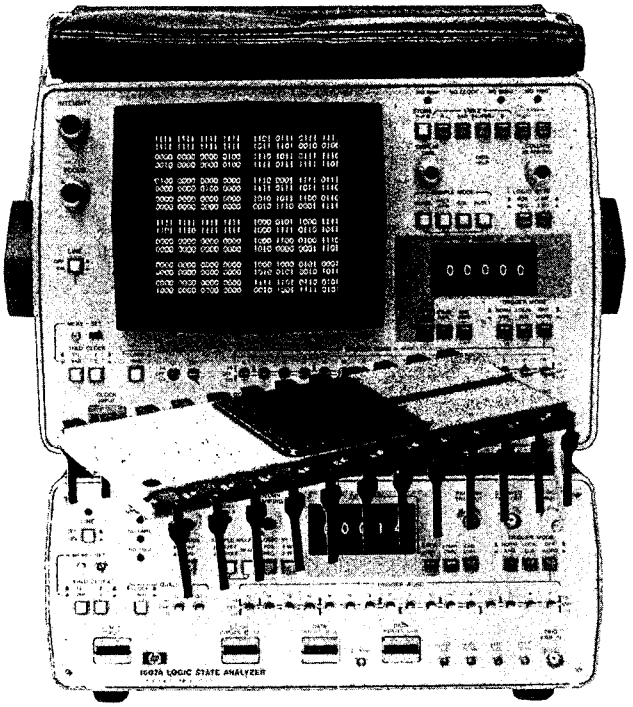
APPLICATION NOTE 167-16
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of Intel 4040 microprocessor systems.



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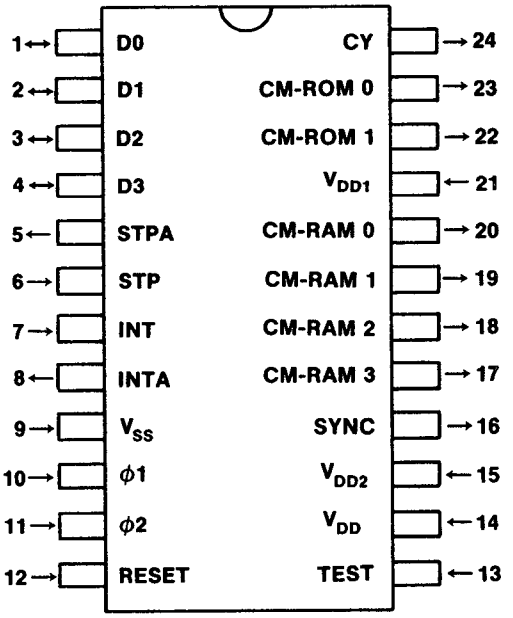
1. INTRODUCTION

This application note is designed to assist the 4040 Microprocessor family user in the real time analysis of his system in both design and troubleshooting environments. This note demonstrates real-time analysis of program flow, triggering on a specific event, as well as paging techniques.

The 4040 microprocessor, which is the heart of the 4040 microcomputer family, is fabricated with P-channel silicon gate MOS technology and operates from +5 volt and —10 volt power supplies. The 4040 features a 4-bit parallel CPU with 60 instructions. The 4040 can directly address 4k 8-bit instruction words of program memory or 8k with bank switching, and 5120 bits of data storage RAM. Up to 16 4-bit input ports and 16 4-bit output ports can also be addressed directly. Twenty-four randomly accessible index registers are provided internal to the microprocessor for temporary data storage. The 4040 microprocessor operates at clock rates to approximately 750 kHz.

2. PIN ASSIGNMENTS



SUMMARY OF CONTROL LINES

STPA Signal acknowledges that the processor has entered the Stop mode.

STP A logic "1" level on this input causes the processor to enter the Stop mode.

INT A logic "1" level on this input causes the processor to enter the Interrupt mode.

INTA Signal acknowledges receipt of an Interrupt command and prevents additional Interrupts from entering the processor. Signal remains active until cleared by the BBS instruction.

ϕ1, ϕ2 Non-overlapping clock signals that determine microprocessor timing.

RESET A "1" level applied to RESET clears all flag and status flip-flops and forces the program counter to 0. RESET must be applied for 96 clock cycles (12 machine cycles) to completely clear all address and index registers.

TEST Input. The logic state of TEST can be examined with JCN instruction.

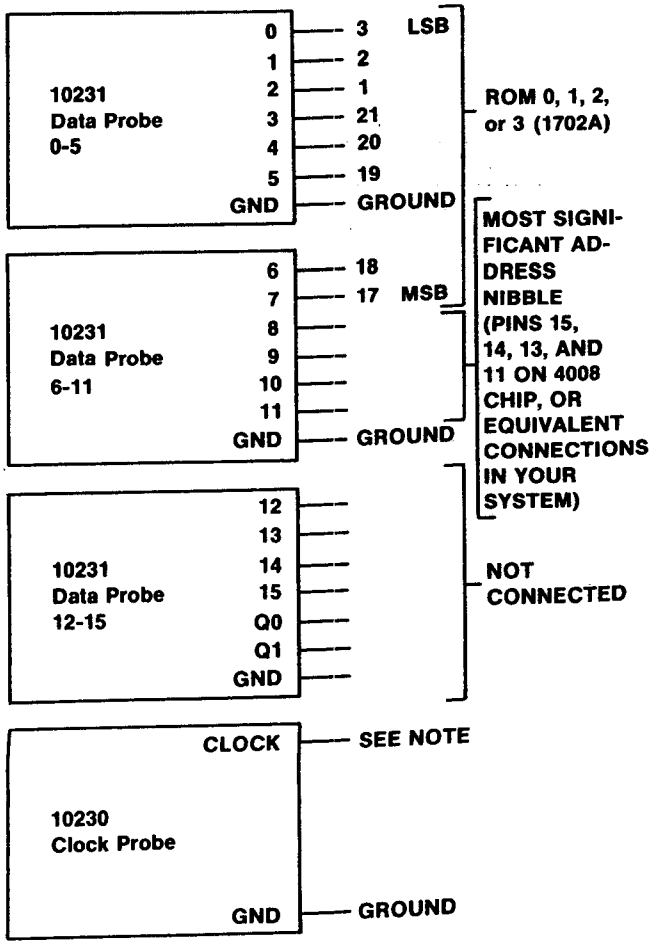
SYNC Synchronization signal indicating beginning of instruction cycle to ROM and RAM chips.

CM-RAM 0 thru CM-RAM 3 Lines function as bank select signals for the RAM chips in the system.

CM-ROM 0 CM-ROM 1 Bank selection signals for program ROM chips in the system.

CY The state of the carry flip-flop is present on this output and updated each X1 time.

3. PROBE CONNECTIONS



A system that will not "come up" can frequently be debugged by monitoring address flow alone. The 4040 CPU chip has a four-bit data bus, on which the 12-bit address is multiplexed during A 1, A 2, and A 3 states of the 4040 machine cycle. In order to view the demultiplexed 12-bit address on a 1600A, your 4040 system must use 4008/4009 Standard Memory and I/O Interface Sets, 4289 Standard Memory Interfaces, or similar logic circuits that provide a demultiplexed address bus. If your system uses memory chips that internally decode the multiplexed address, such as the 4001 ROM, you can monitor the microprocessor data bus as described in parts 9 and 10 of this application note.

NOTE:
Although the 4040 Microprocessor does not provide a unique clock for the Logic State Analyzer at the proper time (end of A 3 state) in the instruction cycle, the CM-ROM line is always true at A 3 and can be used as a clock signal. However, CM-ROM also occurs at states M 1, M 2, and X 2 during the execution of some instructions. This would result in invalid data being displayed by the Analyzer. By constructing the circuit shown in figure 1, you can ensure a correct state display. Use CM-ROM 0 if monitoring program stored in ROM bank 0, or CM-ROM 1 if monitoring program stored in ROM bank 1.

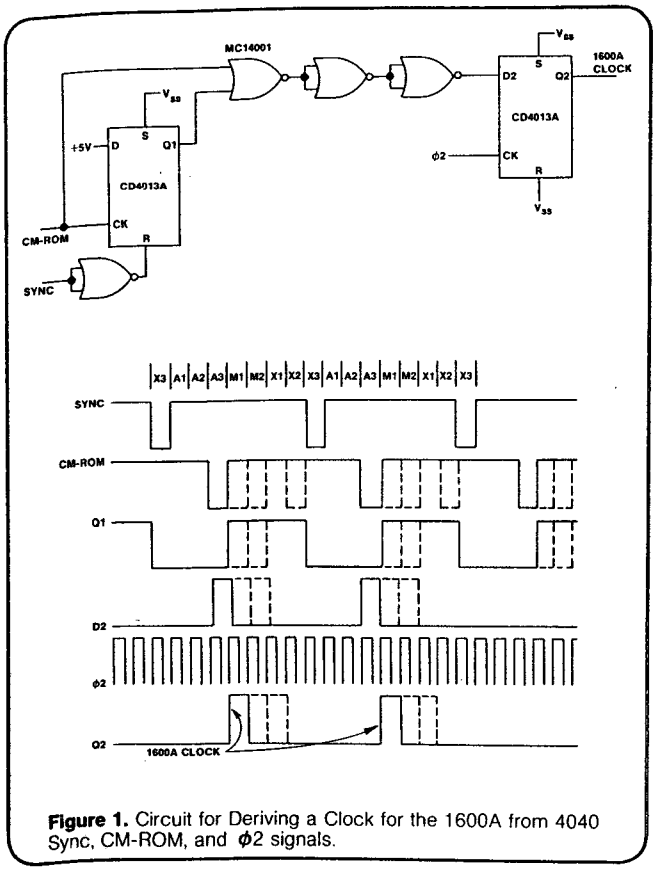


Figure 1. Circuit for Deriving a Clock for the 1600A from 4040 Sync, CM-ROM, and ϕ2 signals.

4. SETTING THE CONTROLS

Turn power on and set Logic State Analyzer controls as follows:

Display Mode ..... Table A
Sample Mode [1] ..... SGL
Trigger Mode
NORM/ARM ..... NORM
LOCAL/BUS ..... LOCAL
OFF/WORD ..... WORD

Threshold [2] ..... VAR, Adjust to 3.7 V
Logic ..... POS
Clock ..... ⌐
All other pushbuttons ..... out position
Display Time ..... ccw
Qualifiers ..... OFF
Trigger Word Switches .... set to match address you want to trigger on
Column Blanking ... after a display is on screen, adjust to display 12 columns of data

[1]"SGL" is selected for viewing single-shot events. Press "Reset" and start your system. The first time the system passes through the trigger point the display will be generated and stored. For programs that are looping or cycling through the selected address, select "Repet" sample mode.

[2]For TTL compatible systems, set threshold to TTL.

5. DISPLAY INTERPRETATION

In this illustration, an output routine is examined. Proper operation is confirmed by a comparison between real time state analysis, figure 2a, and the 4040 cross assembler program listing, figure 2b.

The output routine performs the following events:

1. Sets up a bit pattern in the accumulator.
2. Outputs the accumulator contents to an I/O port for control of status lights.
3. Reads status of start switch connected to input port.
4. If switch position is true (CY = 1), clears status lights and jumps to start routine; if switch position is false (CY = 0), loops.

Consider the state display photograph, figure 2a. Line 1 displays the address 0000 0100 0000 (040). This corresponds to the address of the STC instruction listed in the program listing, figure 2b. Lines 2 and 3 of the state display correspond to the JUN instruction at address 041. JUN is a two-word instruction, thus occupying two address locations. Examination of line 4 of the state display (0000 0100 0100) shows that the JUN instruction was properly executed, i.e., the program jumped to address 044. In a similar fashion, each instruction can be shown to have been executed in the proper sequence.

The last address shown in the state display is address 050. To view subsequent addresses you would simply set the Trigger Word switches to match address 050. This address would then become the trigger word in line 1 with the next 15 addresses listed in lines 2 through 16. If you wish to retain the original trigger point, an alternate technique is to use digital delay and set the thumbwheels to 00015 which would provide the same display.

6. THE MAP

If a tabular display is not presented in Section 5, it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to "map" (figure 3). Using the Trigger Word switches move the cursor (circle in photo) to encircle one of the dots on screen. Switch to Expand and make the final positioning of the cursor—the No Trigger light will now go out and switching back to Table A displays the 16 addresses around that point.

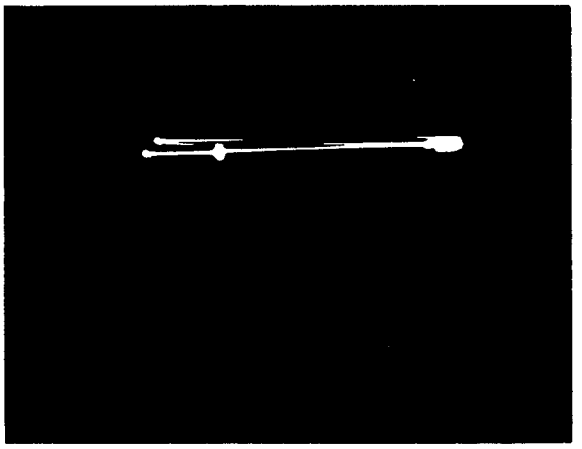
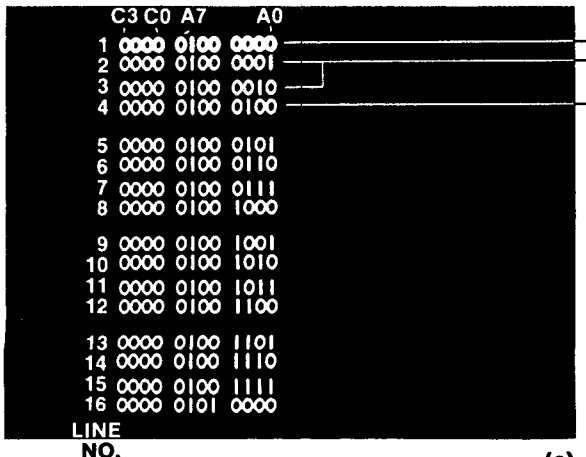


Figure 3. Map Display Shows Entire System Activity.



(a)

057	040	FA	STC	SET CY = 1
058	041	4044	JUN	JUMP TO ADDRESS 44
059	043	F0	CLB	SET ACC AND CY = 0
060	044	F6	RAR	ROTATE ACC RIGHT
061	045	FA	STC	SET CY = 1
062	046	F6	RAR	ROTATE ACC RIGHT
063	047	FA	STC	SET CY = 1
064	048	F6	RAR	ROTATE ACC RIGHT
065	049	FA	STC	SET CY = 1
066	04A	F6	RAR	ROTATE ACC RIGHT
067	04B	21	SRC	SELECT OUTPUT PORT 0
068	04C	E2	WRR	WRITE ACC → OUTPUT PORT 0
069	04D	EA	RDR	READ INPUT PORT 0 → ACC
070	04E	F1	CLC	CLEAR CY
071	04F	F5	RAL	ROTATE ACC LEFT
072	050	1A4D	JCN	JUMP TO ADDRESS 4D IF CY = 0
073	052	F0	CLB	CLEAR ACC AND CY
074	053	E2	WRR	WRITE ACC → I/O PORT 0
075	054	400F	JUN	JUMP TO ADDRESS 0F

(b)

Figure 2. System Response to Output Routine.

7. VIEWING ADDRESS, DATA, AND CONTROLS

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the data bus or command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the 12-bit address, 8-bit data word and up to 12 other active control signals to be viewed simultaneously. The hookup is easy:

1. Connect data cable between rear panel connectors.

2. Connect trigger bus cable between front panel bus connectors.

3. Set 1600A controls as described in Section 4 with the following exception: set display mode to Table A & B

4. Set 1607A controls as follows:

   Sample Mode ..... SGL
   Start Display ..... ON
   Trigger Mode
   NORM/ARM ..... NORM
   LOCAL/BUS ..... BUS
   OFF/WORD ..... OFF
   Threshold, Logic, Clock ..... same as 1600A
   All other pushbuttons ..... out position
   Q0, Q1 ..... OFF

5. Connect data and clock inputs for 1607A as follows:

   a. Connect 1607A Data inputs 0 through 7 to RD 0 through RD 7 outputs of 1702A ROM chip (pins 4 through 11 in order).

   b. Connect 1607A Data Input 8 to CY output of 4040 chip (pin 24).

   c. Connect 1607A clock input to signal used to clock 1600A.

   d. Connect grounds to appropriate points.

6. After a display is on screen, set the 1607A blanking to display nine columns.

8. DISPLAY INTERPRETATION OF ADDRESS, DATA AND CONTROL LINES

By displaying both address, data and control lines, it is now possible to confirm exact system operation with respect to the output routine. Consider the program listing, figure 4b. The first address, 040, contains an STC instruction. The second address, 041, is the address of the first word of a two-word JUN instruction. These two instructions are shown in lines 1 through 3 of the state display, figure 4a. Line 1 shows the address (0000 0100 0000) and instruction code (1111 1010) of the STC instruction. Lines 2 and 3 show the addresses of the two words that make up the JUN instruction. The first byte (0100) of the JUN instruction is the operation code and the remaining three bytes (0000 0100 0100) is the address that program control is transferred to. Examination of line 4 of the state display shows that program control was indeed transferred to the specified address which contains an RAR instruction (instruction code 1111 0110). Line 5 of the state display corresponds to the STC (Set Carry) instruction at address 045. Proper execution of the STC instruction is confirmed by observing that the carry bit (CY column) in line 6 of the state display is a one. The one shows up in the CY column one cycle after the STC instruction because the 1600A is clocked during A 3 state, i.e., before the instruction is executed. Thus the 1600A does not see the results of the instruction execution until the next A 3 state.

Each line of the display can be examined in a similar fashion to reveal exact program operation.

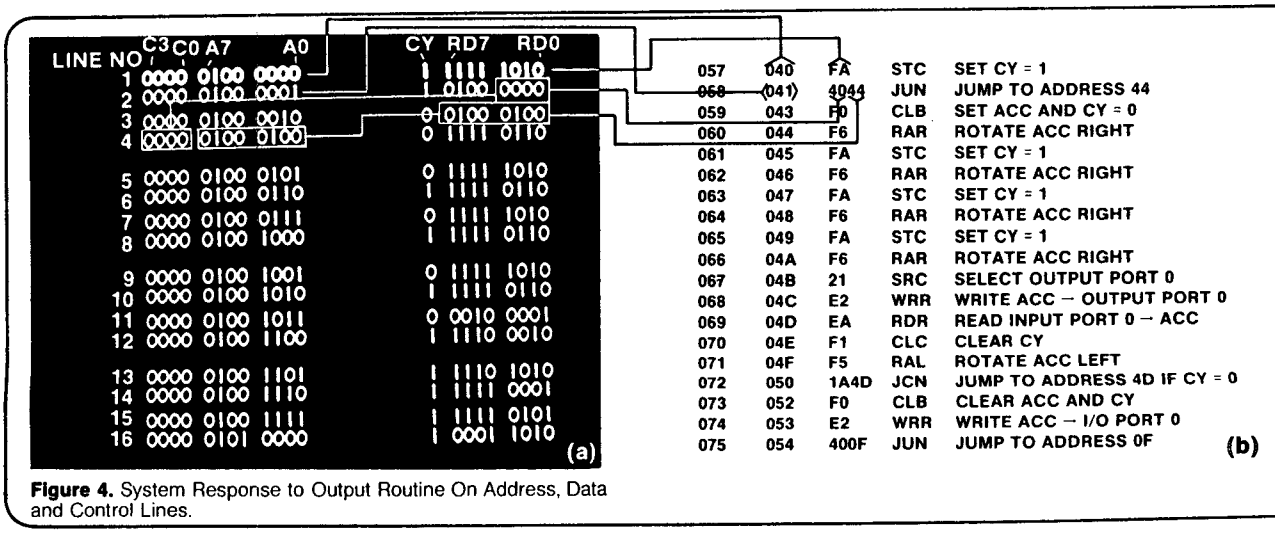


Figure 4. System Response to Output Routine On Address, Data and Control Lines.

9. VIEWING THE MULTIPLEXED DATA BUS

In the preceding examples, the demultiplexed address and data lines have been observed. However, when a hardware failure occurs, it may be very useful to directly observe activity on the multiplexed microprocessor data bus. In the following example, we shall observe data being demultiplexed into a 12-bit address for driving a ROM. Then we shall watch the ROM output being multiplexed back onto the bus.

Set up the 1600A and 1607A to obtain the display as follows:

1. Connect 1600A data, qualifier, and clock inputs as follows:
   a. 1600A data inputs 0 through 7 to RD 0 through RD 7 in order.
   b. 1600A data inputs 8 through 15 to A 0 through A 7 in order.
   c. 1600A Q0 input to ROM 0 chip select line (1702A, pin 14). [3]
   d. 1600A clock input same as in Section 3.

   [3]By qualifying on $\overline{CS}$ and triggering on A 0 through A 7, we derive a unique trigger that is effectively 12-bits wide with only the eight least significant bits displayed.

2. Connect 1607A data and clock inputs to microprocessor as follows:
   a. 1607A data inputs 0 through 3 to D 0 through D 3.
   b. 1607A data input 4 to CM-ROM line for ROM bank being monitored.
   c. 1607A data input 5 to SYNC line.
   d. 1607A clock input to $\phi 2$.

3. Set 1600A controls the same as in Section 4 with the following exceptions:

   Display Mode ..... Table A&B
   End Display ..... ON
   Delay .....ON, delay set to 8
   Qualifier ..... TRIG, Q0 set to LO
   Column Blanking ..... CCW

4. Set 1607A controls as follows:

   End Display ..... ON
   Delay .....ON, delay set to 8
   Logic [4] .....NEG

   [4]The microprocessor data bus uses negative logic, i.e., the most positive voltage is a "0" and the most negative voltage is a logic "1".

5. After a display is obtained, adjust 1607A column blanking to display 6 columns in Table B.

10. DISPLAY INTERPRETATION OF MULTIPLEXED DATA BUS

The state display photograph in figure 5 shows a comparison of the demultiplexed address and data buses (Table A) with the multiplexed microprocessor bus (Table B). Let's compare line 8 of Table A (trigger word) with the multiplexed data in Table B. Examination of the Sync line shows that line 6 of Table B corresponds with instruction cycle state A 1. Note that the Sync and CM-ROM pulses are displayed as ones in the photograph since we have selected negative logic on the 1607A. Comparison of states A 1, A 2, and A 3 (lines 6, 7, and 8 of the Table B state display) with the trigger word address bits reveal that the interface circuit has correctly demultiplexed the address from the 4040. Similarly, comparison of trigger word data bits RD 7 through RD 0 with states M 1 and M 2 (lines 9 and 10 of the Table B display) shows that the interface circuit has correctly multiplexed the ROM data onto the 4040 data bus. Note that the CM-ROM line is true during M 1 and M 2 states indicating that the instruction word being executed is the first word of an I/O instruction.

11. CONCLUSION

From the foregoing examples it may be concluded that efficient troubleshooting of the Intel 4040 Microprocessor system is expedited by two factors: first, the availability of the program lising as produced by 4040 cross assembler; and second, the availability of real time Logic State Analysis to display actual system operation for rapid error detection and correction.

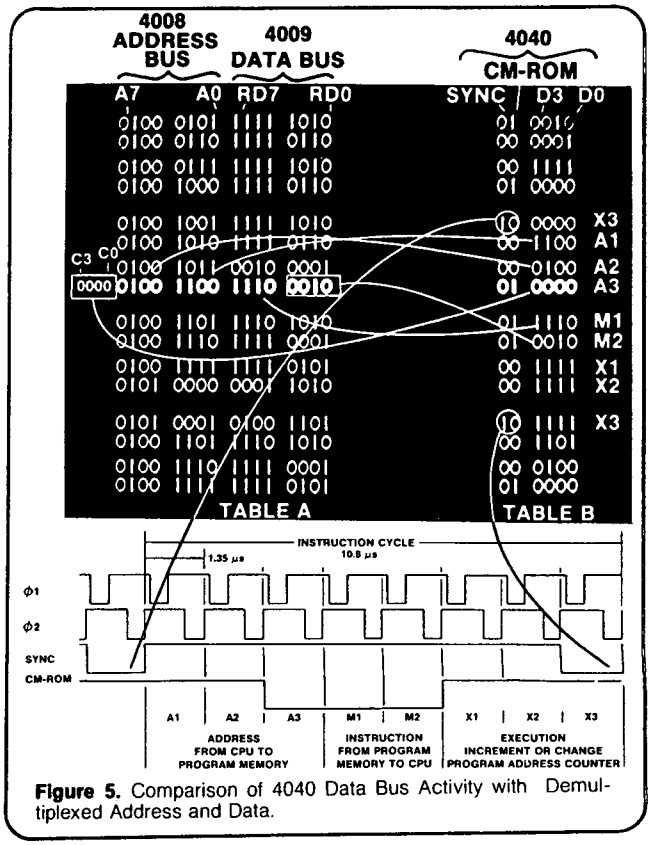


Figure 5. Comparison of 4040 Data Bus Activity with Demultiplexed Address and Data.

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Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Ca ls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A).
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
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167-9 Functional Analysis of Motorola M6800 Microprocessor Systems (1600A and 1607A).
167-10 Using the 1620A for Serial Pattern Recognition (1620A).
167-11 Functional Analysis of Intel 8008 Microprocessor Systems (1600A).
167-12 Functional Analysis of Fairchild F8 Microprocessor Systems (1600A and 1607A).
167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A).
167-14 Functional Analysis of 8080 Microprocessor Systems (1600A and 1607A).
167-15 Functional Analysis of Intel 4004 Microprocessor Systems (1600A and 1607A).

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