Errata

Document Title: Functional Analysis of Fairchild F8 Microprocessor Systems (AN 167-12)

Part Number: 5952-2012

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HP References in this Application Note

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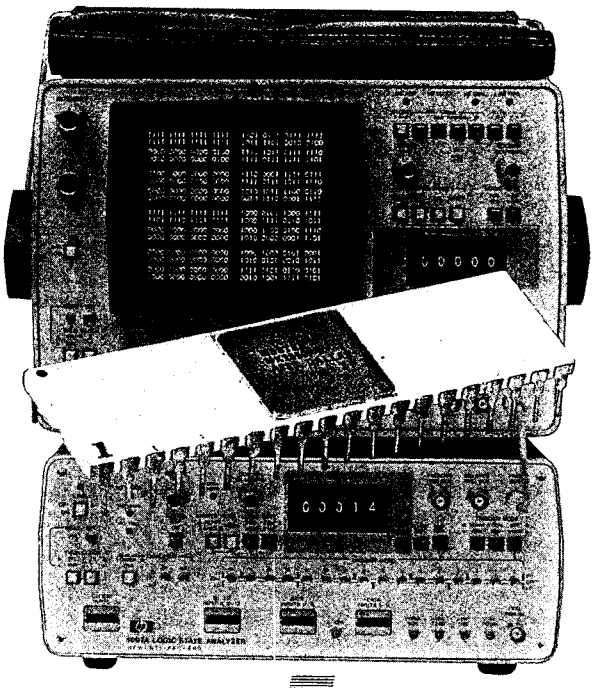
APPLICATION NOTE 167-12 A
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of Mostek F8 microprocessor systems.



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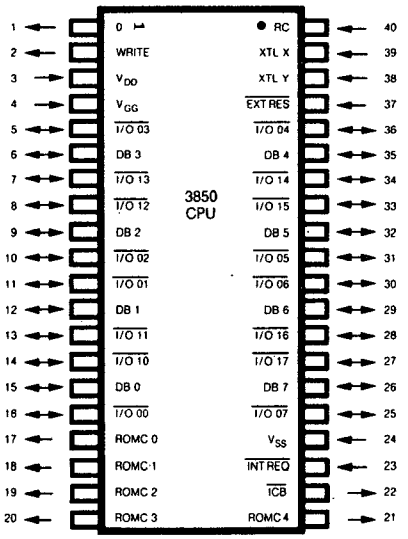
1. INTRODUCTION

This application note is designed to assist the Mostek F8 Microprocessor family user in the real time analysis of his system in both design and troubleshooting environments. The note demonstrates real time analysis of actual program sequences, triggering on specific events, selective data qualification, and paging techniques.

The Microprocessor and Read Only Memory form a basic two chip system that will handle most simple tasks. For more complex processing functions the memory access and interface chips complete a four chip set. The F8 System is unique in that each chip has its own resident program counter eliminating the need for a dedicated address bus and its associated circuits. Branch commands which require resetting the address counter are multiplexed onto the data bus for implementation. This architecture makes possible a very low cost system including I/O ports as a standard part of the basic chips.

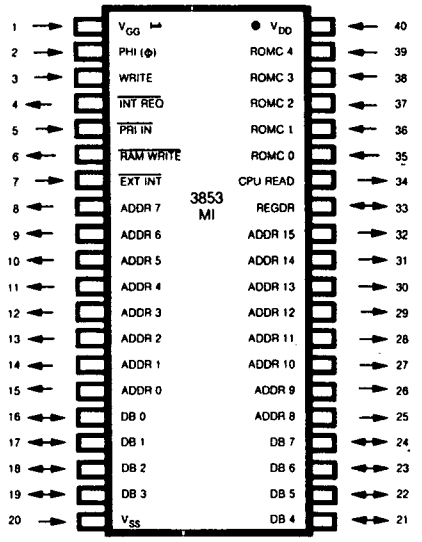
2. PIN ASSIGNMENTS

Central Processing Unit Chip Pin Assignments



PIN NAMES	DESCRIPTION	TYPE
DB 0 - DB 7	Data Bus	Bidirectional
I/O 00 - I/O 07	I/O Port Zero	Input/Output
I/O 10 - I/O 17	I/O Port One	Input/Output
ROMC 0 - ROMC 4	Control Lines	Output
RC	RC Timing Input	Input
XTL-X	Crystal Clock Inputs	Input
XTL-Y	External Clock Inputs	Input
EXT RES	External Reset	Input
Φ, WRITE	Clocks	Output
$\overline{ICB}$	Interrupt Control Bit	Output
$\overline{INT\ REQ}$	Interrupt Request	Input
V_{DD} V_{SS} V_{GG}	Power	Input

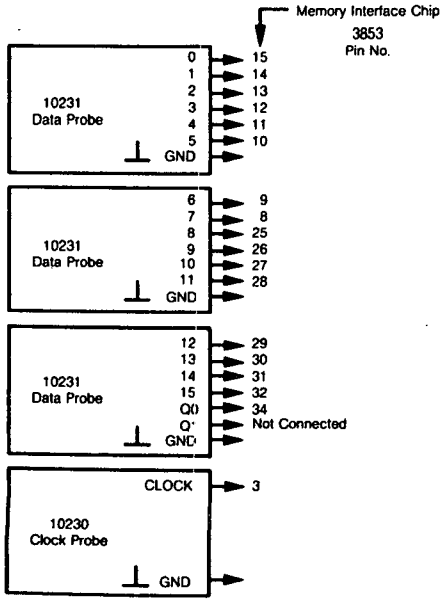
Memory Interface Chip Pin Assignments



PIN NAME	DESCRIPTION	TYPE
DB 0 - DB 7	Data Bus	Bidirectional
ADDR 0 - ADDR 15	Address	Output
Φ WRITE	Clocks	Input
INT REQ	Interrupt Request	Output
PRI IN	Priority in Line	Input
RAM WRITE	Write Line	Output
EXT INT	External Interrupt Line	Input
REGDR	Register Drive Line	Input/Output
CPU READ	CPU Read Line	Output
ROMC 0 - ROMC 4	Control LInes	Input
V_{SS} V_{DD} V_{GG}	Power Lines	Input

3. PROBE CONNECTIONS

A system that will not "come up" can frequently be debugged by monitoring address flow alone. With a system comprised of the F8 Central Processing Unit and Memory Interface chips, the following Logic State Analyzer probe connections provide a display of the activity on the address lines located on the Memory Interface chip.



4. SETTING THE CONTROLS

Turn power on and set the Logic State Analyzer Controls as follows:

Display Mode - Table A
Sample Mode - REPET
Start Display - ON
Trigger Mode - NORM
LOCAL
WORD
Threshold - TTL
Clock slope - ⌐
All other pushbuttons - out
Display Time - ccw
Column Blanking - ccw
Qualifiers - Q0-HI, Q1-OFF
Trigger Word switches - Set to Address at which you wish to trigger*

*If program is not looping or cycling through the selected address, select "Single", press "Reset" and start your system. The first time the system passes through the selected trigger state the display will be generated and stored.

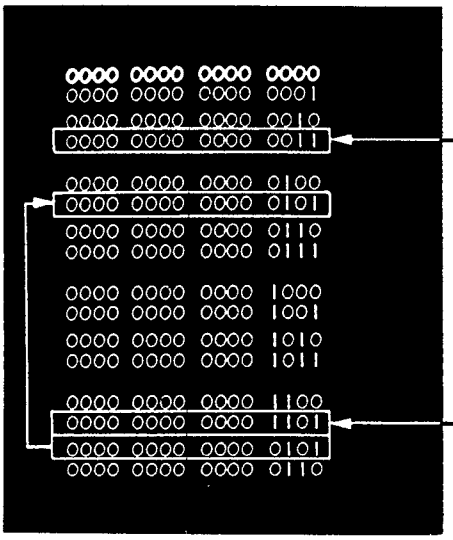
5. DISPLAY INTERPRETATION

Figure 1 illustrates a portion of a start-up program to help you understand the Logic State Analyzer display. Your program will work equally well. Proper operation is confirmed by a comparison between real time state analysis and the start-up program.

With Q0 probe connected to CPU READ, Q0 set HI, and triggering on address 0000, an address is incremented with every memory fetch. Notice that the address sequence branches after address 000D where it loops back to clear all F8 scratch pad registers, and then the program is re-entered at address 000E.

It is easy to determine whether this loop is completed by using the "Paging" technique. Reset the Logic State Analyzer trigger word switches to address 000D and restart the system. The display then begins at address 000D and the next 15 addresses are displayed.

Some addresses in the start-up program involve multiple word instructions. These may be observed on the display as redundant consecutive addresses by placing the Q0 switch in the OFF position.



ADDRESS	MACHINE FORMAT INSTRUCTION	FUNCTION
0000	70	Clear Accumulator
0001	B0	Output Port 00 ◄ one byte from ACC
0002	B1	Output Port 01 ◄ one byte from ACC
0003	B8	Output Port 08 ◄ one byte from ACC
0004	B9	Output Port 09 ◄ one byte from ACC
0005	0B	Load ISAR from ACC
0006	70	Clear Accumulator
0007	5C	Load Scratch Pad Register 'C' ◄ ACC
0008	0A	Load Accumulator from ISAR
0009	58	Load Register 8 from ACC
000A	24	Add Immediate
000B	41	41 to Accumulator
000C	81	If result of previous step is positive
000D	F8	Branch to Address 0005
		Loop is continued until all F8 Scratch Pad Registers Clear
000E	20	Load Immediate and
000F	0C	Call Subroutine Direct

Figure 1. System Response to a Start-up Program.

6. THE MAP

If a tabular display is not presented in the previous step it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to "map" (figure 2). Using the Trigger Word switches move the cursor to encircle one of the dots on screen. Switch to expand and make the final positioning of the cursor---the No Trigger light will now go out and switching back to Table A displays the 16 bit address around that point.

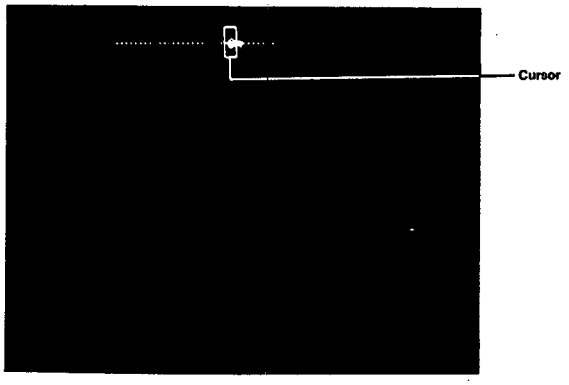


Figure 2. Map Display Shows Entire System Activity

7. VIEWING ADDRESS, DATA, AND CONTROLS

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data Bus, Control Bus, or other command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the 16 bit address, 8 bit data bus, and eight other active command signals to be viewed simultaneously. A typical test setup is shown in figure 3. The hookup is easy.

Figure 3. Typical Test Setup of 1600A and 1607A for Displaying up to 32 Bits of Information.

1. Connect data cable between rear panel connectors.
2. Connect trigger bus cable between front panels of instruments.
3. Select Trigger Mode "Word" on 1600A, "Bus" and "Off" on 1607A.
4. Select "Start Display", sample mode "Repet", on both Analyzers, and the table "A&B" on 1600A.

5. Select Threshold and Logic Polarity on 1607A to be the same as the 1600A.
6. Leave all other pushbuttons out.
7. 1600A data and clock inputs connected for address as described in Part 3.
8. Set Q0 and Q1 off.
9. Connect data and clock inputs for 1607A to the MI as follows:
   a. 1607A Data inputs 0 through 7 to DB 0 through DB 7 in order.
   b. 1607A Data Input 8 to pin 34 CPU READ.
   c. Clock to pin 3.
   d. Grounds to appropriate point(s).
10. Set Column Blanking to display 9 columns on the 1607A.

8. DISPLAY INTERPRETATION OF ADDRESS AND DATA BUSES AND CPU READ CONTROL LINE

As an amplification of the previous example, it is possible to investigate all the activity on the address and data buses plus the CPU READ control line.

Operating the Logic State Analyzer system as set up in section seven, the display shows all activity on the address bus as well as on the data bus during the start-up program. In addition, the CPU READ control line is monitored to permit confirmation of system performance.

Figure 4 illustrates multiple-word instruction addresses and at the same time shows activity on the address bus during the execution of the instruction. At address 0004, the data bus indicates that I/O Port 08 is addressed. Then, contents of the accumulator are sent to the I/O Port. In the next instruction, CPU READ is high and the data bus shows that the instruction has been completed at instruction code B9 and the program counter has been incremented to the next address. In a similar manner, each address in the program may be analyzed.

9. CONCLUSION

From the foregoing examples it may be concluded that efficient troubleshooting of the Mostek F8 Microcomputer System is expedited by two factors; FIRST: the availability of the program listing as produced by F8 cross assembler, which is the definitive document of program execution and; SECOND: the availability of real time Logic State Analysis to display actual system operation for rapid error detection and correction.

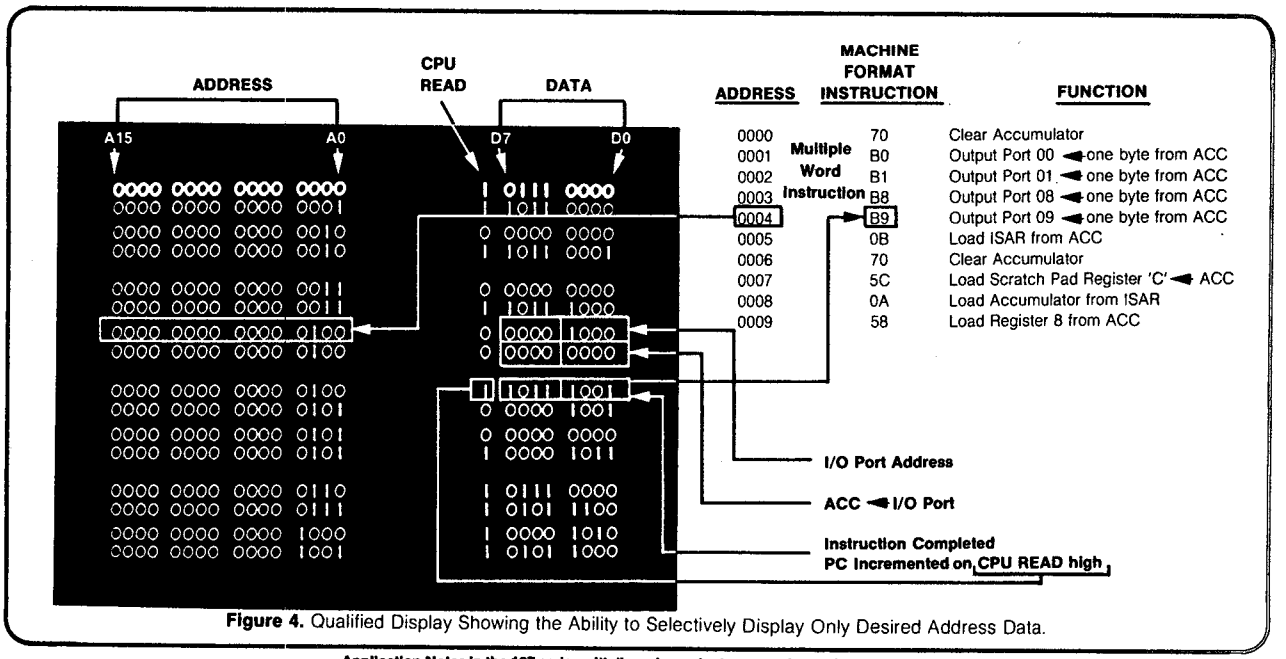


Figure 4. Qualified Display Showing the Ability to Selectively Display Only Desired Address Data.

Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Calls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A).
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
167-8 Stable Displays of Disc System Waveforms Synchronized to Record Address (1620A).
167-9 Functional Analysis of Motorola M6800 Microprocessor Systems (1600A and 1607A).
167-10 Using the 1620A for Serial Pattern Recognition (1620A).
167-11 Functional Analysis of Intel 8008 Microprocessor Systems (1600A and 1607A).
167-12 Functional Analysis of Fairchild F8 Microprocessor Systems (1600A and 1607A).
167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A).
167-14 Functional Analysis of 8080 Microprocessor Systems (1600A and 1607A).
167-15 Functional Analysis of Intel 4004 Microprocessor Systems (1600A and 1607A).
167-16 Functional Analysis of Intel 4040 Microprocessor Systems (1600A and 1607A).
167-17 Functional Analysis of National IMP Microprocessor Systems (1600A and 1607A).
167-18 Functional Analysis of National Semiconductor SC/MP Microprocessor Systems (1600A and 1607A).
167-19 Systematic "turn-on" of μP Systems using Logic State Analyzers (1600A and 1607A).

VIDEO TAPE SERIES: The four hour series titled "The Data Domain Its Analysis and Measurements" introduces logic state analysis and measurement techniques unique to the data domain. Contact your HP Field Engineer for price and availability of this color tape series.

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