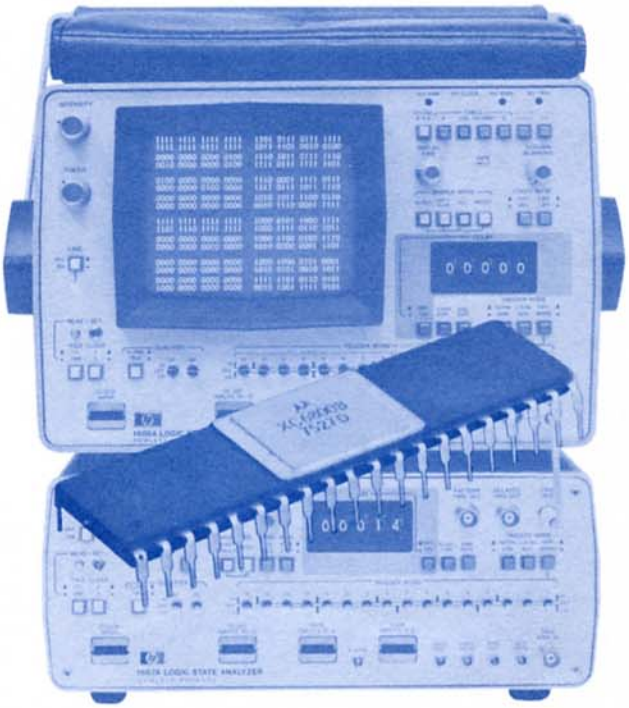
APPLICATION NOTE 167-9
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of the Motorola M6800 microprocessor system.



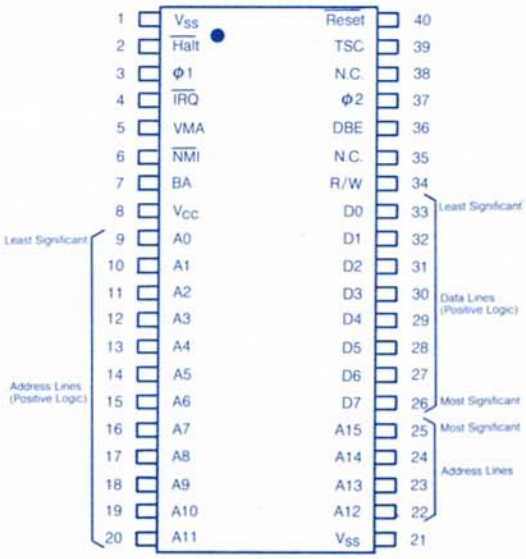
HEWLETT hp PACKARD

1. INTRODUCTION

This application note is designed to assist the M6800 Microprocessor family user in the real time analysis of his system—in both design and troubleshooting environments. The note demonstrates real time analysis of program flow in positive and negative time, triggering on a specific event, as well as paging techniques.

The MC6800 microprocessor, which is the nucleus of the M6800 microcomputer family, is constructed with N channel silicon-gate MOS technology, operating from a single +5 volt supply. The features of the microprocessor include a 16-bit three-state address bus allowing 65K addressable bytes of memory and a three-state 8-bit bidirectional data bus. The system, which includes both maskable and nonmaskable interrupts, operates at clock rates to 1 MHz.

2. PIN ASSIGNMENTS

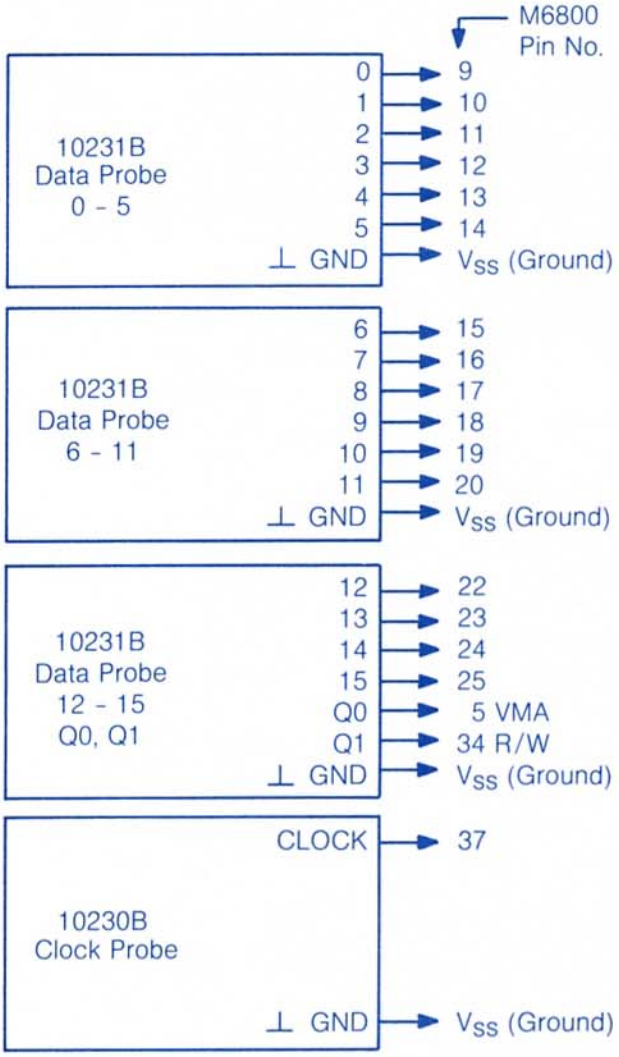


SUMMARY OF CONTROL LINES

	LOW "0" V_{SS}	HIGH "1" ≥2.4 V
$\overline{HALT}$	All machine activity halted	Machine will fetch and execute instructions
$\overline{IRQ}$	Interrupt request pending	No Interrupt Request
VMA	Address Bus data is INVALID	Address Bus data is VALID
$\overline{NMI}$	A nonmaskable Interrupt Request is pending	Nonmaskable interrupt is not pending
BA	Address bus is not available	Address bus is available and microprocessor activity has stopped
$\overline{RESET}$	All microprocessor registers cleared, all machine activity halted	On ⌐ microprocessor executes initial start-up sequence
TSC	Address lines and R/W line are not HI-IMPEDANCE	Address lines and R/W in HI-IMPEDANCE
DBE	Data bus lines are in HI-IMPEDANCE	Data bus drivers are enabled
R/W	MPU "WRITE" operation-data from microprocessor to memory or peripheral	MPU "READ" operation-data from memory or peripheral into microprocessor

3. PROBE CONNECTIONS

A system that will not "come-up" can frequently be debugged by monitoring address flow alone. The following Analyzer probe connections provide a display of the activity on the address lines. If address bus extenders are employed, make connections on the "Extended" side of the Bus.



4. SETTING THE CONTROLS

Turn power on and set Logic State Analyzer Controls as follows-

Table - "A"
Sample mode - "Repet" [1]
Start Display-On
Trigger mode - "NORM"
"LOCAL"
"WORD"

For connection directly to the M6800
Threshold - Var, Adj to 2.4 V
Logic - Pos
For connections to an extended bus
Threshold } to match extender used
Logic }
All other pushbuttons - "out"
Display time-ccw
Column Blanking-ccw
Qualifiers-Q0, hi [2] Q1, off
Trigger word switches-Set to address at which you wish to trigger

[1] If program is not looping or cycling through the selected address, select "Single" and press "Reset" and start your system. The first time the system passes through the trigger point the display will be generated and stored.

[2] If it is desired to observe system activity after the completion of the wait for interrupt instruciton (WAI = 3E), the Q0 qualifier channel, connected to VMA, should be set to the "off" position since VMA is low at the completion of this instruction.

5. DISPLAY INTERPRETATION

In this illustration, system response to an interrupt will be considered. Proper operation is confirmed by a comparison between real time state analysis, figure 1a, and the M6800 cross assembler program listing output, figure 1b.

The MC6800 responds to an interrupt according to the following:

1. Complete current instruction
2. Store microprocessor registers on stack
3. Load program counter with interrupt service routine vector fetched from memory locations FFF8 (PCH) and FFF9 (PCL)
4. Begin execution of interrupt service routine at vectored location

Consider the program listing, figure 1b. Observe the vector routine beginning at location 274C with the

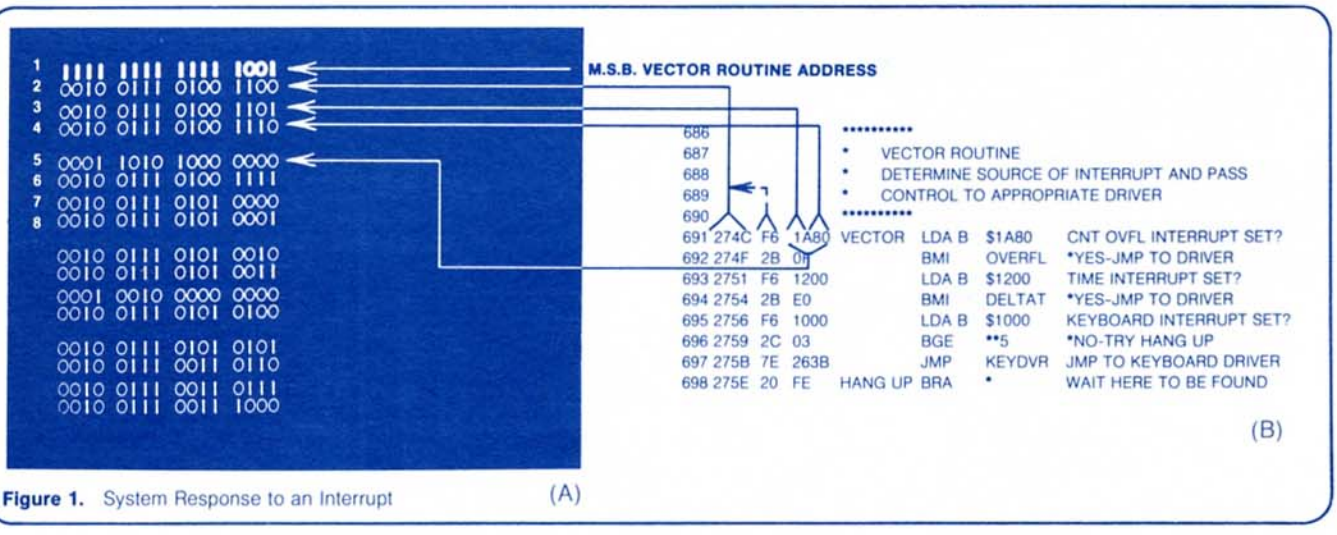


Figure 1. System Response to an Interrupt

instruction LDA B $1A80. This is a three byte instruction: the first byte (F6) is the operation code and the second (1A) and third (80) being a double byte operand, in this case an extended address.

Proper operation of the vector fetch is confirmed by observing the address immediately following the intensified trigger word, FFF9, figure 1a, is 274C. This means that the microprocessor fetched 27 from FFF8 and 4C from FFF9.

The LDA B $1A80 may be confirmed by observing the second, third, and fourth lines of the state analysis photograph. Line 2, 274C, is the fetch of the operation code LDA B (F6) and lines 3 and 4 are the fetch of 1A80, 274D contains 1A and 274E contains 80. The next line, the fifth, shows the address to be 1A80 which implies correct execution of the instruction in the routine. In a similar fashion, each instruction may be shown to have been properly executed.

6. THE MAP

If a tabular display is not presented in the previous step it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to **"map"** (figure 2). Using the Trigger Word switches move the cursor (circle in lower right on photo) to encircle one of the dots on screen. Switch to **expand** and make the final positioning of the cursor—the No Trigger light will now go out and switching back to Table A displays the 16 bit address around that point.

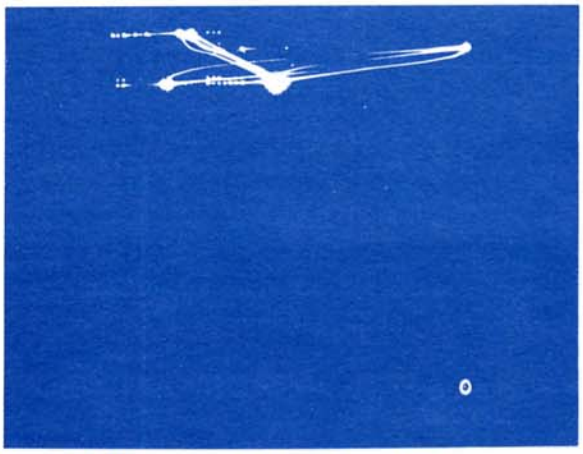


Figure 2. Map Display Shows Entire System Activity.

7. VIEWING ADDRESS, DATA and CONTROLS

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data Bus, Control Bus, or other command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the 16 bit address, 8 bit data bus, and eight other active command signals to be viewed simultaneously. A typical test setup is shown in figure 3. The hookup is easy:

1. Connect data cable between rear panel connectors.
2. Connect trigger bus cable between front panels of instruments.
3. Select Trigger Mode "Bus" and "Word" on 1600A, "Bus" and "Off" on 1607A.
4. Select "End Display", sample mode "Repet", set Delay to "3" and "ON" on both Analyzers, and Table "A&B" on 1600A.
5. Select threshold and Logic Polarity on 1607A to be the same as the 1600A.
6. Leave all other pushbuttons out.
7. Set Column Blanking to display 10 columns on the 1607A.
8. 1600A data and clock inputs connected for address as described in Part 3.
9. Set Q0 hi and Q1 off (or as in Note 2 in Part 4).
10. Connect data and clock inputs for 1607A to the MPU as follows:

    a-1607A Data inputs 0 through 7 to D0 through D7 in order.

    b-1607A Data input 8 to R/W Pin 34.

    c-1607A Data input 9 to NMI Pin 6.

    d-Q0 to 5 VMA.

    e-Q1 to 34 R/W.

    f-Clock to 37-ϕ2.

    g-Grounds to appropriate point(s).

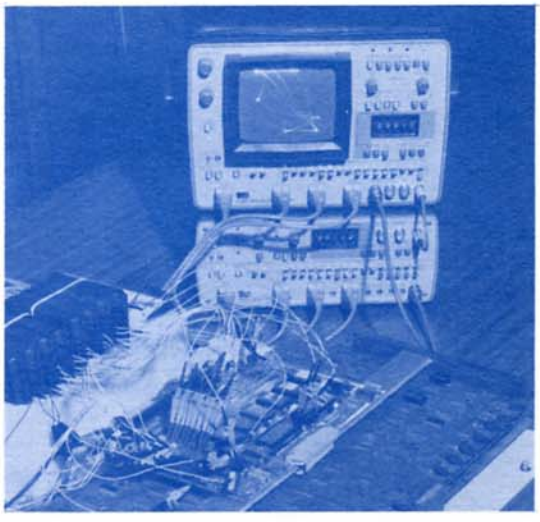


Figure 3. Typical Test Set-up of 1600A and 1607A for displaying up to 32 Bits of Information

8. DISPLAY INTERPRETATION of ADDRESS and DATA BUSES, READ/WRITE, and $\overline{IRQ}$ LINES

As an amplification of the previous example it is possible to investigate the interrupt sequence discussed in section five of this note.

Using End Display triggering and Digital Delay it

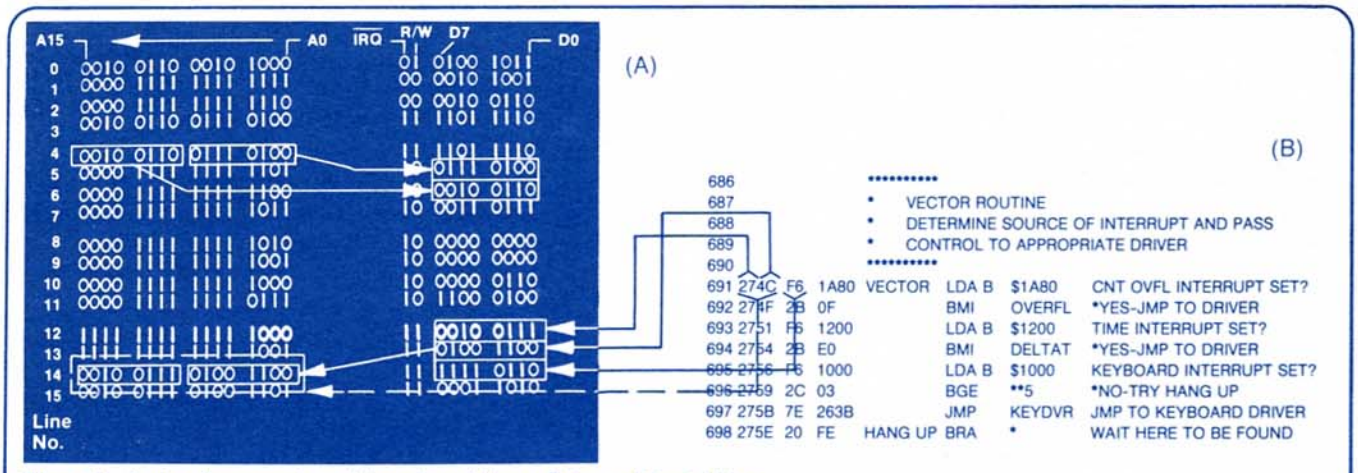


Figure 4. System Response to an Interrupt on Address, Data, and Control Lines.

is now possible to confirm exact system operation with respect to interrupt response as noted in points 1 through 4 of section five.

With reference to lines 0 thru 2 of figure 4a observe that the $\overline{IRQ}$ line is low for three clock periods which signals the microprocessor to begin executing an interrupt service operation.

Confirmation that the microprocessor completed the current instruction is shown in lines 3 and 4 of figure 4a.

Similarly it can be shown that the microprocessor saved the internal registers on the stack by an examination of lines 4 through 11. Line 4 shows the completion of the current instruction at location 2674. Line 5 shows the least significant byte of this address (74) being written into location 0FFD while the Read/Write line is low or in the "WRITE" mode. Line 6 shows the analagous operation for the most significant byte of the program counter (26) being written into location 0FFC.

This process is continued until all registers have been stored on the stack as shown in figure 5.

You can see that seven stack locations are required to save the microprocessor status which may be confirmed by lines five through eleven inclusive, of figure 4a.

As discussed in section five, the microprocessor then reads memory locations FFF8 and FFF9 to set the interrupt service vector. Observe that the program listing, figure 4b, defines this to be 274C which means memory location FFF8 must contain the data 27 and FFF9 must contain 4C.

This is confirmed by lines 12 and 13 of figure 4a. Also observe that fetch was executed properly as the next address following FFF9 is 274C (line 14). In addition, the data at location 274C is F6, figure 4b, which corresponds with the program listing.

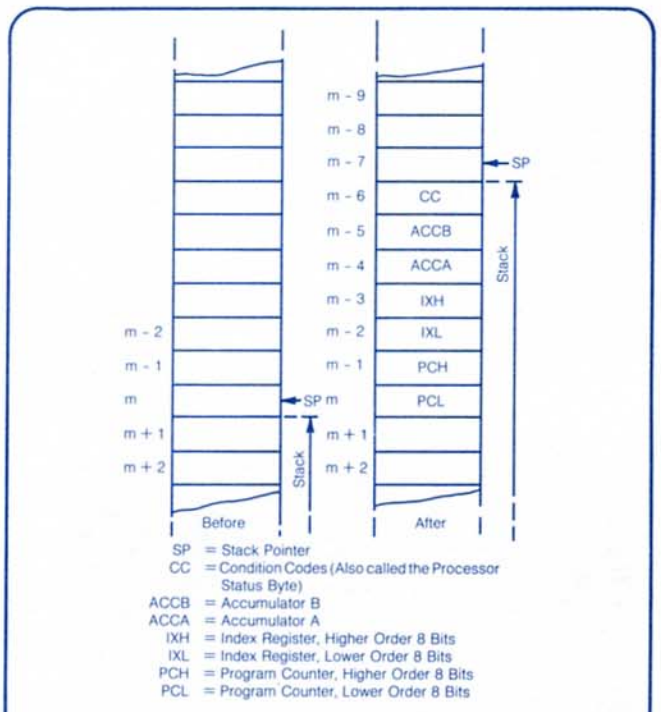


Figure 5. Saving the Status of the Microprocessor in the Stack.

9. CONCLUSION

From the forgoing examples it may be concluded that efficient troubleshooting of the Motorola M6800 microcomputer system is expedited by two factors: **First:** the availability of the program listing as produced by M6800 cross assembler, which is the definitive document of program execution and; **second:** the availability of real time Logic State Analysis to display actual system operation for rapid error detection and correction.

Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Calls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A).
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
167-8 Stable Displays of Disc System Waveforms Synchronized to Record Address (1620A).

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