Saving Time with Multiple-Channel Signal Integrity Measurements

Application Note 1382-8

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Who Should Read This Application Note?

Digital designers in R & D who design complex, high-speed digital circuits (ex. printed circuit boards and integrated circuits) for the computer and communications industries.

New Challenges for System Designers

Three trends converge to create decreased confidence in signal integrity in digital systems.

Increasing Signaling Speeds

Moore's law enables designers to pack more gates onto each chip that run at higher clock rates. To take advantage of the resulting increases in silicon performance, the system designer must seek innovative ways for chips to communicate faster with one another and with the rest of the world. Today's most successful innovations take the form of higher clock speeds and more complex protocols. The higher bus speeds result in ever-shrinking data valid windows.

Decreasing Amplitudes

To increase frequencies without increasing slew rates or power consumption in direct proportion, designers turn to smaller signal amplitudes. Smaller amplitudes translate to reduced noise margins.

Increasing Complexity

System complexity continues to grow exponentially. This results in more buses with more high-speed signals, which translates into more chances of signal integrity problems.

Complex protocols, varying data payloads, and multiple operating modes create more opportunities for signal integrity to be affected by pattern-dependent jitter and delay, and for simultaneous switching noise to eat up time and voltage margins.

Shrinking Schedules

At the same time, time-to-market pressure on development schedules has increased. The designer is left with less time to validate signal integrity.

A New Tool in the Signal Integrity Tool Kit

Eye scan is a new tool in the designer's bag of tools for signal integrity validation. It enables digital circuit designers to save time validating signal integrity in complex, high-speed designs while at the same time gaining confidence in signal integrity. The purposes of this application note are as follows:

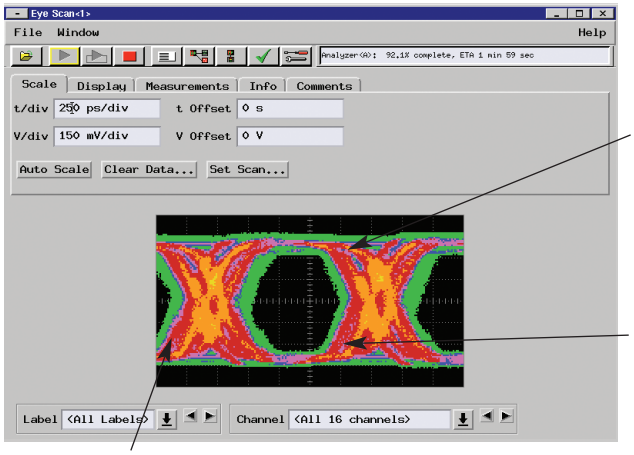
- Introduce the concept of eye scan and explain what it does.
- Show how you can use eye scan to save time while building confidence.
- Help you use eye scan most effectively.
- Provide examples of the expediency of eye scan.

In the eye scan mode, the Agilent 16760A logic analyzer scans all incoming signals for activity in a time range centered on the clock and over the entire voltage range of the signal. The results are displayed in a graph similar to an oscilloscope eye diagram.

Eye scan examines regions of time and voltage for signal transitions that occur. The time regions are defined relative to active clock transitions in the user's system.

The scan proceeds first along the time axis. When the user-specified range of time has been scanned, the threshold voltage is incremented and the time range is scanned again at a new threshold. This is repeated until all time and voltage regions have been scanned.

The user can adjust the scan range and resolution in both time and voltage.



Time and voltage margins are displayed similar to an oscilloscope eye diagram on a logic analyzer, on hundreds of channels.

The horizontal axis represents time and the vertical axis represents voltage, just like an oscilloscope.

Display colors correspond to the amount of signal activity detected.

Figure 1. With eye scan, time and voltage axes are scanned for signal transitions that occur.

A New Tool in the Signal Integrity Tool Kit (continued)

Eye scan provides three options for viewing signals:

- All channels on a bus or multiple buses can be overlaid on the display.
- Individual channels can be highlighted in the composite display.
- Signals can be examined individually.

In addition, results can be viewed for each run individually, or results from multiple runs can be superimposed on the screen.

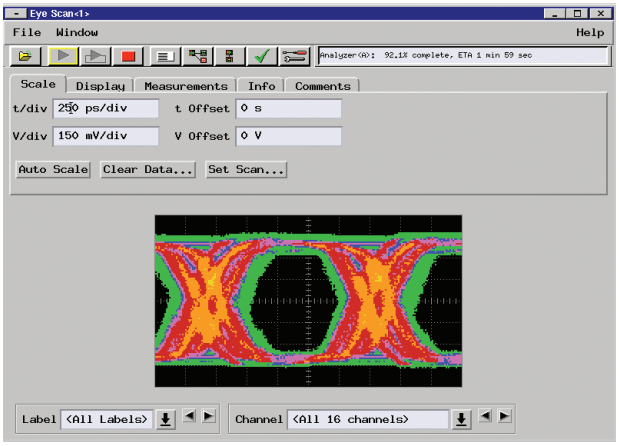


Figure 2. By viewing all signals on a bus or multiple buses overlaid, you can quickly confirm that all signals meet specifications.

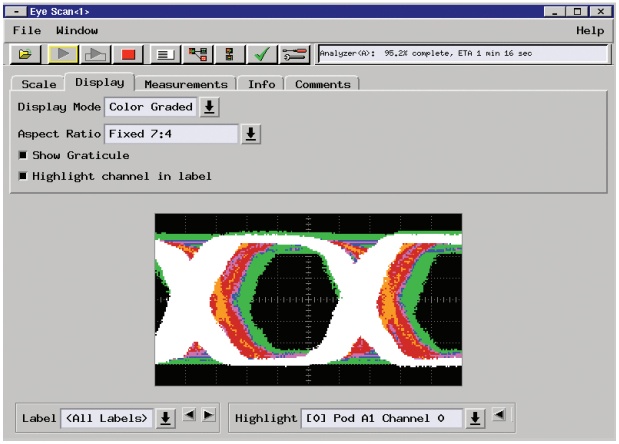


Figure 3. Quickly identify non-compliant signals by highlighting individual channels.

A New Tool in the Signal Integrity Tool Kit (continued)

By selecting the option "Accumulate results from run to run," you can view the results of multiple runs superimposed on the display. This could be useful if, for example, you wanted to vary the power supply voltage in the target system in several increments and then view the worst case eye opening for all power supply settings in one view. In this case, you would set the power supply voltage to a starting level and run eye scan. Then you would increment the power supply voltage and run eye scan again. After running eye scan at all the power supply settings in the test range, you could see the worst case eyes for the whole test on the display.

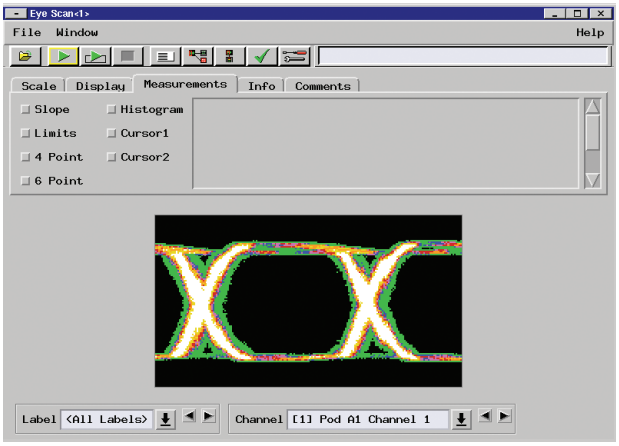


Figure 4. Examine individual signals one at a time.

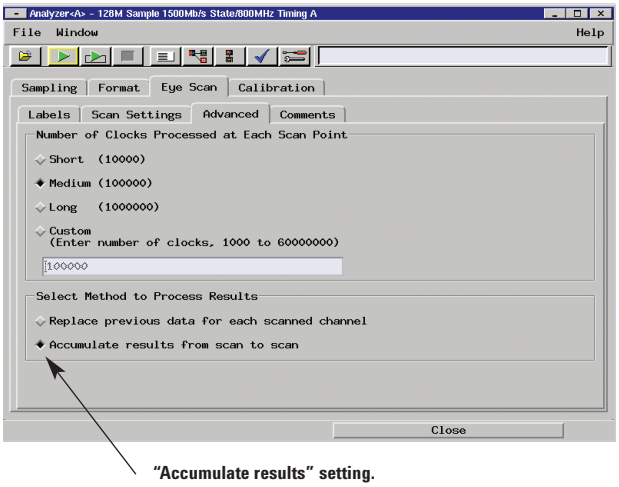


Figure 5. Accumulate results on the display.

Eye Scan as Part of a Process

Eye scan complements and supplements other Agilent measurement tools in the overall signal integrity assurance process. Table 1 lists various measurement tools related to signal integrity and the roles they play.

Vector network analyzers (VNA) and time domain reflectometers (TDR) are used to measure circuit parameters. These parameters are then used to develop accurate models and to verify model accuracy. Simulators use these models to predict circuit behavior.

Oscilloscopes have traditionally been used to characterize and validate the signal integrity behavior of prototype circuits.

Eye scan enables you to measure signal integrity behavior on tens, or even hundreds, of signal nodes much more quickly than an oscilloscope. You can acquire comprehensive signal integrity information on all the buses in a design, under a wide variety of operating conditions, in minimum time. The end result is greater confidence that the design meets your signal integrity goals.

If eye scan identifies problems, you may then use an oscilloscope to investigate the nature or cause of the violation in more detail.

Tool	Role
Vector network analyzer (VNA)	Model development, model verification
Time domain reflectometer (TDR)	Model development, model verification
Oscilloscope	Characterization, validation, troubleshooting
Eye scan	Validation

Table 1.

Saving Time

The time-consuming portion of eye diagram measurements with an oscilloscope is primarily dominated by connecting and moving probes. Only four connections can be made at a time, so to measure hundreds of nodes requires moving the probes hundreds of times. Some engineering teams spend days to months making scope measurements on prototypes for the purpose of margin validation.

With eye scan, the connection is instantaneous (assuming the connector has been designed into the board).

The time spent making the measurement depends on a number of variables which are under the user's control. Dominant variables include:

- The measurement duration, which can be set to any value from a few measurements at each time and voltage region to millions.
- The time range and resolution.
- The voltage range and resolution.
- The number of channels measured simultaneously.

Effect of Resolution
As you can see from table 2, the measurement time is strongly affected by the resolution. In the examples in the table, in column one, there are 30,000 regions to be examined. The voltage is scanned from -600 mV to +600 mV, a scan range of 1.2 V, in 10 mV steps, for a total of 120 steps. The time is scanned from -1.25 ns to +1.25 ns, a total range of 2.5 ns, in 10 ps steps, for a total of 250 steps.

120 voltage steps ×
250 time steps = 30,000 regions

In the remaining examples, the number of regions is reduced to 1/4 of that number, 7500 regions, by doubling the size of the voltage and time steps. Comparing column one to column two, where everything is the same except for time and voltage resolution, you can see that the time is reduced by a factor of 6.7 just by reducing the resolution slightly in each axis. The reduction is greater than a linear factor of four, which you might expect, because some of the measurement time is determined by processing time in the computer.

Effect of Number of Pods
Comparing column two to column three illustrates the difference between one pod (16 channels) and two pods (32 channels). The analyzer only scans one pod on a module at a time, and the increased size of the data set causes the time increase to be nonlinear.

Effect of Number of Clock Cycles
Comparing columns two and four in the table highlights the difference in measurement time as a function of the number of clock cycles examined at each time/voltage point. As you can see, the time does not increase proportionally to the number of clock cycles. With ten times as many clock cycles, the elapsed measurement time only increased by a factor of 3.33.

Effect of Number of M odules
If two or more 16760A modules are coupled together, all the cards run simultaneously in parallel. So five cards will theoretically take only slightly more time than one card.

However, eye scan can generate huge sets of data. Evaluating a large number of channels on multiple cards at high time and voltage resolution can generate a sufficiently large amount of data to cause the system computer to spend a lot of time swapping data on the hard drive, which will substantially lengthen the measurement time. For this reason it may be more time-efficient to break this type of measurements up into groups of channels.

Number of channels	16 (on one pod) 16 (on one pod)	16 (on one pod)	32 (one module)	
Voltage resolution	10 mV	20 mV	20 mV	10 mV
Voltage scan range	–600 mV to +600 mV	–600 mV to +600 mV	–600 mV to +600 mV	–600 mV to +600 mV
Time resolution	10 ps	20 ps	20 ps	20 ps
Time scan range	–1.25 ns to +1.25 ns	–1.25 ns to +1.25 ns	–1.25 ns to +1.25 ns	–1.25 ns to +1.25 ns
Duration (number of clocks)	Medium (400 K)	Medium (400 K)	Medium (400 K)	Long (4 M)
Total time	20 min, 30 sec.	3 minutes, 0 sec.	15 min, 0 sec.	10 min, 0 sec.

User Adjustments

Using eye scan wisely and effectively requires paying attention to a number of variables. This section will discuss the following key variables:

- Resolution
- Range
- Number of clocks

Resolution and Range

Resolution and range determine the number of individual cells of time and voltage that must be examined, which in turn dominates the measurement time.

If you set the time range to scan just one eye (data valid window), this will yield as much information as scanning several eye intervals. The smaller the range, the shorter the measurement time.

Likewise, the voltage scan range should optimally be set to cover just the active range of the signal. Again, the smaller the voltage scan range, the quicker the measurement time.

If you're not sure of the voltage range of the signal, you can use the button "Scan voltage over entire range of signal activity." Eye scan will then automatically detect the upper and lower bounds of signal activity. This may take a bit longer than if the scan range were set precisely to the optimum, but it will probably save you time on the first run.

Number of Clocks

As shown in table 2 on page 6, the measurement time does not increase linearly with the number of clocks. Examining more clocks is often a good idea, as it will increase your confidence in capturing infrequent or corner-case signal behavior.

Recommended Practices

To get the most out of eye scan, use it to thoroughly examine all signals, under all the conditions that might influence signal integrity, on multiple prototypes.

For example, if you are designing an edge router, there may be specific data patterns in packets that cause pattern-dependent delay, leading to jitter. You can use the Agilent RouterTester VNA (virtual private network) test solution or the ParBERT 81250 parallel bit error ratio tester to provide varying stimulus patterns, while monitoring eye opening quality with eye scan.

In a computer, there may be data patterns that induce pattern-dependent delay or simultaneous switching noise, that can lead to an unacceptable closing of the data valid window.

You may also want to vary power supply voltage or temperature while monitoring signal integrity using eye scan.

Once eye scan has given you a comprehensive overview of signal integrity, you can then identify trouble situations. You may elect to examine these cases in more detail with an oscilloscope. Or, in some cases, the information from eye scan may be sufficiently diagnostic to identify the cause and solve the problem. For example, skew between two signals can be visualized and measured very quickly using just eye scan.

An example of a case where the oscilloscope and eye scan can work together effectively might be where a connector is suspected of introducing a signal integrity problem. The symptom can be seen by observing the signals at the receiver with eye scan. An oscilloscope can then be used to examine the signals before and after the connector to verify that the connector is introducing the problem.

Spend sufficient time analyzing the placement and design of the probing connectors in your design to ensure that:
a) the connection to the probe connector is not introducing distortions into the signals in your system, and
b) that the signals you are measuring with eye scan are a sufficiently adequate replica of the signals you wanted to measure. Agilent's application note *"Designing High-Speed Digital Systems for Logic Analyzer Probing,"* publication number 5988-2989EN, is a valuable reference (available at www.agilent.com/find/probeguide).

Examples
Bimodal Jitter on an 800 MT/s PRBS Signal

The first example illustrates a measurement of an 800 MT/s PRBS signal with bimodal jitter.

In this and the following examples, eye diagrams viewed on both eye scan and an oscilloscope will be shown side-by-side for comparison. For this reason, only one channel is shown on eye scan. The oscilloscope used in the examples is an Agilent Infiniium 54846A oscilloscope, which has 2.25-GHz bandwidth and an 8-GSa/s sampling rate.

Note the difference in the appearance of the "shoulders" of the distribution in the histogram between the oscilloscope and eye scan. Eye scan uses a log vertical scale, while the oscilloscope uses a linear vertical scale for the histogram. This ends to emphasize the "tails" of the distribution. This makes it easier to visualize how much activity is present in the "tails" of the distribution.

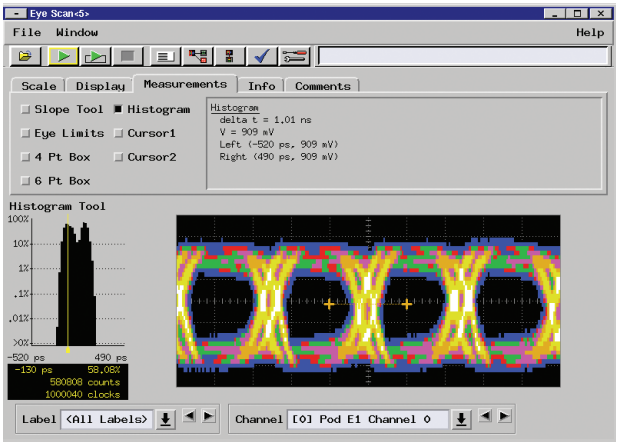


Figure 6. Bimodal jitter, 800 MT/s PRBS signal (Agilent 16760 logic analyzer with eye scan's histogram tool).

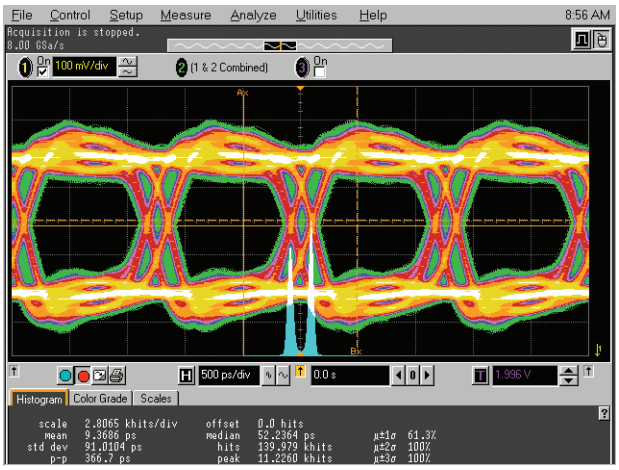


Figure 7. Bimodal jitter, 800 MT/s PRBS signal (Agilent Infiniium 54846A oscilloscope).

Examples (continued)
Noisy 800 MT/s Signal

This example gives a striking illustration of the power of eye scan to quickly identify problems with signal integrity. Figure 8 shows an eye diagram of an 800 MT/s signal acquired using eye scan. The acquisition time was less than one minute.

Figures 9, 10 and 11 show the same 800 MT/s PRBS signal using an oscilloscope with infinite persistence after 5 minutes, 2 hours, and 72 hours.

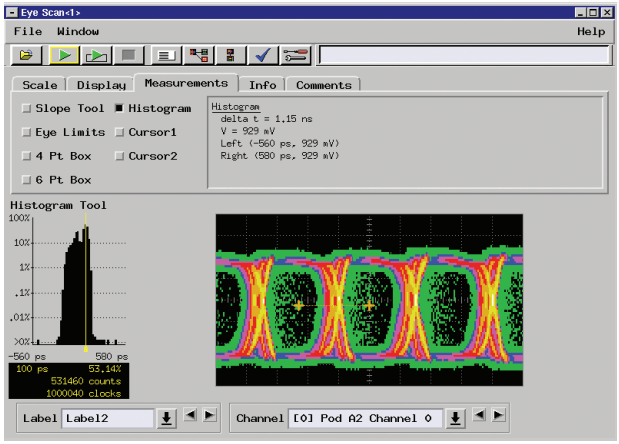


Figure 8. Noisy 800 MT/s PRBS signal (Agilent 16760 logic analyzer with eye scan).

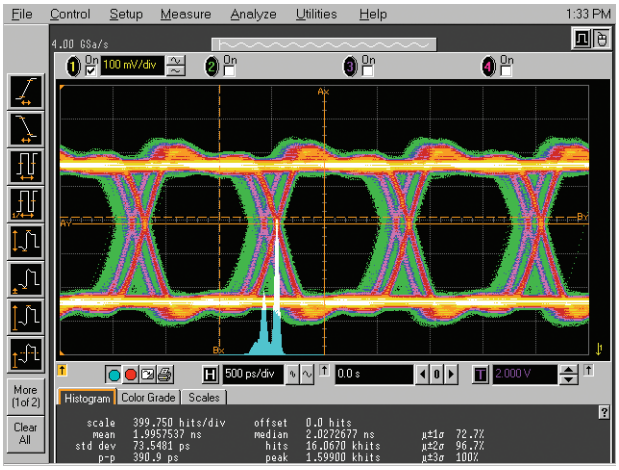


Figure 9. Noisy 800 MT/s PRBS signal (oscilloscope, 5 minutes).

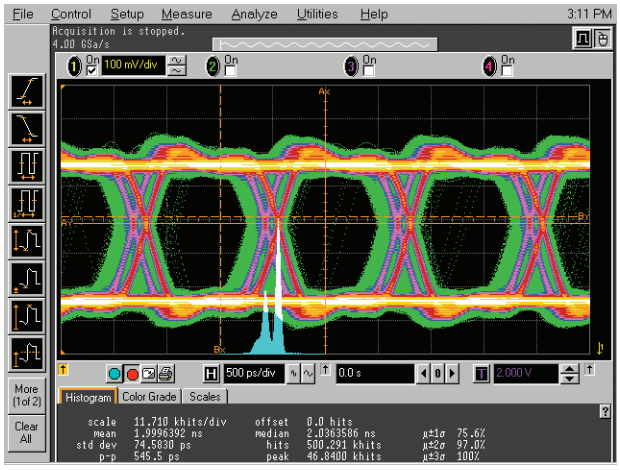


Figure 10. Noisy 800 MT/s PRBS signal (oscilloscope, 2 hours).

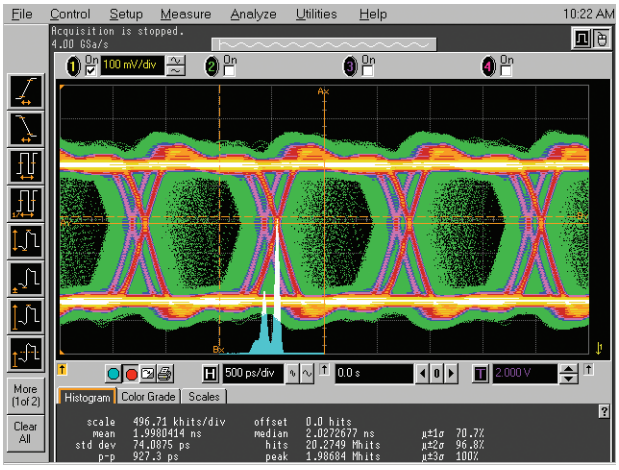


Figure 11. Noisy 800 MT/s PRBS signal (oscilloscope, 72 hours).

Summary

With increasingly faster digital signals in high-speed circuits, digital design engineers are faced with unanticipated signal integrity problems that crop up in the latter stages of the design and development process. The staggering pace of new technology and high-speed innovations is forcing them to get products out faster than ever before to meet customer needs. Ensuring signal quality, as designs get more complex, has become increasingly more challenging, especially with digital edge rates operating at sub-nanosecond levels and getting faster. Designers are working with edge speeds that they have never worked with before and need to pay more attention to things that affect a signal's rise time, pulse width, timing, jitter, and noise content. Even the little things may impact system reliability and the design schedule. To ensure signal quality at these fast edge speeds means understanding analog affects such as cross talk, ground bounce, impedance, and EMI (electromagnetic interference). To do digital design today means effectively dealing with analog characteristics of the digital signals in order to maximize a system's performance. Digital designers are now spending less time simulating and more time in design validation and debug because their design margins are much slimmer now and it is a real challenge to understand and resolve problems.

Agilent helps you meet these challenges with the right information and tools. Agilent can help you understand the strengths of various test tools or validating signal integrity in high-speed digital circuits, and which ones to select for a particular task. Agilent also provides training and tips for dealing with signal integrity challenges. To learn more, log onto:
www.agilent.com/find/signalintegrity

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Related Literature

Publication Title	Publication Type	Publication Number
Agilent 16700 Series Logic Analysis System	Product overview	5968-9661E
Agilent 16702A Logic Analysis Module	Photo card	5988-1665EN

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Product specifications and descriptions in this document subject to change without notice.

Printed in USA March 14, 2002
5988-5409EN

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