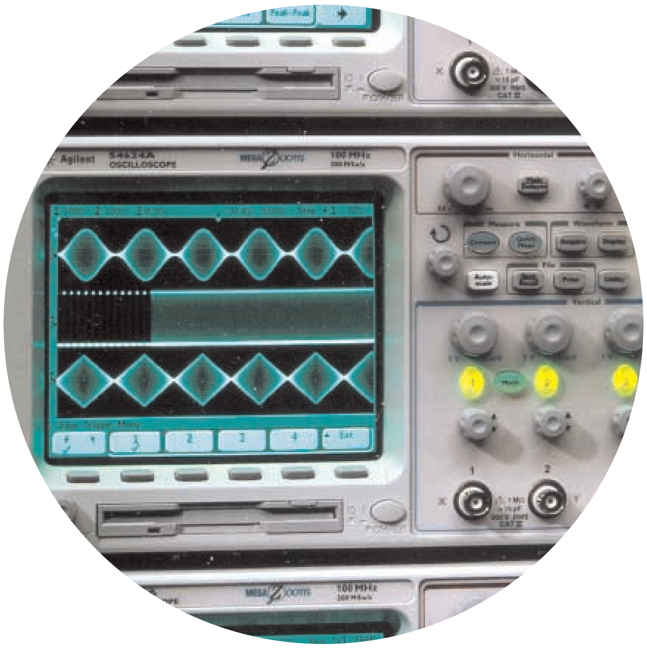
54622D

Agilent MSO and CEBus PL Communications Testing

Application Note 1352



Introduction

The P300 encapsulates the Data Link and Physical layers of the CEBus (EIA-600) standard for power line communications. This standard describes a peer-to-peer, low cost ($3 - $6) networking solution for communication between devices in the home using robust spread spectrum signaling techniques.

Using CEBus power line communication allows products like smart switches and smart outlets to communicate with each other and with higher function devices like home controllers and/or personal computers. For the most part, these devices all need power from the power line to operate and by also using the power line for communication there are no new wires necessary and installation is simplified. Communication on a CEBus PL network has a base rate of 10,000 bits per second and, after various overheads, communicates at an effective rate of between 4,000 and 6,000 bps. On the simple side – CEBus devices like switches and outlets can be used to make 2-way, 3-way, or n-way circuits where the current wiring is insufficient. More sophisticated home control situations are possible using these simple devices and a dedicated smart controller with macros, monitoring, and time scheduling. All with no new wires!

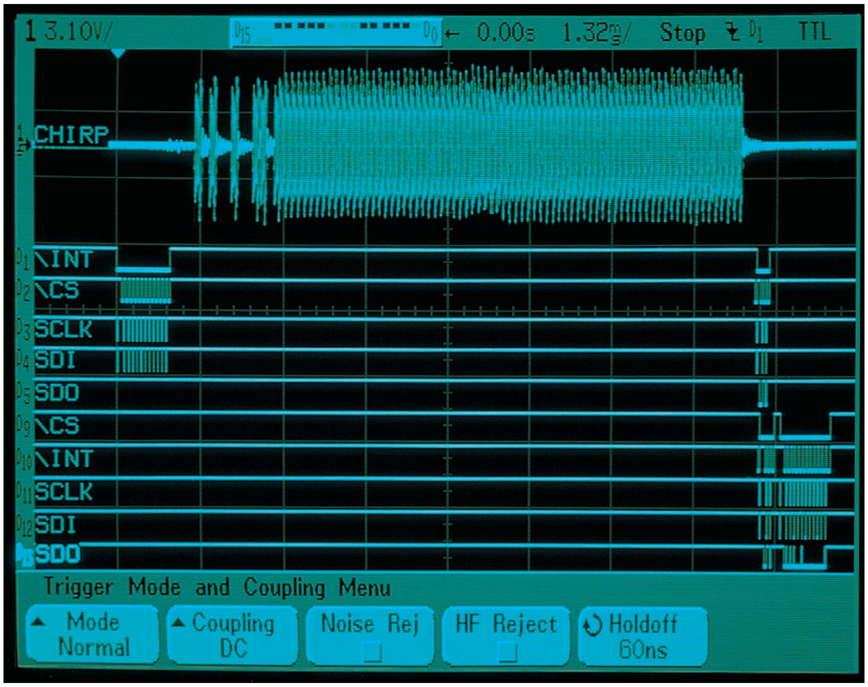


Figure 2. Capture of complete transaction between P300 and host CPU

The Application

The Intellon P300 power line communication coprocessor is normally used with a host processor and a small mix of analog components for signal coupling to the power line. The interface to the host processor is a clocked serial interface with some slightly unusual aspects. Since the CEBus specification defines a peer-to-peer network there are many cases where it is advantageous to view the data going into the data link layer (P300) from the processor side and the analog signals on the "bus" (power line) at the same time.

The test and debug environment is complicated by this mix of analog and digital signals which must be looked at in a time critical manner. There are six digital signals which make up the host processor to P300 interface on the transmit and receive device (total of 12 signals) and the analog signaling path on the power line. In the past I have used a digital scope and a separate logic analyzer to capture and analyze the multitude of signals. This approach works but is complicated by the two instruments having separate time bases, different trigger points, and two sets of (slightly different) controls.

A complete transaction between the P300 and the host CPU can be seen in the above screen shot (Figure 2). The communication between the sending host µC and the sending P300 is on digital lines D1-D5, the spread spectrum data from the power line is shown on the analog trace 1, and the communication between the receiving host µC and the receiving P300 is on digital lines D9-D13.

The 54622D makes this very easy (compared to using two separate instruments) since the time base is now common between the analog and digital channels. This keeps the signals aligned at all times and there is never any confusion due to the two instruments having been adjusted separately to different time/division settings. The signals are easy to label with their data sheet names further reducing confusion. The single instrument works easily with Agilent's IntuiLink software to get the measurement picture into a Microsoft Word® document on your PC (try this with two separate instruments!).

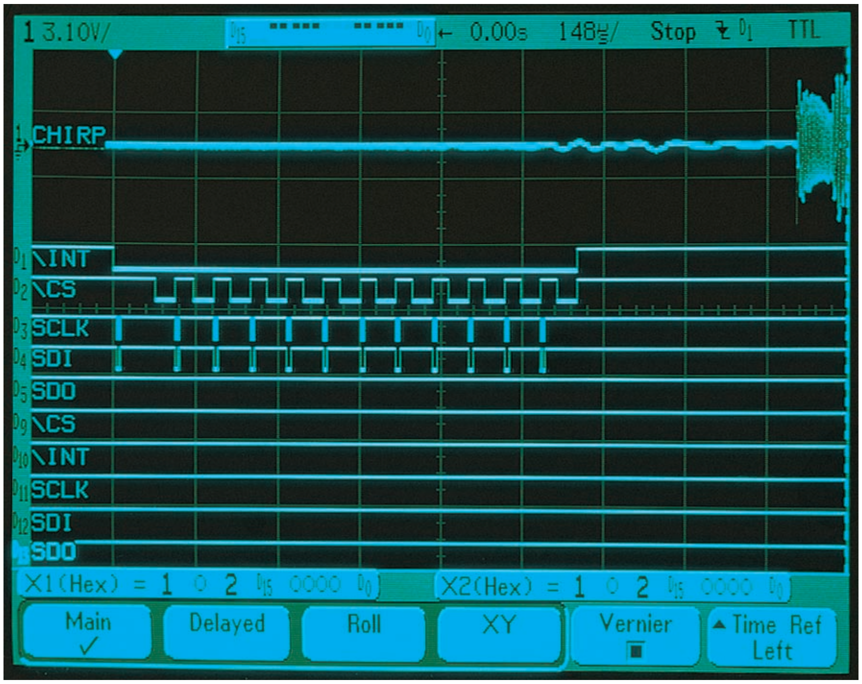


Figure 3. Zoom in on details for analysis

Zooming In on The Signals

The 54622D has a two mega sample storage buffer which is used for the entire screen at trigger time. I use a slow sweep speed to capture the whole waveform as shown in the Figure 2 screen shot. The screen shot above (Figure 3) is from the same trigger event. Once the signals are captured I can zoom in on any portion of any signal of interest including the 500 kHz serial clock (SCLK). Each clock edge and the associated data can be easily seen and analyzed since the 54622D took a sample every 10 ns at 2 ms/div sweep speed. The front panel controls are easy and intuitive and zooming and panning across the signals makes easy work of interface troubleshooting.

Conclusion

Having the 16 channels of logic analysis and the two analog channels available in the same instrument allows me to look at all of the signals and maintain temporal alignment at ALL times. I have never made a measurement mistake with different time bases or incorrect triggers using this instrument. These are common errors using two instruments and can cause a good bit of head scratching. Also – instead of trying to control two instruments simultaneously I can control one display and concentrate on the current measurement challenge.

Figure 4. Five models to satisify your bandwidth, channel count and budget needs

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Model Number	Bandwidth	Sample Rate	Channel Count	Memory Depth	Price
54621A	60 MHz	200 MSa/s	2	2 MB/ch	$2,801
54621D	60 MHz	200 MSa/s	2 + 16	2 MB/ch	$4,031
54622A	100 MHz	200 MSa/s	2	2 MB/ch	$3,403
54622D	100 MHz	200 MSa/s	2 + 16	2 MB/ch	$5,352
54624A	100 MHz	200 MSa/s	4	2 MB/ch	$5,207

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