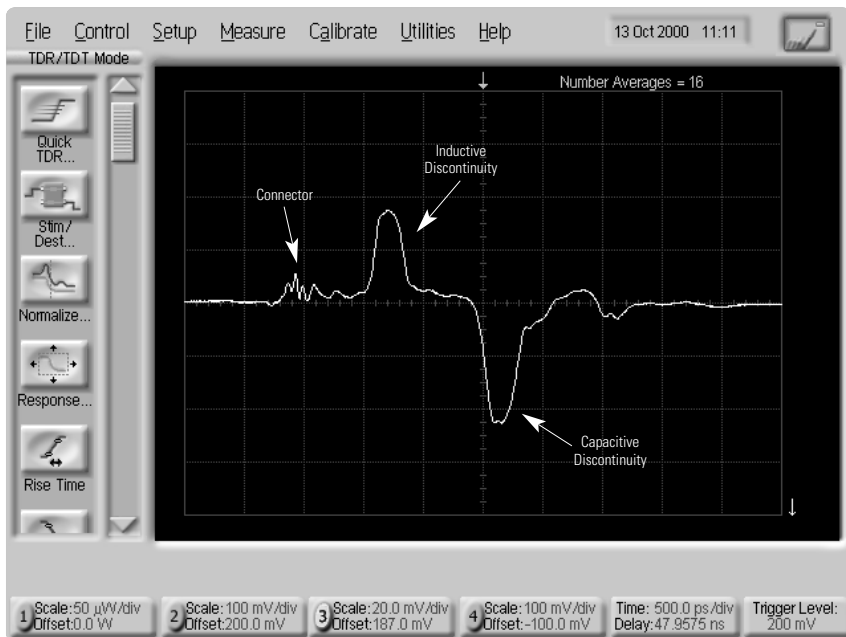


# Evaluating Microstrip with Time Domain Reflectometry

Application Note 1304-1



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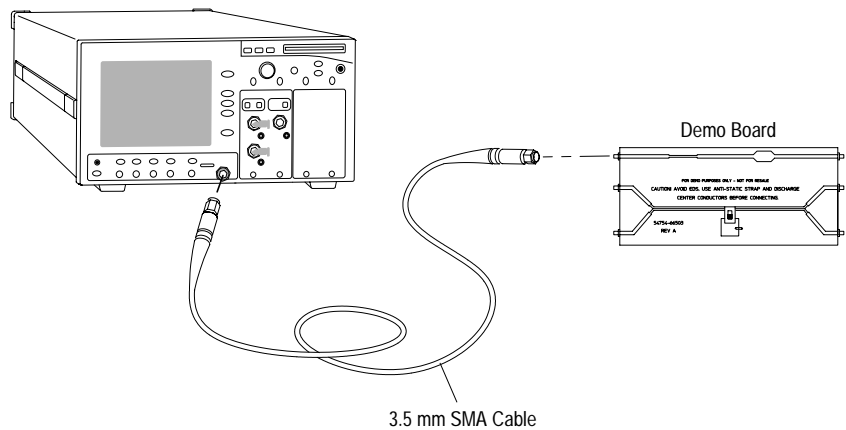
## Introduction

In the world of high-speed digital design, clock rates are increasing at a dramatic pace. Gigabit per second data rates are creating signal integrity problems for printed circuit board structures such as backplanes, microstrip traces and interconnects. While simulation tools allow helpful insights into predicting structure performance, more test and measurement tools are needed to measure and verify the actual response to fast edge speeds. Time Domain Reflectometry is one of the tools used most frequently by digital design engineers to relate physical interconnect structures to such parameters as characteristic impedance, reflection coefficient, propagation velocity and edge effects.

This application note highlights experiments that were conducted on microstrip lines with various geometries. Printed circuit boards were fabricated with stubs and dividers to intentionally cause reflection and crosstalk problems. The intent is to show examples of how to recognize and avoid some common problems associated with high-speed digital design.

## Microstrip Transmission Line Techniques, Evaluated Using TDR Measurements

The time domain reflectometer (TDR) employs a step generator and an oscilloscope in a system which might be described as “closed-loop radar.” Refer to the figure below. In operation, a voltage step is propagated down the coax cable to the device under test (DUT). As an impedance discontinuity is encountered in the DUT, some of the energy is reflected. Both the incident and reflected voltage waves are monitored on the oscilloscope at a particular point on the line.

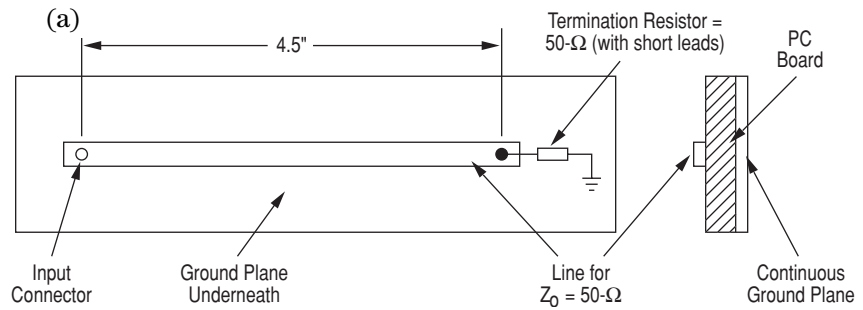


### Time domain reflectometer.

For these examples, the incident voltage setup is a positive edge with an amplitude of 200 mV and a nominal risetime of 40 ps. It is generated from a source impedance of 50-Ω and has an overshoot of  $\leq 5\%$ .

TDR reveals the characteristic impedance of the line under test. It shows both the position and the nature (resistive, inductive, or capacitive) of each discontinuity along the line and signifies whether losses in a transmission system are series losses or shunt losses. An example of a microstrip line evaluated with TDR techniques is shown below:

**TDR Example 1:** Board material: Norplex Type G-10  
 Dielectric thickness:  $h = 0.062$  inch;  
 Copper thickness:  $t = 0.0014$  inch;  
 Dielectric constant:  $\epsilon_r = 5.3$ .



**Figure 1A. Microstrip circuit example 1**

A printed circuit board was fabricated as shown in Figure 1A to the dimensions specified above. Figures 1B and 1C show the incident and reflected waveforms observed with the TDR. The vertical scale can be calibrated in terms of voltage (mV), reflection coefficient ( $\rho$ ) or impedance (ohms). The horizontal scale can be expressed in either time or distance. The equation for characteristic impedance of the line is:

$$Z_{\text{line}} = \left( \frac{1 + \rho}{1 - \rho} \right) \cdot Z_{\text{reference}} \quad (1)$$

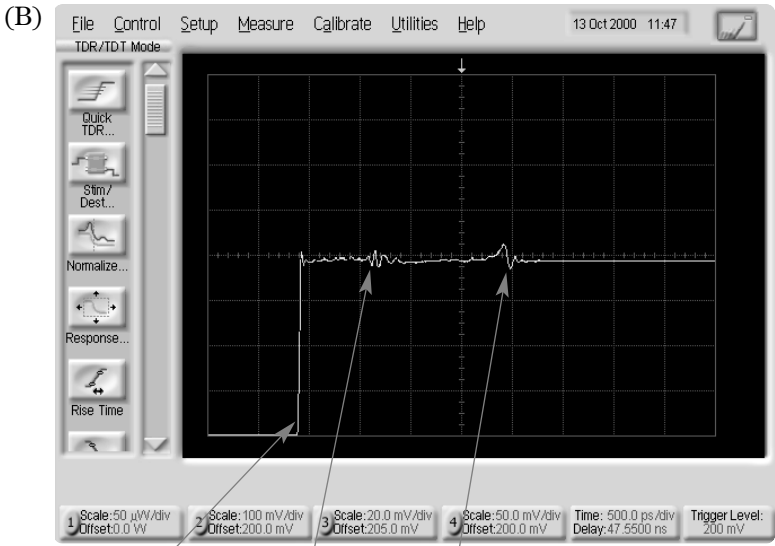
where:  $Z_{\text{line}}$  = characteristic impedance of the line under test,

and  $Z_{\text{reference}}$  = impedance of the known line.

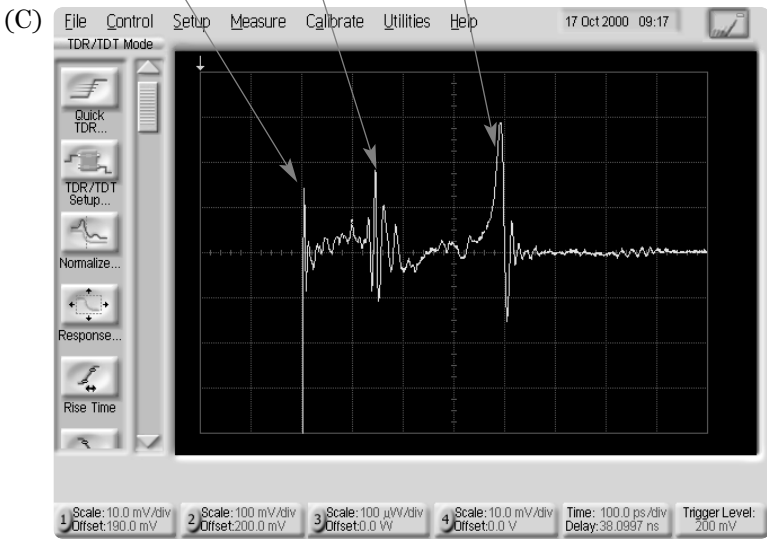
The mean level of the reflected waveform due to the line has a  $\rho = 1.08\% = 0.0108$  (see Figure 1B). Substituting values into equation 1 permits calculation of the line impedance:

$$Z_{\text{line}} = \left( \frac{1 + 0.0108}{1 - 0.0108} \right) \cdot 50\text{-}\Omega = 51.1\text{-}\Omega, \quad (2)$$

which agrees closely with the measured value shown in Figures 1B and 1C.



Incident Step    Connector    50- $\Omega$  resistor

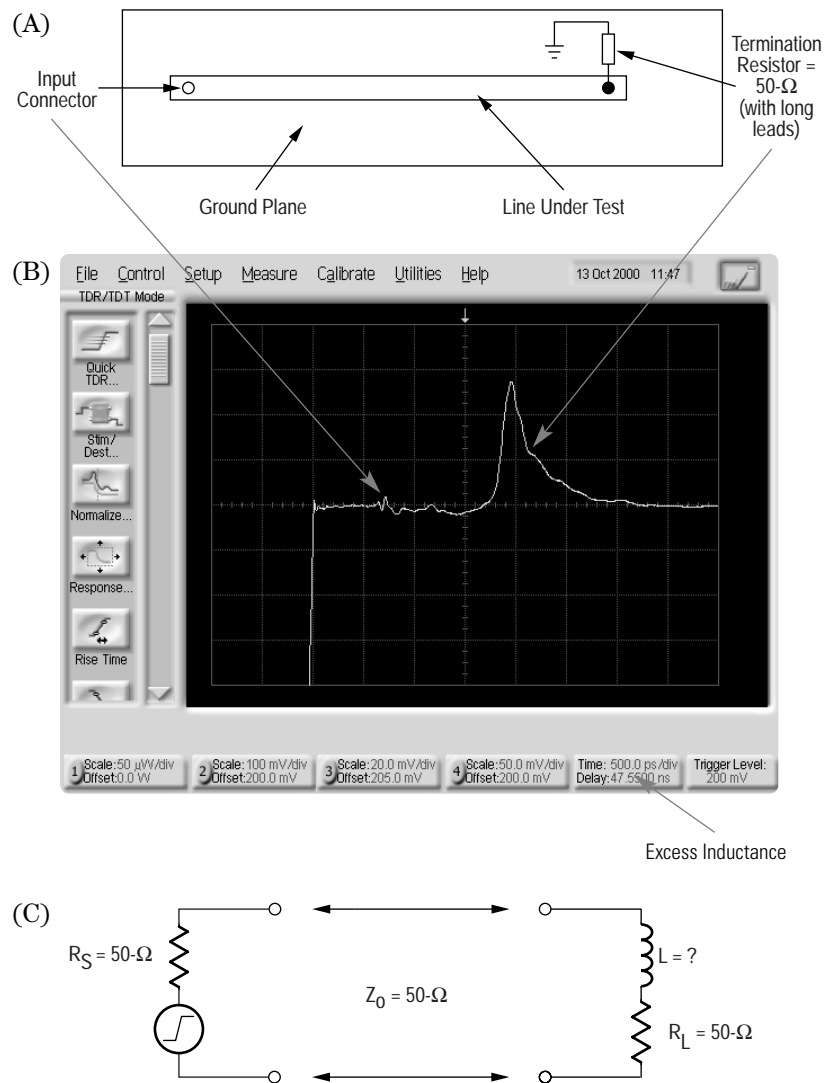


**Figure 1B. TDR determination of line characteristic impedance.**

**Figure 1C. Same as 2B with expanded vertical scale.**

**TDR Example 2:** This example indicates how to measure the effect of long resistor leads using TDR (same as Example 1, except long resistor leads). Figure 2A shows the construction of a microstrip line terminated with a resistor having 1-inch lead lengths. The reflection coefficient determined from the TDR measurement is 71% (see Figure 2B). The risetime at the input to the line is a nominal 40 ps, but it is lengthened to about 80 ps as the wavefront reaches the termination resistor.

To measure the excess inductance on the microstrip line due to the resistor leads, the excess reactance function can be used. Turn on the markers by pressing the buttons below the screen. The markers used for TDR are the first and third buttons from the left hand side of the front panel. On the marker tab, excess reactance is displayed in the lower right corner. By comparing the TDR waveform in Figure 2B to that of Figure 1B, one can see how crucial a good termination can be to reducing unwanted reflections.

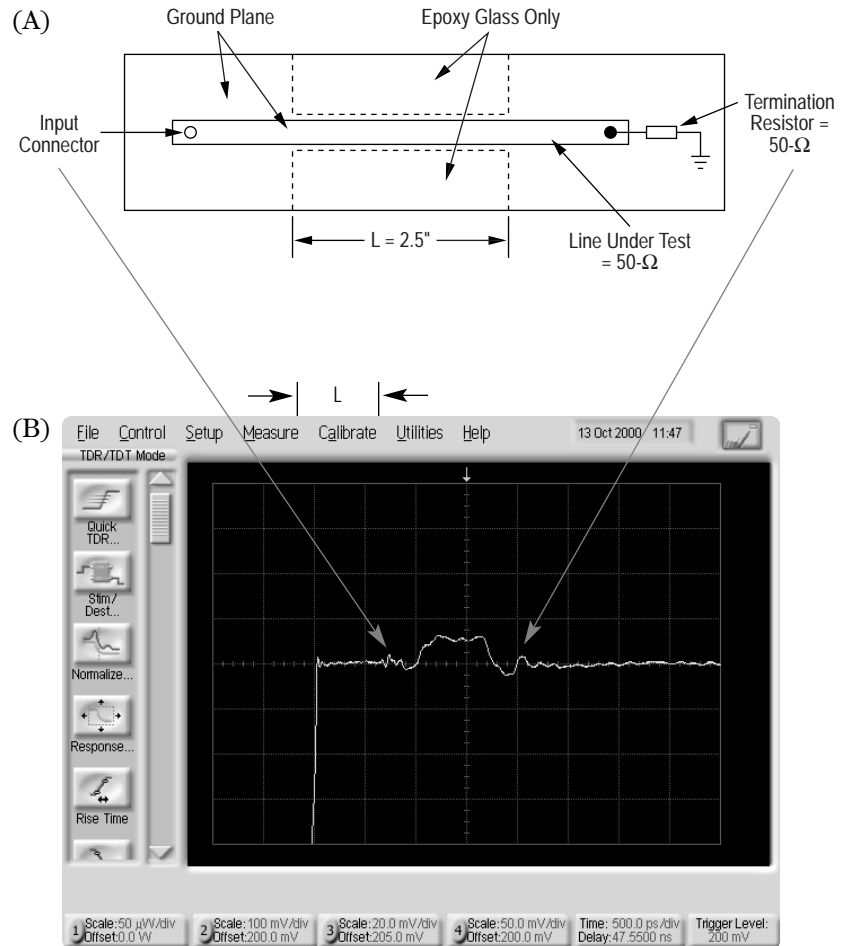


**Figure 2. Effects due to termination resistor leads**

**TDR Example 3.** This experiment shows the effects of a ground plane on the characteristic impedance of microstrip lines. Figure 3 illustrates what happens when the ground plane width under the transmission line abruptly drops to the width of an active line. The TDR waveform shows that a reflection of 12.4% occurs due to this discontinuity in the ground plane.

Using markers, the impedance of the 2-1/2 inch-long strip can be measured to be 64.2-Ω. As a check, the impedance can be calculated using equation 1:

$$Z_{\text{line}} = \frac{1 + 0.124}{1 - 0.124} \cdot 50 = 64.2\text{-}\Omega. \quad (3)$$

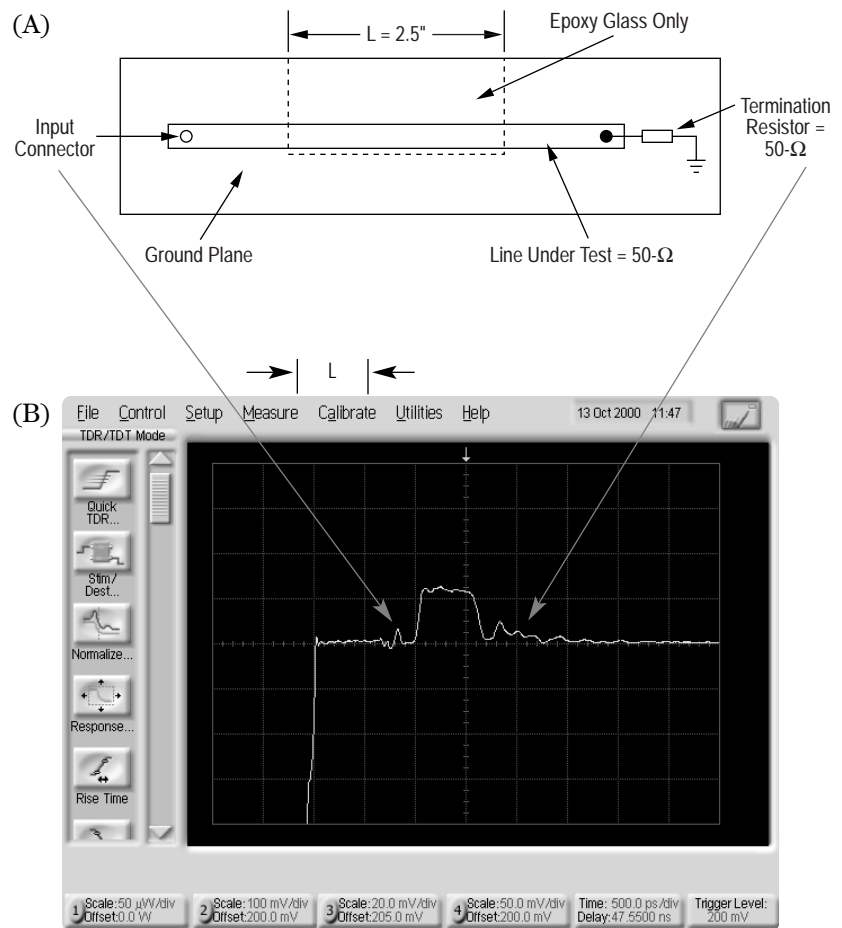


**Figure 3. Effects of ground plane discontinuities.**

**TDR Example 4.** A related experiment was performed to find the reflection due to a ground plane near, but not directly under the active line. The test configuration and test results are shown in Figure 4. As indicated by the TDR measurement, the reflection is 36%. This corresponds to an impedance of 106-Ω.

$$Z_{\text{line}} = \frac{1 + 0.36}{1 - 0.36} \cdot 50 = 106\text{-}\Omega. \quad (4)$$

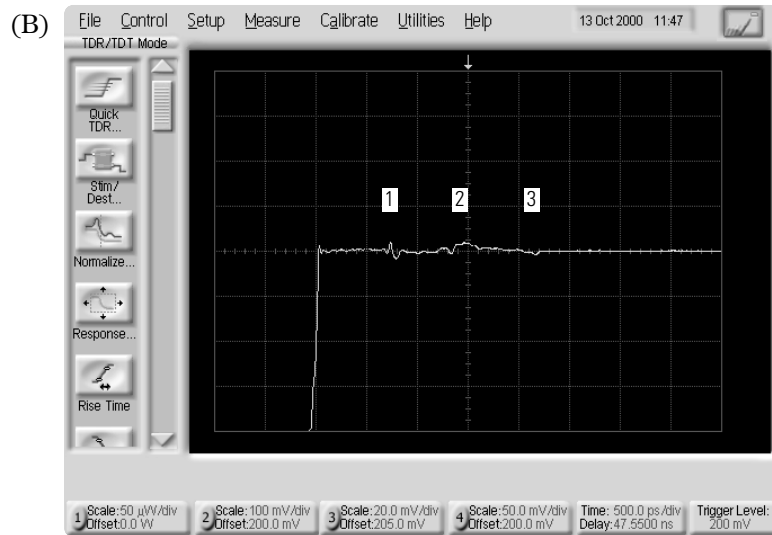
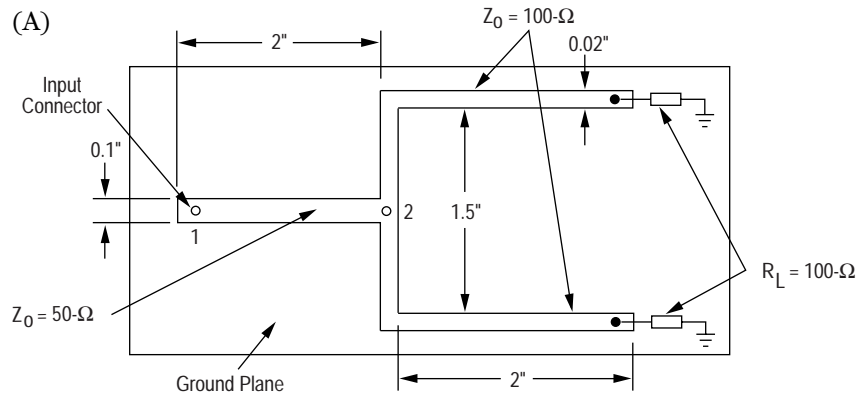
The reason for the reflection is the change in the characteristic impedance resulting from the ground plane not being under part of the active line. In such a region, capacitance of the line to ground decreases while the inductance of the line increases, the net result being a higher characteristic impedance.



**Figure 4. Effects for ground plane discontinuity.**

**TDR Example 5.** Another measurement was performed to observe the reflections due to the use of a hybrid divider. The construction of the microstrip board used is shown in Figure 5. Note that the 50-Ω line branches out into two 100-Ω lines. A reflection of 4 percent is observed where the junction occurs at point 2.

Note that no impedance mismatch appears due to crosstalk between the two 100-Ω branches, because of their wide separation.



**Figure 5. Hybrid divider.**

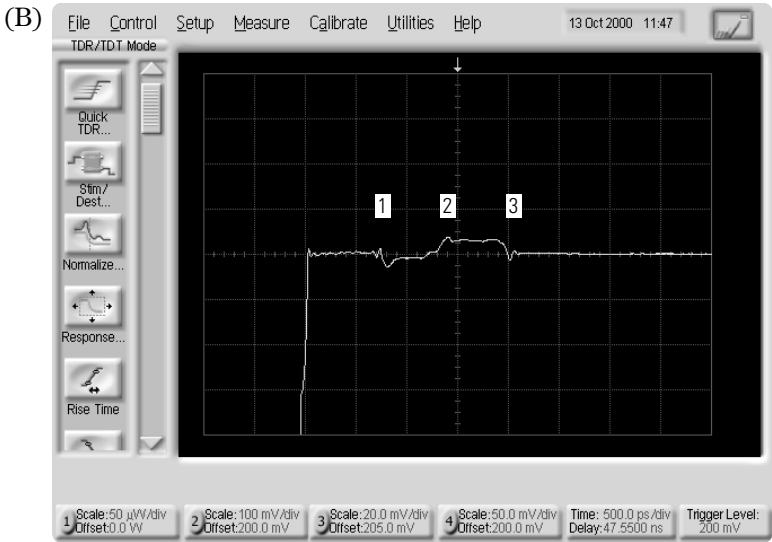
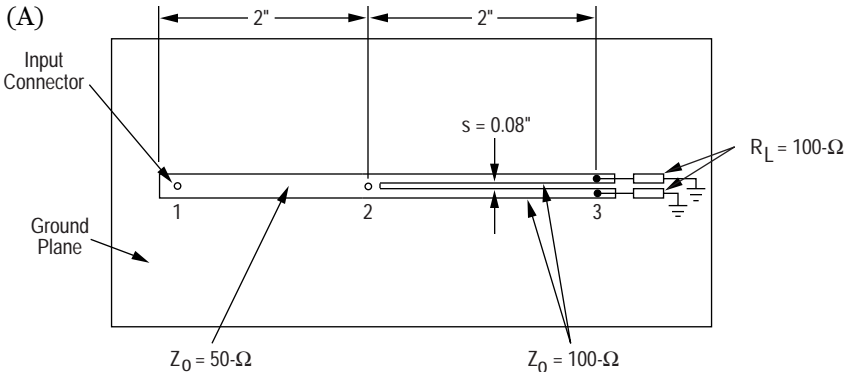


**TDR Example 6.** Figure 6 shows a similar hybrid divider to example 5, but now the two 100-Ω lines have been brought close together. The reflection at point 2 is now equal to 8.4% arising from the cross coupling of the two lines.

Even mode or odd mode characteristic impedance ( $Z_{oe}$  or  $Z_{oo}$ ) can be considered to exist in a circuit with crosstalk. One term,  $Z_{oe}$ , is due to the strips being at the same potential and carrying equal currents in the same direction. The other,  $Z_{oo}$ , is due to the strips being at equal but opposite potentials and carrying equal currents in opposite directions. The backward crosstalk voltage,  $V_B$ , on a passive line is:

$$V_B = \left( \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \right) E_1 \quad (5)$$

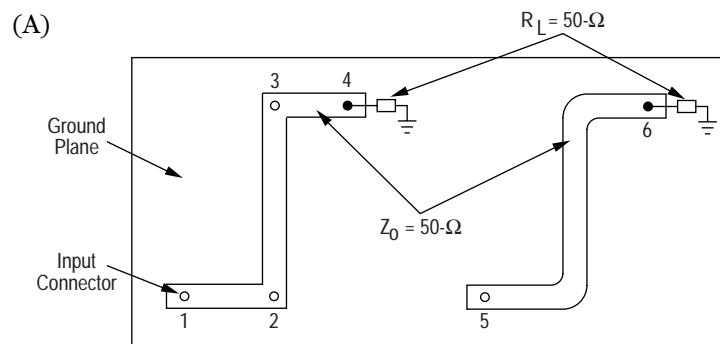
where  $E_1$  is the signal propagating down the active line. The backward crosstalk voltage shown in Figure 6B at point 2 is equal to 8% of the incident voltage  $E_1$ . Since both lines are active, the crosstalk due to one active line is 4% of  $E_1$  for a spacing of 80 mils.



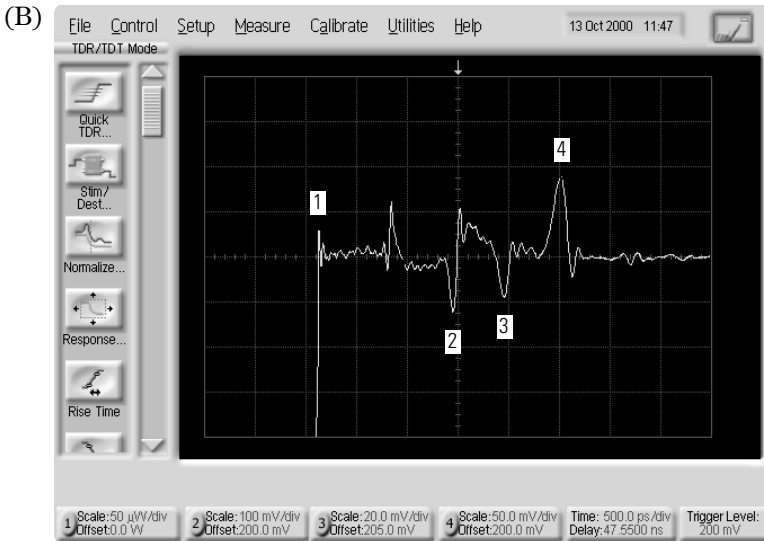
**Figure 6. Hybrid divider with crosstalk problem.**

The mutual inductance and capacitance between two lines are used to determine the crosstalk coefficient. Forward crosstalk is normally much smaller than the backward crosstalk on microstrip lines—except for very long lines (>5 feet). Forward crosstalk does not exist at all on strip lines, since they are made with a homogeneous dielectric medium, so that the inductively and capacitively induced currents cancel.

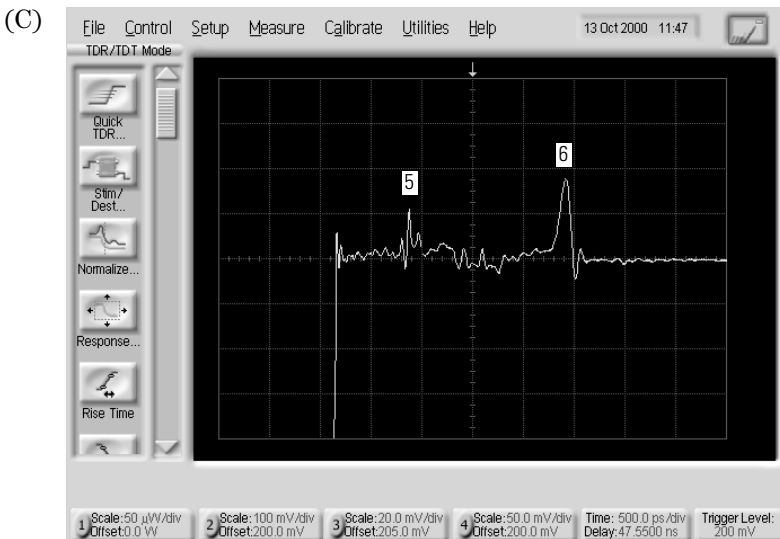
**TDR Example 7.** In very high-speed systems, the exact shape of a line can be important if reflections are to be kept to a minimum. The arrangement shown in Figure 7A has been used to investigate the behavior of two different line shapes. For one line, corners are sharp. This causes the width of the line to be larger at corners than elsewhere. Figure 7B shows that a  $-7.5\%$  reflection occurs at points 2 and 3 due to the lowered characteristic impedance at the corners. For the other line, the corners are rounded to produce a constant line width. Figure 7C shows that a constant line impedance exists for the second line. Note that an inductive reflection, as discussed before, does occur at the end of the line due to the inductance of the resistor. It is desirable to have smooth, rounded line edges and constant line widths when designing transmission lines for high-speed systems. Resistor leads should be kept short to minimize termination inductance.



**Figure 7A. Reflections caused by signal-line shape variations.**



**Figure 7B. Reflections caused by signal-line shape with sharp corners.**



**Figure 7C. Reduced reflections caused by signal-line shape with rounded corners.**

In conclusion, this application note has shown the strong relationship between microstrip geometry and time domain reflectometry measurements. As the reader becomes more familiar with recognizing printed circuit board structures and their corresponding TDR signatures, high-speed digital circuits can be designed with a minimum of reflections due to impedance discontinuities. As digital speeds continue to climb to unprecedented levels, it is clear that signal integrity will play a more important role in the design and layout of printed circuit boards and their related structures.

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