Errata

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HP References in this Application Note

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LOGIC
TIMING
MEASUREMENTS

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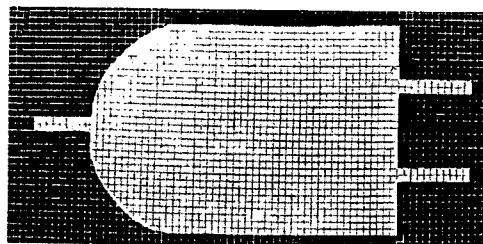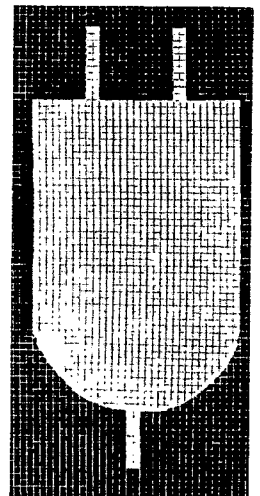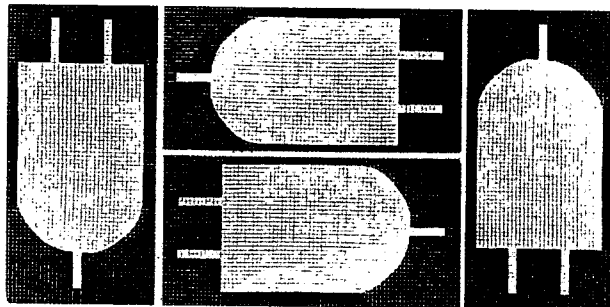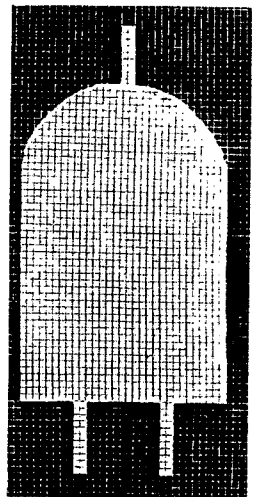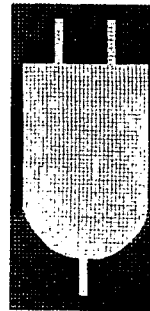
APPLICATION NOTE 129

LOGIC TIMING MEASUREMENTS

Digital logic designers and users have ever increasing requirements for high resolution time interval measurements to determine, for example:

What is the relationship between propagation delay and temperature?

What is the t_{pd} variations (0 to 1 and 1 to 0) due to changes in V_{cc}?

How does fall time vary with fan out?

These questions required time interval resolution in the sub-nano-second region as well as a good understanding of the physical characteristics of the device and the test system, Figure 1. This article will discuss terminations, mismatch, loading, comparator techniques, calibration, etc., associated with a new economical and accurate digital measurement technique of time interval averaging.

Switching Characteristics,
$V_{cc} = 5$ V, $T_A = 25°C$, N = 10

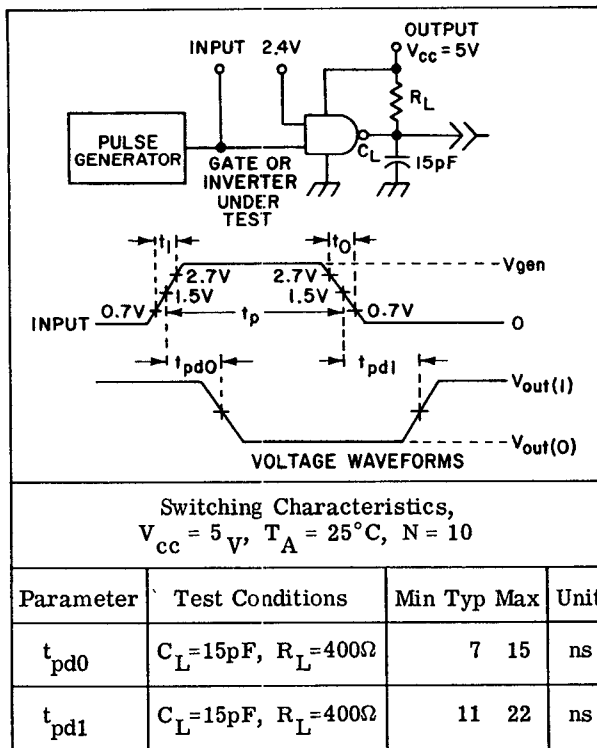| Parameter	Test Conditions	Min	Typ	Max	Unit
t_{pd0}	C_L=15pF, R_L=400Ω		7	15	ns
t_{pd1}	C_L=15pF, R_L=400Ω		11	22	ns

Figure 1. Typical Timing Measurements

Previously, these measurements were relegated primarily to sampling oscilloscopes which have limited time range and required skilled operators. Counter techniques can easily go from a pulse rise time measurement (1 to 5 ns) to a propagation delay measurement (15 to 20 ns) with a minimum of simple adjustments. Furthermore, the answer is an easy-to-evaluate digital form.

INTERFACING

Interfacing any fast rise time electronic phenomenon to a timer/counter requires that the operator terminate the input cable with its characteristic impedance to eliminate reflections, Figure 2. But attaching this cable directly to a TTL gate will result in severe pulse distortion due to loading of the device because of the rather high output impedance of presently available logic. These effects are reduced in the case of ECL because of its lower output impedance, but care must be taken when any logic is interfaced with a timer/counter. Interfacing logic, as in Figures 2 and 3, reduces the loading effects, but some other limitations are also present.
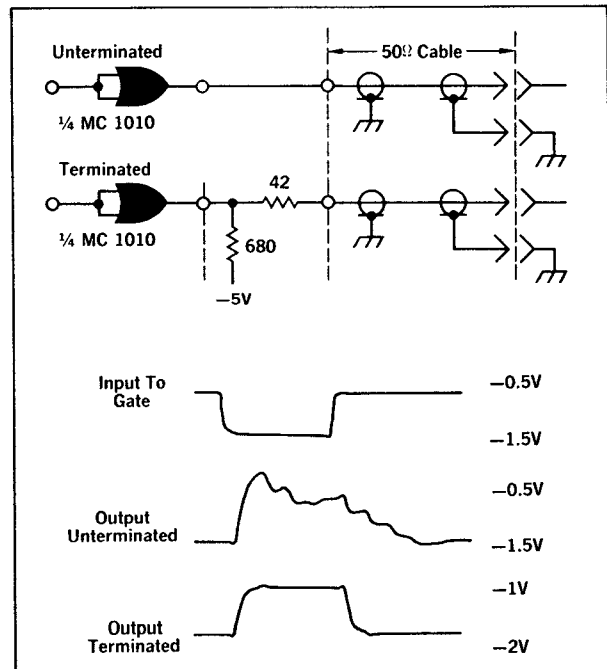

Figure 2. Output of an ECL gate connected to Model 5326A Timer/Counter, first using only a 50Ω cable (middle trace) and then a 50Ω cable with the proper series termination. Reflections resulting from improper termination can cause double counts, incorrect readings.

The input amplifiers have a fixed sensitivity and working with levels near this sensitivity limit increases trigger errors. Furthermore, the input amplifiers have finite rise times and the associated slewing becomes a limiting factor when dealing with time intervals of less than 10 ns (TTL, DTL, and ECL). Merely setting the digital timer/counter trigger levels at the 10% and 90% points for a fast test gate will not give accurate results. Instead of measuring the rise time of a test gate, one will get results which are degraded by the finite rise time of the input amplifiers. The

way to overcome these difficulties is to take advantage of the close matching which exists between the two input amplifiers. This is done by g e n e r a t i n g equal amplitude start and stop pulses with equal rise times for both input amplifiers.
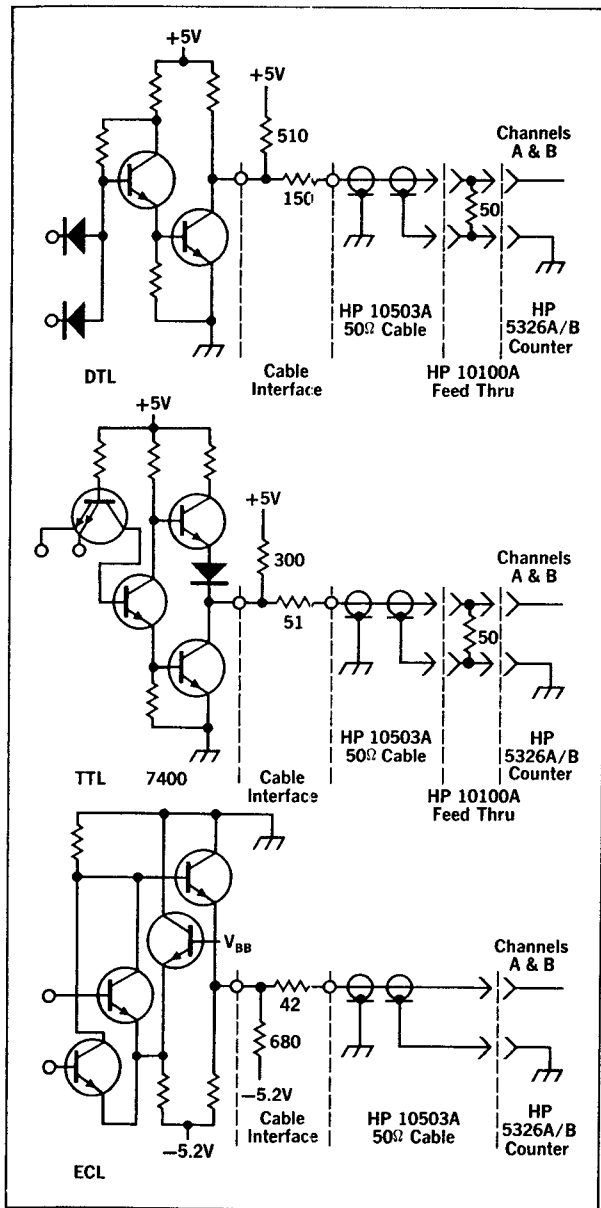

Figure 3. Recommended interface between integrated logic circuits and counter.

LOCAL COMPARATORS

The use of comparators located adjacent to the IC under test will generate the required start and stop pulses, and reduce the distortion a s s o c i a t e d with attenuators, probes, and cables. The comparators produce equal amplitude pulses and are matched into the 50Ω terminated cable (Figure 4). The rise and fall time of the NAND gate induces a time delay between the leading and t r a i l i n g edges of the pulses generated by the local comparators (Figure 4). The

comparators are biased to switch at the 10% and 90% point of the ECL gate under test, and the two timer/counter input trigger levels can now be set to equal levels, greatly reducing slewing errors.
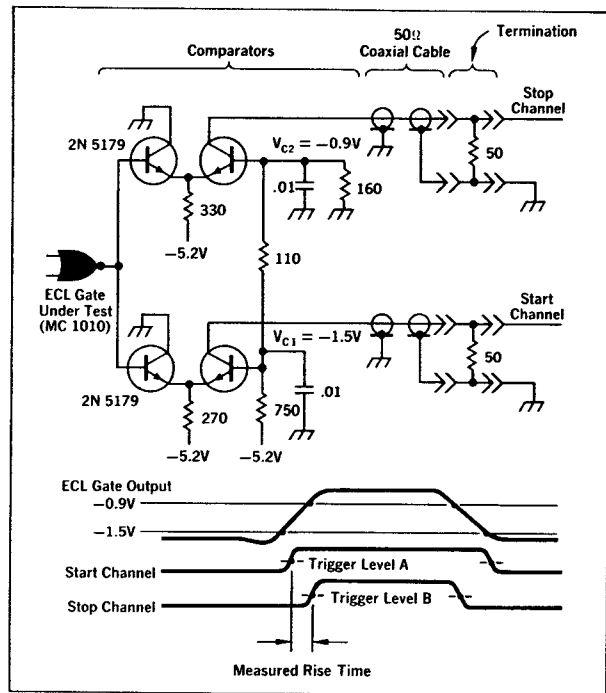

Figure 4. Measuring rise times comparable to those of Model 5326A/B's input a m p l i f i e r s (about 6 ns) requires special techniques. Here is a method that uses local comparators.

COMPARATOR

The comparators are simple and easy to design, and some of the design considerations and limits of the comparator will be explored. First, the setability of the switching point of the comparators depends on both the match of the t r a n s i s t o r s and the bias circuit. Matching the comparator transistors V_{be} will determine the setability of the switching point. The other factor is the voltage shift (V_{c1} and V_{c2}) due to switching which should be minimized by providing large bias network current and by adding capacitors.

Comparators are designed from the simple dc characteristics. The biasing networks total resistance ($R_3 + R_4 + R_5 = R_T$) is selected to be between 1000Ω and 2500Ω for good regulation of the switching point voltage. The value of C_1 and C_2 are not c r i t i c a l and merely improve switching characteristics. A capacitance of .01 μf is a nominal value and should be adequate for most applications.

For convenience, the supply voltage was selected to be equal to the IC supply voltage. Increasing the supply voltage to some higher value improves the operation and electrical stability of the circuit. R_1 and R_2 are determined by $V_{cc} = I_c R_1 + V_{BE} + V_{c1}$ where I_c is selected to be $I_c = \dfrac{V_{out}}{50\Omega}$ where $V_{out} = .5V$ to $1.0V$.

Comparators may be made in a variable or adjustable configuration for greater versatility (Figure 5). The variable comparators may be easily set to measure a variety of IC timing parameters, as rise time, propagation delays, and time constants.
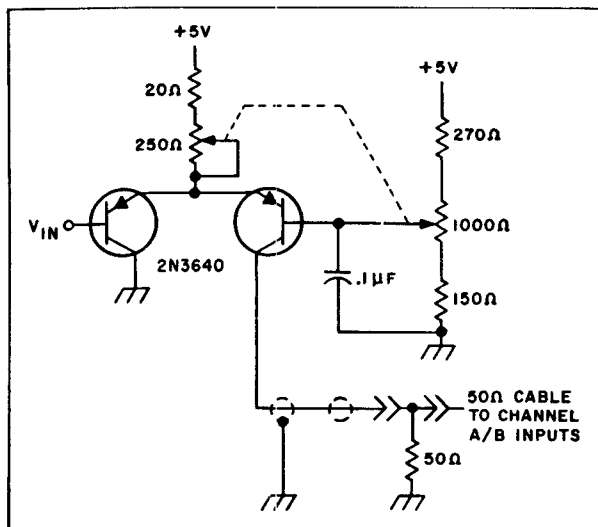

Figure 5. A similar circuit for ECL levels can be made using 2N3563 with a 0 and -5 volt supply. The output swing is approximately 0 to +.8 volt, and therefore, the trigger level on the 5326A/B would be set at .4 volts.

The transistors shown in the comparator circuits are commonly available inexpensive high-speed switching transistors. Care should be taken to select transistors which are matched electrically and for switching speed. The setability of the switching point is primarily determined by the electrical match of the transistors. Remember the test fixture should have short lead lengths and a good ground plan.

There are several commercially available comparators which may be used. A good choice is the MC 1650. This unit has high input impedance and high gain. The propagation delay is very stable with respect to both input rise time and amplitude. Comparators such as the μA 710 or LM 106 show propagation delay changes of up to 20 ns with variation in input rise time and amplitude and therefore, can only be used effectively with rise times greater than 10 ns.*

TIME INTERVAL AVERAGING

Time interval averaging is a new inexpensive timer/counter technique available in the HP 5326A/B universal timer/counter, and as the name implies, the time base clock pulses are accumulated for a pre-selected number of time interval (10^0 to 10^8). The counter then displays the total count with the decimal shifted to the left such that the time displayed equals the total count divided by the number of time intervals.

*The trigger voltage may be conveniently measured and set with the internal digital VOLTMETER in the 5326B Timer/Counter/DVM.

The result is a dramatic reduction in trigger and ±1 count errors. The improvement in accuracy and resolution (derived assuming a random occurrence of pulse of random pulse width) produces a theoretical improvement proportional to $\sqrt{\text{time intervals averaged}}$. But in reality, the results are better than predicted if a coherent signal is applied. Typically for 10^6 intervals averaged the short term repeatability of the measurement is ± 20 ps with long term drift less than ± 100 ps over 24 hours.

The ability to measure very short time intervals (less than .15 ns) is derived from a synchronizer scheme which translates the measured time interval into an integral number clock periods.

The synchronizers then gate the time base clock, Figure 6. This means for a given 180 ns time interval, the counter will count two clock pulses spaced at 100 ns for 80% of the interval averaged and one-clock pulse for 20% of the intervals averaged. The count therefore converges to the value of the time interval.

Time interval averaging can be used whenever the unknown test signal has a high enough repetition rate such that the averaging of 10^3 and 10^6 intervals can be accomplished in a short enough time, 1 sec. or less. If however, one is restricted to one-shot time interval measurements, the 5360A/5379A Computing Counter can make IC time interval discriminations to ± 200 ps using these comparator techniques.**

Because the 5326A/B's ability to measure very short time intervals (150 ps) with very high resolution (>100 ps) is statistically and electronically derived, there are three conditions which are to be met for best results:

    a. The most obvious is that the applied signal must be repetitive.

    b. The signal/triggering must not be synchronous with the internal clock or a sub-harmonic of the clock.

    c. The time between the Stop and the next Start trigger points should be a minimum of 150 ns.

The first condition is straightforward in that averaging implies multiple measurements. However, the reason for the second condition is not so obvious. If the time interval repetition rate were synchronous or phase locked to the clock of the 5326A/B, the synchronizers would no longer function as they should (Figure 6). Time interval averaging is based on statistical methods and for meaningful results the triggering must be distributed randomly with respect to the counted clock. When synchronization occurs, the readings are usually obviously erroneous, but marginal readings are possible and could go undetected. The amount of frequency offset required is easily determined (Figure 7). The amount of offset depends on both the
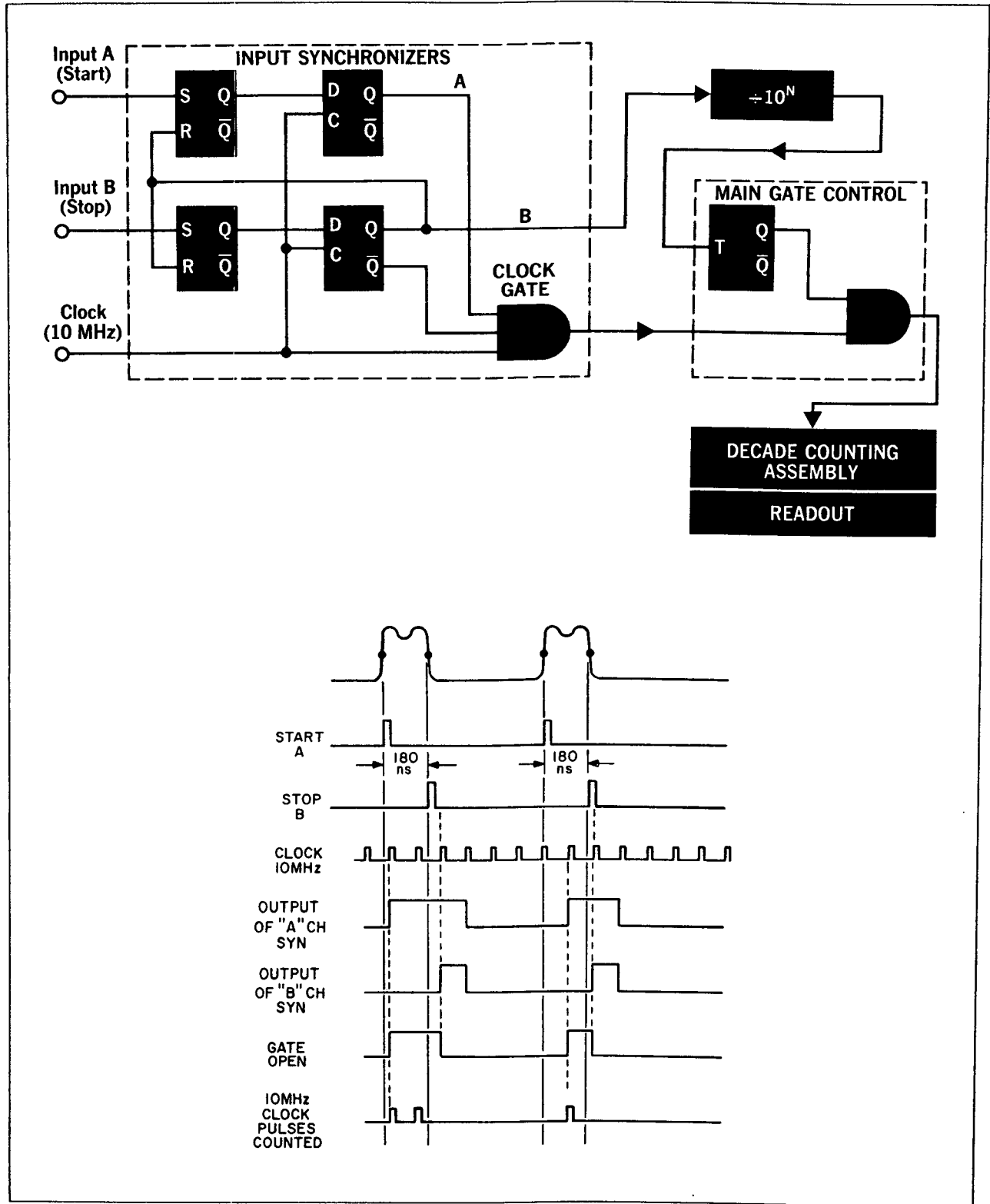
**Computing Counter, Application Note #9.

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Figure 6. Synchronizing circuit makes certain that a multiple-time-interval average will tend towards the true value. Time intervals are translated to an integral number of clock periods by the synchronizers. The synchronizers gate the clock pulses to be counted. The averaged total count converges to the true value of the time interval.

repetition rate and the number of time interval averaged. For example, if 10^5 intervals were averaged and the repetition rate were approximately 1 MHz, this repetition rate would have to differ from exactly 1 MHz by 1.0 Hz to be well out of the erroneous reading zone.
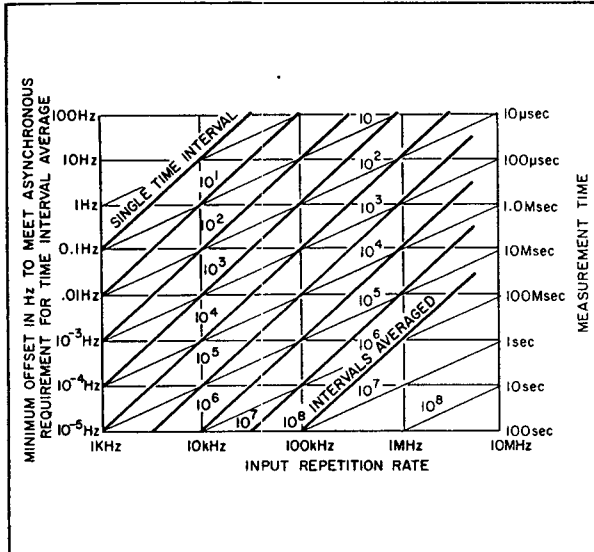

Figure 7. Frequency offset to ensure repetition rate is asynchronous with the counter's clock.

Condition number three is generated by the circuits since the registers are automatically guarded against summing clock pulses for negative time intervals. The circuit has a lockout characteristic where the clock cannot be counted when the stop precedes the next start by less than a preset dead time. It is very important to be out of this dead time area to obtain accurate readings. The recommended minimum time between the stop trigger point and the next start trigger point is 150 ns.

PRECISION

The trigger error and ± 1 count error are random by nature and may be diminished by averaging, but there is also an error due to the time delays of the internal circuitry. Therefore, the actual precision of time interval averaging is: ± time base accuracy ± 2 ns ±

$$\frac{\text{Trigger Error* ± 100 ns**}}{\sqrt{\text{Number of periods averaged}}}$$

The reproducibility of Time Interval Averaging is better than 100 ps over a 24-hour period (for 10^6 intervals). Short term stability is better than ± 20 ps (for 10^6 intervals) measuring delays through comparators. ***

The ± 2 ns error in Time Interval Averaging is established by the degree to which the propagation delays between the start and stop amplifiers, and other delays are matched. These systematic errors can be eliminated by calibrating the test setup.

CALIBRATION

Calibration is simply the removal of the systematic errors present by altering the measurement setup. In the case of the 5326A/B, this would include the ± 2 ns systematic error and cable error.

Calibration is accomplished by inducing pulses of equal pulse widths and amplitudes into the two input timing amplifiers of the digital timer/counter. The calibration pulses are generated by setting both comparators to the same trigger point ($V_{c1} = V_{c2}$) and applying the same driving signal to both. This eliminates the delays between the leading and trailing edges of the pulses generated by the comparators. Then the propagation delays in the measurement system are altered to minimize the internal and external systematic errors.

To obtain very high resolution with time interval averaging the timer/counter is electronically guarded against responding to negative time intervals and therefore, it will display zero or some positive time interval value only. The input cable lengths are changed slightly, thus, altering the propagation delay into the inputs until a reading near zero is present. When calibrating, remember that the measurement scheme will not measure negative time intervals and will display zeros. It is, therefore, very important to have a small positive reading present to be sure you are not in the negative time interval region; that is, the 10^6 intervals averaged, the calibration reading should be less than 50 ps but greater than zero. The calibration should produce a small positive reading which is less than the usable resolution of the measurement, but greater than zero.

*Trigger error $\dfrac{\pm\,.0025V}{\text{signal slope}}$ (signal slope in V/μs with signal-to-noise at 40 dB).

**± 1 Count error.

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