A High IIP3 Balanced Low Noise Amplifier for Cellular Base Station Applications Using the Agilent Enhancement Mode PHEMT ATF-54143 Transistor and Anaren Pico Xinger 3 dB Hybrid Couplers

Application Note 1281

Introduction

Most base stations (BTS) can transmit a signal to a mobile device further and stronger than they can receive the signals coming back from it. This is known as link imbalance and is made worse by the feeder loss between the base station and the antennas. This imbalance can be as high as 20% or more, so system designers need to correct the balance in order to improve coverage. The simplest solution is the addition of a Tower Mounted Amplifier (TMA) or Masthead Amplifier. A TMA installed directly beneath a base station antenna can increase the sensitivity of the base station and increase its range by up to 40%, correcting the link imbalance and almost doubling its reception coverage area. A low loss filter and low noise amplifier within the TMA help to select and amplify the received signal. In effect, the Tower Mounted Amplifier works as a powerful "hearing aid" for the base station.

This paper describes the design of the balanced low noise amplifier within the TMA. A typical TMA functional block diagram is shown in Figure 1. The alarm circuit senses a failure in the LNA and is normally triggered by a window comparator circuit that checks the bias current. The by-pass switch allows bypass of the LNA if a failure occurs, and thus allows the base-station sector to keep operating although with reduced performance. The switch can be implemented with PIN or FET devices.

The LNA described in this paper is for use in applications covering 1.7 GHz to 2.2 GHz. This frequency range includes GSM-1800, US-PCS, W-CDMA, and IMT-2000 cellular up-link frequencies. This application note will focus on the design considerations as well as the expected and actual performance. The paper contains six sections:

1) Design Goals
2) Device Selection
3) Splitter/Combiner Selection
4) Amplifier Design
5) Test Results
6) Conclusions

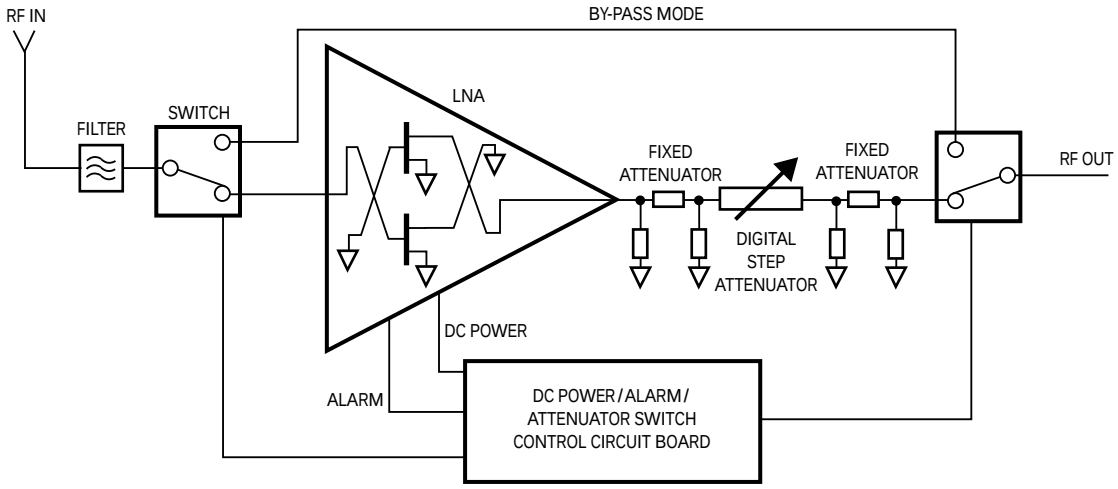

Figure 1. Tower Mounted Amplifier Functional Block Diagram

Design Goals

The primary goals for any low noise amplifier are:
1) low noise figure
2) adequate gain
3) stability

For the case of a tower-mounted application, high intercept point, 5 volts supply voltage, and low current consumption are also required. Figure 2 shows the top level schematic of the LNA. The balanced topology shown has several important features:
1) 3 dB higher intercept point than a single stage.
2) 50 ohm input and output match.
3) Redundancy which minimizes a hard failure.

The use of a balanced configuration insures good input and output match, and helps ensure stability. However, the splitter/combiner network must be low loss, physically small, and have good phase and amplitude matching over the bandwidth of interest. Finally, the bandwidth should be high enough to include the up-link (mobile device to base-station) frequencies for cellular standards around 2 GHz. The design goals were thus chosen as shown in Table 1.

Device Selection

The Agilent ATF-54143 is one of a family of new high dynamic range, low noise enhancement mode PHEMT (E-pHEMT) devices designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. It is an 800-micron gate width device with 2 GHz performance tested and guaranteed at a V_{CE} of 3 V and I_d of 60 mA. The ATF-54143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The enhancement mode ATF-54143 will only require one regulated supply. If an active bias is desirable for repeatability of bias setting, then the ATF-54143 will only require the addition of a single PNP BJT [1].

Compared to amplifiers using depletion mode devices, the Agilent ATF-54143 has another significant advantage – a lower part count and a more compact layout. An amplifier using a depletion mode FET will require: a negative voltage source, a regulator for the negative voltage, a timing circuit so the drain voltage does not arrive before the gate voltage, and a limiting circuit to make sure the gate voltage does not exceed the maximum gate to source voltage (V_{gs}).

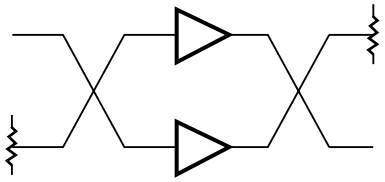

Figure 2.

Table 1. Design Goals

Parameter at 2000 MHz	Value
Gain	15 - 16 dB
Noise Figure, dB	< 1 dB
Output 3rd Order Intercept Point	> 37 dBm
Input 3rd Order Intercept Point	> 21 dBm
Output P-1dB Compression	22.4 dBm
Input return loss	> 15 dB
Output return loss	> 15 dB
Supply Current	< 150 mA
Bandwidth	1.7 - 2.2 GHz

Splitter/Combiner Selection

An important consideration for a balanced amplifier is the splitting and combining of the RF signal. Power division and power combining are generally accomplished by use of a power divider or a hybrid coupler. Power dividers and hybrid couplers are passive microwave components, and can be printed on a substrate (in microstrip form), or can be obtained in surface mount packages. This section compares the various methods used for power division and combining.

When designing the splitter network for a balanced low noise amplifier, it is important to minimize insertion loss and return loss while providing equal power to each of the two amplifiers. Power dividers are sometimes used to

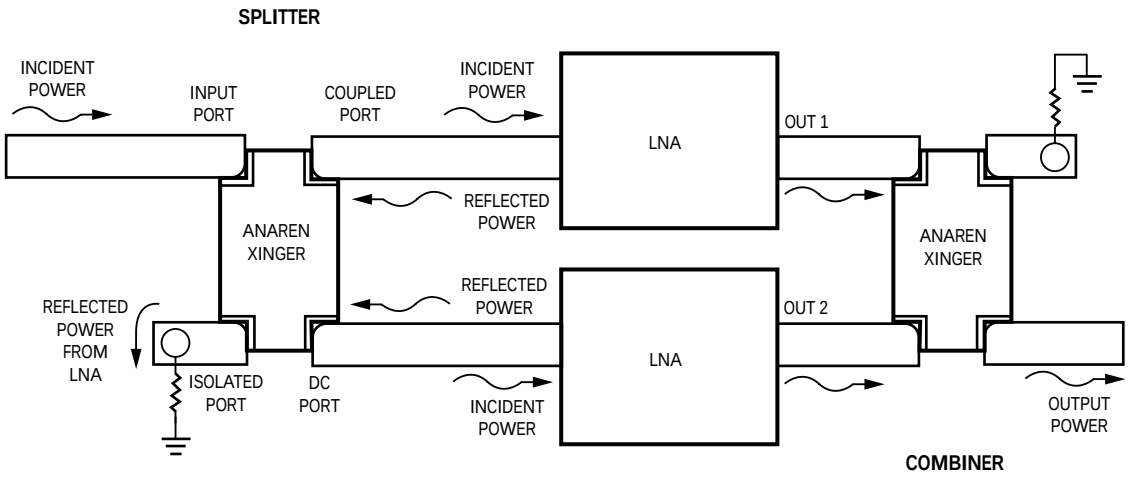

Figure 3. A Balanced Low Noise Amplifier

accomplish this task. The two most popular types of power dividers are the T-junction divider and the Wilkinson power divider. Wilkinson power dividers make use of quarter wavelength transmission lines to produce the desired power splits. A shunt resistor placed between the two output legs of the divider is used to isolate and match all ports. Due to the quarter wavelength transmission lines, the bandwidth of a single section power divider is limited to 10 - 20%.

Table 2. Typical Data for the Anaren Pico Xinger JP503

Specification	Bandwidth	Units
Frequency	2.0 - 2.3	GHz
Isolation	20	dB min.
Insertion Loss	0.30	dB max.
VSWR	1.20	Max: 1
Amplitude Balance	±0.25	dB max.
Phase Balance	3	Degrees max.
Power Handling	25	Avg. Watts - CW max

Although power dividers can be used in balanced amplifier design, low loss hybrid couplers prove to be superior for several reasons. Hybrid couplers are four port devices characterized by good match and isolation and by a fixed 90° phase shift between the output ports. Two popular hybrids are the branch-line hybrid and the broadside-coupled hybrid. The bandwidth of a branch-line hybrid is limited to 10 - 20%, but a single section broadside coupler can have bandwidth as large as an octave. Furthermore, a broadside coupler requires only half the amount of line used in a branch-line hybrid, and can thus be made smaller in size.

Figure 3 illustrates the most important advantage of using a hybrid coupler over a power divider on the input side of the balanced amplifier. Reflected power from each of the two identical LNA inputs recombines at the isolated port of the hybrid coupler, and is dissipated in the resistive termination. This feature of the hybrid coupler allows Agilent to design each LNA for optimum noise figure performance, without actually worrying about return loss from each of the two LNAs. It follows that if a hybrid coupler is used on the input side, then an identical hybrid coupler can be used on the output side to recombine the signals.

Anaren Microwave Inc. manufactures surface mount hybrid couplers that are excellent for splitting and combining signals. Anaren recently released a new class of miniature hybrid couplers called Pico Xingers®. The Pico Xinger® is a low profile, miniature 3 dB hybrid coupler that comes in an easy-to-use surface mount package and is designed for DCS and PCS applications. For this balanced amplifier, Agilent chose to use the Pico Xinger® JP503 surface mount coupler. The coupler has low loss and good return loss over a wide frequency band. Typical specifications for the JP503 are shown in Table 2.

Amplifier Design

Biasing Options and Source Grounding

In order to meet the design goals for noise figure, intercept point and gain, the drain source current (I_{ds}) was chosen to be 60 mA. As indicated by the characterization data shown in the device data sheet [XX], 60 mA gives the best IP3 while at the same time a very low minimum noise figure (F_{min}). Also shown in the data sheet, a 3 volt drain to source voltage (V_{ds}) gives a slightly higher gain and is also preferred since it easily allows the use of a 5 volt regulated supply.

As mentioned earlier, one of the advantages of the enhancement mode PHEMT is the ability to dc ground the source leads and yet only require a single positive polarity power supply. A depletion mode PHEMT pulls maximum drain current when V_{gs} = 0 V whereas an enhancement mode PHEMT pulls nearly zero drain current when V_{gs} = 0 V. The gate must be made positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

Biasing the Agilent ATF-54143 is accomplished by the use of a voltage divider consisting of R1 and R2. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant. The purpose of R4 is to enhance the low frequency stability of the device by providing a resistive termination at low frequencies. Capacitor C3 provides a low frequency bypass for R4. Additional resistance in the form of R5 (approximately 10 kΩ) is added to provide current limiting for the gate of enhancement mode devices such as the ATF-54143. This is especially important when the device is driven to P1-dB or Psat.

$$R1 = \frac{V_{gs}}{I_{BB}}$$

$$R2 = \frac{(V_{ds} - V_{gs}) \times R1}{V_{gs}}$$

$$R3 = \frac{V_{DD} - V_{ds}}{I_{ds} + I_{BB}}$$

Where:
I_{ds} is the desired drain current.
I_{BB} is the current flowing through the R1/R2 voltage divider network.
Example, choosing I_{BB} to be at least ten times the maximum expected gate leakage current. I_{BB} was chosen to be 2 mA. V_{DD} = 5 V, V_{ds} = 3 V, I_d = 60 mA, V_{gs} = 0.56 V.

R1 = 280 Ω,
R2 = 1220 Ω and
R3 = 32.3 Ω

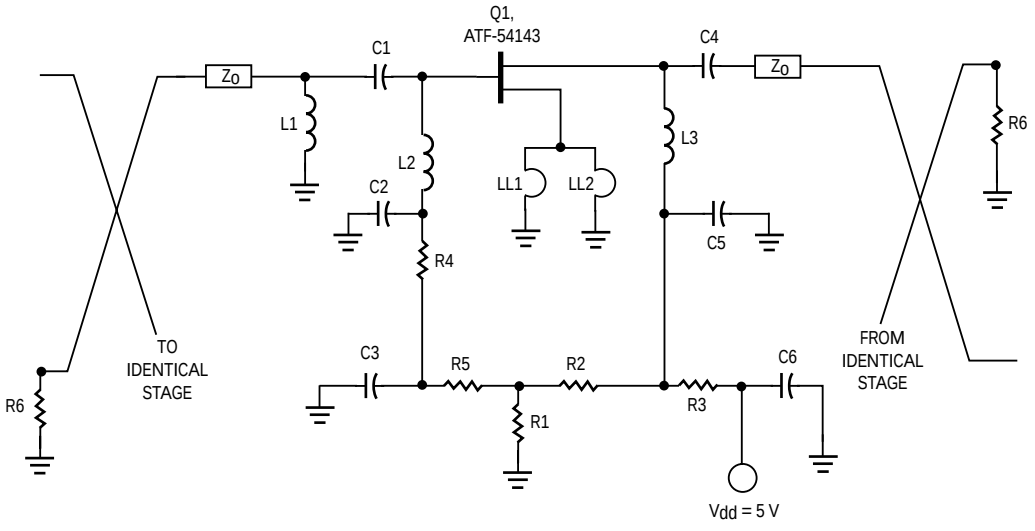

Figure 4. The Amplifier Schematic

The repeatability of the bias settings from device to device is a function of a particular device's DC characteristics. As mentioned previously, to get better repeatability of bias setting, an active bias is recommended. More information including design equation for active biasing is shown in reference [1].

The use of a controlled amount of source inductance can often be used to enhance LNA performance. The amount of inductance required is usually only a few tenths of a nano-Henry. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily modelled using a RF simulation tool such as Agilent Technologies' advanced design system (ADS). The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be.

Agilent ATF-54143 Low Noise Amplifier Design

Using Agilent Technologies' EEsof Advanced Design System Software the amplifier circuit can be simulated in both linear and non-linear modes of operation. The original design draft was a low noise amplifier with an Output Third Order Intercept Point (OIP3) of 39 dBm with a noise figure close to 1.0 dB at 2.0 GHz.

Linear Analysis

One half of the amplifier circuit used for the linear analysis is shown in Figure 5. For the linear analysis the transistors can be modelled with a two port s-parameter file using Touchstone™ format. The ATF54143.s2p file can be downloaded from the Agilent Wireless Design Centre web site. The simulation controls can be obtained from the Sparams_wNoise template available in ADS. The circuit components can then be added to the simulation circuit. The more detailed the simulation the more accurate the results will be. An accurate circuit simulation can provide the appropriate first step to a successful amplifier design. Transmission line section can be modelled with various micro-strip and strip-line elements available in the component library. In this case, all micro-strip section assumed a 0.031 inch thick board and FR-4 material. The inductance associated with the chip capacitors and resistors was also included in the simulation. Where possible, models were chosen from the ADS SMT component library. Models of SMT components can also be obtained from the manufacturers' web sites. Manufacturing tolerances in both the active and passive components often prohibit perfect correlation. When the design met the target specifications for gain, noise figure and stability, the create/edit schematic symbol function was used from the view menu in ADS. This allows the designer to easily duplicate the amplifier design.

The model for the hybrid coupler is based on 4 port Touchstone™ linear s-parameter file and can be downloaded from the Anaren web-site. The micro-strip elements, the circuit balanced amplifier input and output tracks and 50 ohm load resistor pads were added to build up the complete amplifier. The input and output matching networks use a high pass topology to ensure good low frequency stability. The simulator is then used to find component values, which give the desired performance.

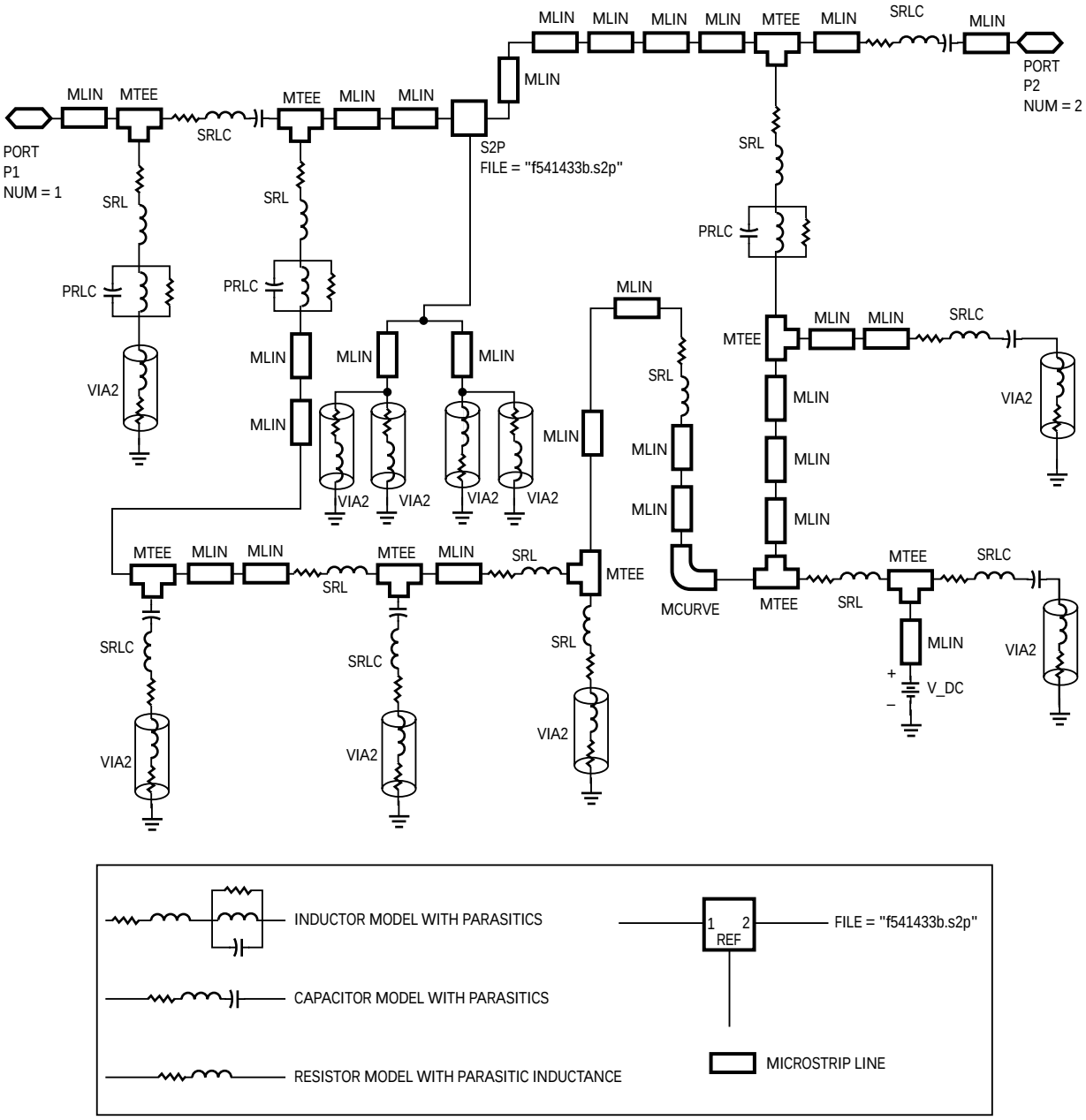

Figure 5. ADS Schematic

The results of the simulated noise figure, gain, input and output return losses are shown in Figures 6, 7, and 8. The linear simulated performance of the amplifier was very close to the measured results. The design was tested with 3 V, 40 mA S-parameter file and showed no changed in linear performance.

As noted on the data sheet, the ATF-54143 S and Noise Parameters are tested in a fixture that includes plated through holes through a 0.025" thickness printed circuit board. Due to the complexity of de-embedding these grounds, the S and Noise Parameters include the effects of the test fixture grounds. Therefore, when simulating a 0.031" thickness printed circuit board, only the difference in the printed circuit board thickness is included in the simulation, i.e., 0.031" - 0.025" = 0.006". The transmission lines that connect each source lead to its corresponding plated through hole is simulated as a microstrip transmission line (MLIN).

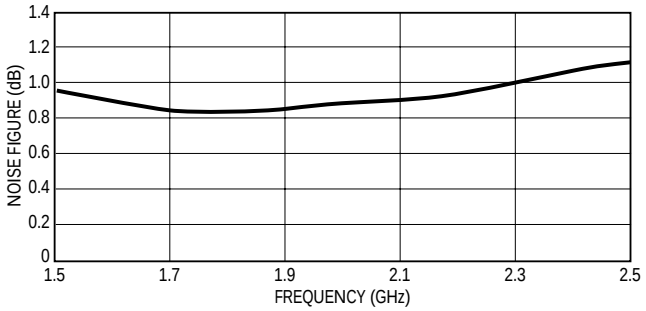

Figure 6. Linear Simulated Noise Figure vs. Frequency

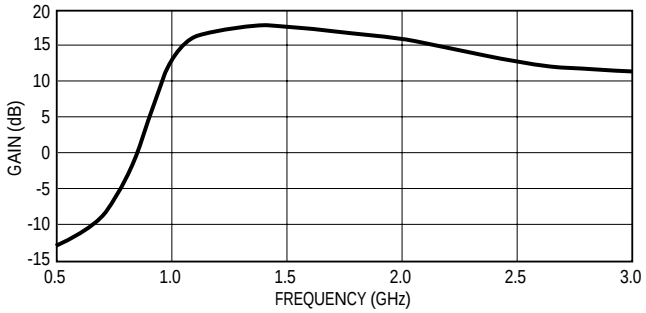

Figure 7. Linear Simulated Gain vs. Frequency

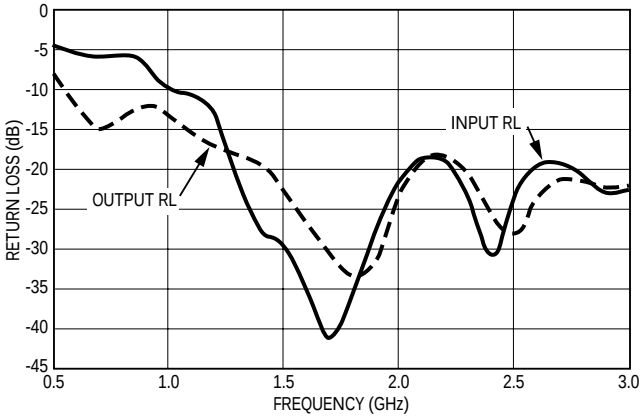

Figure 8. Linear Simulated Input and Output Return Loss vs. Frequency

Non-linear Analysis

For the non-linear analysis, a harmonic-balance (HB) simulation was used. HB is preferred over other non-linear methods because it is computationally fast, handles both distributed and lumped element circuitry, and can easily include higher-order harmonics and inter-modulation products [2]. In this application HB was used for simulation of 1 dB compression point (P-1dB) and output third order intercept point (OPI3).

The non-linear transistor model used in the simulation is based on the work of Curtice [3]. The model can be downloaded from Agilent's web-site. An important feature of the non-linear model is the use of a quadratic expression for the drain current versus gate voltage. Although this model closely predicts the DC and small signal behavior (including noise), it does not predict the intercept point correctly. For example, the balanced amplifier OIP3 was simulated at +34.4 dBm and the P-1dB at +21.8 dBm. The simulated performance for P-1dB was very close to the measured results, however, the simulated OIP3 was too low. (see Table 3).

Table 3. Simulated non-linear performance

Bias Conditions per FET	P-1dB	Third Order Intercept
3 V, 40 mA	19.8 dBm	31.9 dBm
3 V, 60 mA	21.8 dBm	34.4 dBm
3 V, 80 mA	22.0 dBm	34.7 dBm

To properly model the exceptionally high linearity of the E-pHEMT transistor, a better model is needed. This model, however, can still be used to predict the relative importance of output matching, bias, and source inductance.

Circuit Stability

Besides providing important information regarding gain, P-1dB, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

The simulated gain, noise figure, and input/output return loss of the ATF-54143 amplifier are shown in Figures 9, 10 and 11. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss and stability. A plot of Rollett Stability factor K as calculated from 1 GHz to 3 GHz is shown in Figure 12 for the amplifier. Emitter inductance can be used to help stability. However, it should be noted that excessive inductance will cause high frequency stability to get worse (i.e., decreased value of K).

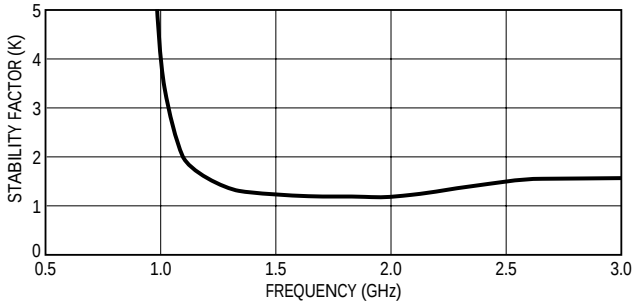

Figure 9. Simulated Rollett stability factor K

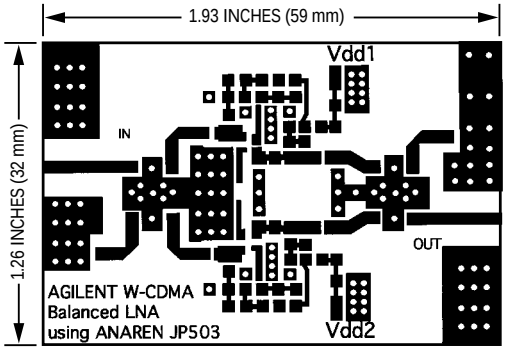

Figure 10. Artwork for the Balanced ATF-54143 Low Noise Amplifier

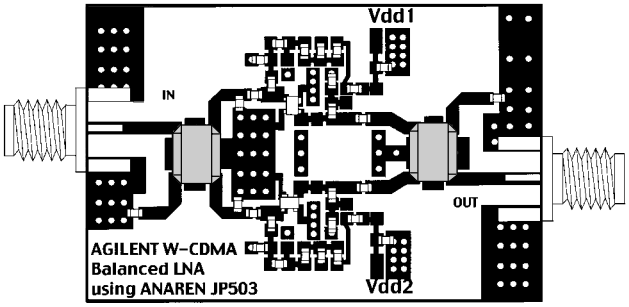

Figure 11. Component Placement Drawing for the ATF-54143 Low Noise Amplifier

Final ATF-54143 Amplifier Design

As discussed previously, the amplifier was designed for a V_{ds} of 3 volts and an I_{ds} of 60 mA. The amplifier schematic is shown in Figure 4. A typical power supply voltage, V_{dd}, would be in the 5 volt range. The evaluation board shown in Figure 10 is used. The board gives the designer several design options for the RF circuitry. The evaluation board was designed such that the input and output impedance matching networks can be adjusted to optimize the performance over the 1.7 - 2.2 GHz frequency range. Either low pass or high pass structures can be generated based on system requirements. The demo board is etched on 0.031" thickness FR-4 material for cost considerations. The main constraint for the LNA RF layout is the circuit must be a balanced configuration, the path lengths in each arm of the amplifier must be the same. The effect of uneven path lengths results in the summing of the signals out of phase and lower output power and IP3 than expected. To necessitate this the bottom ATF-54143 is turned through 90°. This allows for an easy duplication of the top and bottom RF micro-strip tracks.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor C1 and shunt inductors L1 and L2. The circuit loss will directly relate to noise figure, thus Q of L1 and L2 is extremely important. The Toko LL1608-FS4N7 or similar device is suitable for this purpose. The Toko LL1608-FS4N7S is a small multi-layer chip inductor with a rated Q of 43 at 800 MHz. Shunt inductor (L1) provides low frequency gain reduction, which can minimize the amplifier's susceptibility to low frequency transmitter overload. It is also part of the input matching network along with C1. C1 also doubles as a dc block. L2 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. This network has been a compromise between low noise figure, input return loss and gain. Capacitors C2 and C4 provide in band stability while resistors R3 and R4 provide low frequency stability by providing a resistive termination. The high-pass network on the output consists of a series capacitor C4 and shunt inductors L3. L3 also doubles as a means of inserting drain voltage for biasing up the PHEMT. The parts list for the first amplifier is shown in Table 4. The artwork and component placement are shown in Figures 10 and 11.

Inductors LL1 and LL2 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstrip section, which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.050" from the source lead. The 0.050" is measured from the edge of the source lead to the closest edge of the

Table 4. Component Parts List for the ATF-54143 Amplifier.

C1	2.2 pF chip capacitor 0603
C2, C5	8.2 pF chip capacitor 0603
C3, C6	10000 pF chip capacitor
C4	10 pF chip capacitor 0603
LL1, LL2	Source inductance of width 25 mil x length 50 mil microstrip between source and first via hole can be used to increase stability and improve NF and input match.
L1, L2	4.7 nH Toko LL1608-FS chip inductor
L3	5.6 nH Toko LL1608-FS chip inductor
R1	300 Ω
R2	1300 Ω
R3	32 Ω
R4	47 Ω
R5	10 kΩ
R6	50 Ω load resistors
Q1	Agilent Technologies ATF-54143

first via hole. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimise performance. This is discussed in detail in the next section.

Determining the Optimum Amount of Source Inductance

As mentioned previously, adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential downside is reduced low frequency gain. However, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far? For an amplifier operating in the 2.0 GHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is fine as long as the amount of source inductance is fixed and has some margin in the design in order to account for S21 variations in the device.

Test Results for the Complete Balanced Agilent ATF-54143 Amplifier

Each FET in the amplifier is biased at a V_{ds} of 3 V and I_d of 60 mA, giving a total current of 120 mA. Typical V_{gs} is 0.56 volts. The complete amplifier is shown in Figure 12. The measured noise figure and gain of the completed amplifier are shown in Figures 13 and 14. Noise figure is a nominal 0.8 dB from 1.7 through 2.1 GHz. Gain is typically 15.3 dB at 2.1GHz with a peak of 18.2 dB at 1.1 GHz. The noise figure measurement was made on the bench and includes connector losses and secondary noise losses. Noise fig-

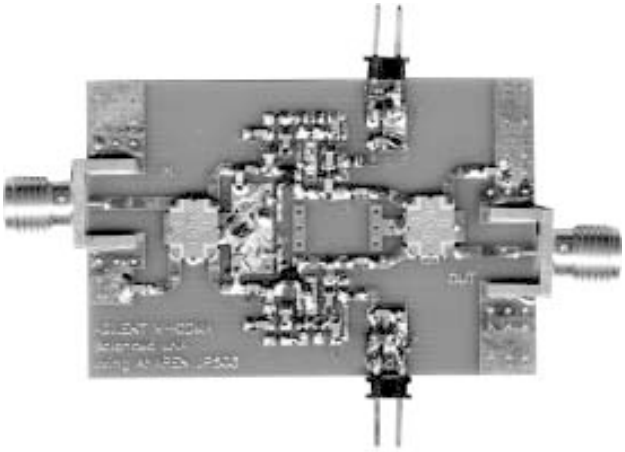

Figure 12. Photograph of Balanced Amplifier Board

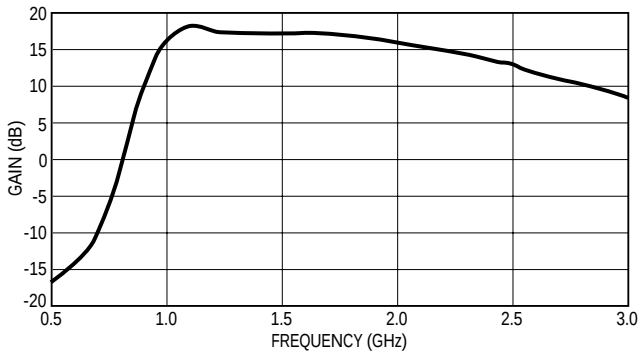

Figure 13. Gain vs. Frequency

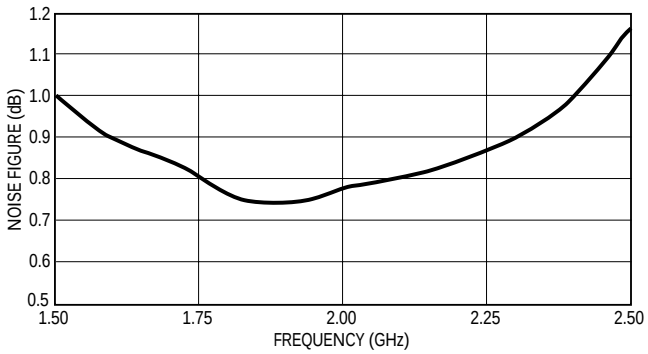

Figure 14. Noise Figure vs. Frequency

ure performance was found to be slightly better than the simulated noise figure of the circuit.

Measured input and output return loss is shown in Figure 15. The input return loss at 2.0 GHz is 17.3 dB with a corresponding output return loss of 20.0 dB. The amplifier output intercept point (OIP3) was measured at a nominal +39 dBm at a dc bias point of 3 volts V_{ds} and an I_d of 60 mA. P-1dB measured +22.4 dBm. The amplifier was also checked at lower bias conditions of 3 volts V_{ds} and I_d of 40 mA. No degradation to the noise and gain response was noted. Typical output third order intercept was measured at a nominal 36 dBm.

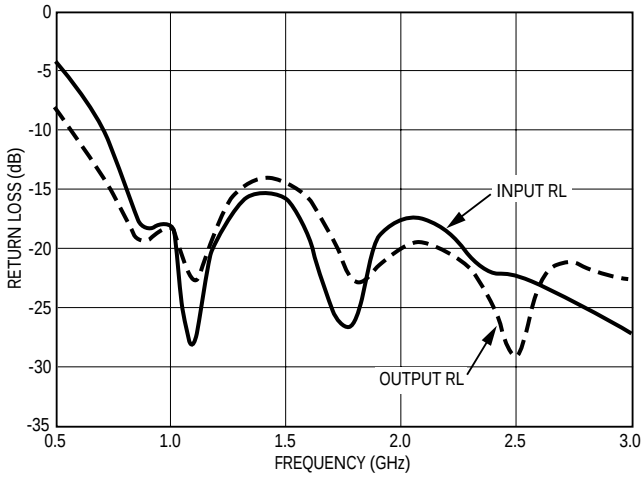

Figure 15. Input and Output Return Loss vs. Frequency

Conclusions

A balanced low noise amplifier design has been presented using the Agilent Technologies ATF-54143 low noise enhancement mode PHEMT and the Anaren JP503 Hybrid couplers. The ATF-54143 provides a very low noise figure along with high intercept point making it ideal for applications where high dynamic range is required. It also has the advantage of a single polarity bias. The design may easily be adapted for a multi-stage amplifier, with the first ATF-54143 set to a lower bias setting of 30 - 40 mA, followed by a second stage biased at 60 mA. The Anaren couplers provide a very small, low loss solution while providing excellent input and output return loss, making the amplifier easy to cascade with other amplifiers and filters with minimal effect on system pass band gain ripple. The use of simulation to predict performance before fabricating the prototype led to first time success. The models for the

Table 5. Measured Results

Parameter	Value
Minimum Gain	14.8 dB
Maximum Noise Figure, dB	0.85 dB
Output 3rd Order Intercept Point	39 dBm
Input 3rd Order Intercept Point	24.2 dBm
Output P-1dB Compression	22.4 dBm
Maximum Input return loss	17.2 dB
Maximum Output return loss	18.5 dB
Supply Current	120 mA
Bandwidth	1.7 – 2.2 GHz

transistor, the coupler, microstrip line, and the lumped elements led to excellent agreement between modelled and measured thus confirming the validity of the simulations.

References

[1] Agilent Application Note AN1222, “A Low Noise High Intercept Point Amplifier for 1930 to 1990 MHz using the ATF-54143 PHEMT”, A.J. Ward.

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Performance data for the Agilent ATF-54143 PHEMT may be found on http://www.agilent.com/view/rf Application Notes
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