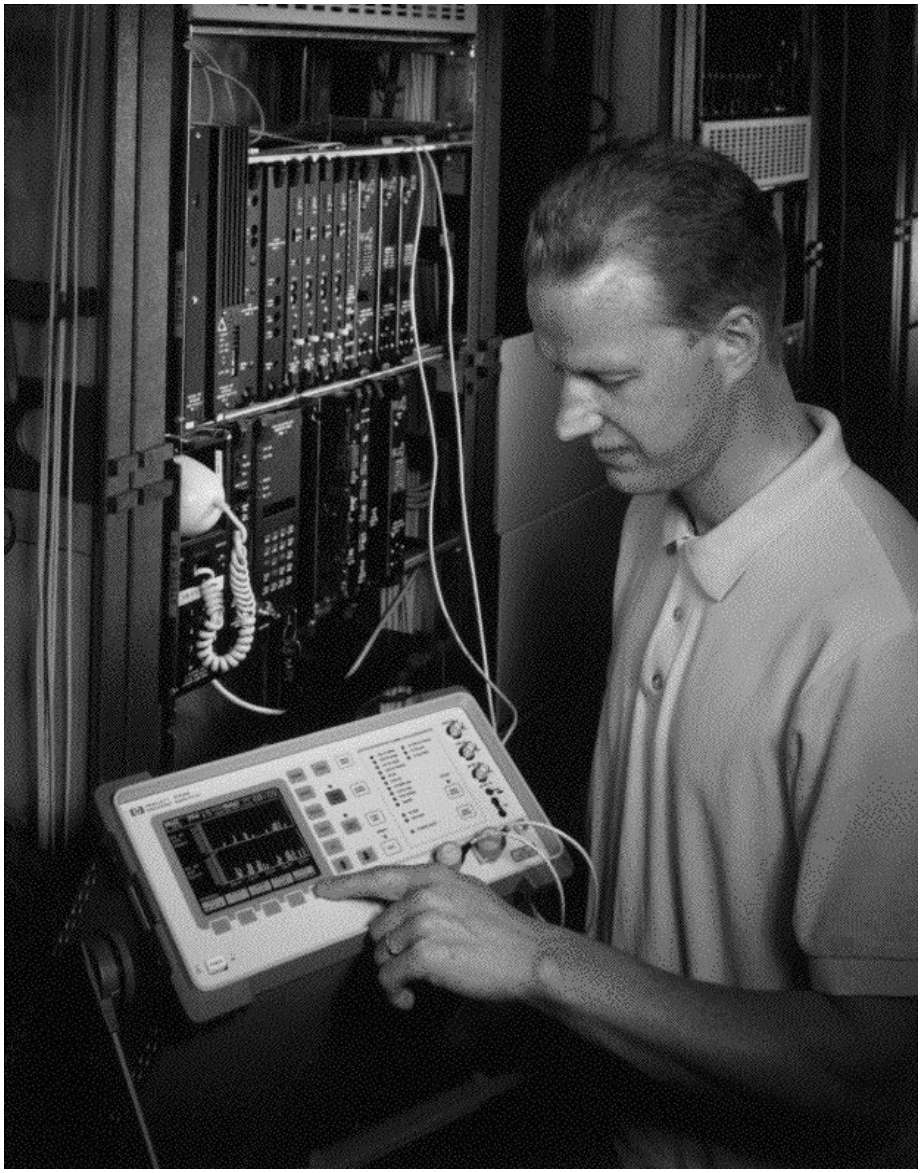
HEWLETT PACKARD

Evaluating Tributary Jitter from the SDH Network

Application Note 1258



SDH

Introduction

The innovation of using pointers to track the position of the Virtual Container (VC) within SDH signals has produced many benefits that will minimize the cost and complexity of network equipment. For example, SDH removes the need for back-to-back multiplexers/demultiplexers in cross-connects and add/drop multiplexers by enabling any customer payload to be located and tracked without the need to dismantle the multiple layers of hierarchy within the structure. However, due to the large inherent phase step associated with a pointer movement (ie, 24UI per AU-4 pointer movement), compared to that produced by pulse stuffing techniques used in asynchronous multiplexing, the SDH network has the potential of creating large jitter transients in the demultiplexed tributary outputs. The need to characterize the jitter performance of demultiplexers is being considered by Standards Committees such as ITU Study Group 13 at the time of writing (April 1994).

The network architecture

In the long term, the synchronous SDH network may develop to the state where asynchronous networks will only exist at the periphery of the synchronous network, and all transport through the network is on SDH. However, this is an ideal model that may not be prevalent until well into the next century. At present, and during this intervening period as the SDH network evolves, the hybrid synchronous/asynchronous network will predominate. Thus a signal may experience several synchronous/asynchronous conversions during its passage through the network.

As SDH equipment is installed in the network, SDH islands will appear. Initially, these SDH islands are likely to be point-to-point networks. As the SDH portions of the network increase, these islands will merge to form larger more sophisticated islands consisting of not only Path Terminating Equipment (PTE) but also Add/Drop Multiplexers (ADM), Digital Cross-connect Systems (DCS), etc. As the tributary signal traverses these larger SDH islands as part of an VC, phase and/or frequency differences between SDH network elements will induce pointer activity in the SDH signal.

The impact of this pointer activity will be to increase the jitter on the asynchronous tributary signal passing out of the SDH island. This will produce an accumulation of jitter on the tributary signal as it traverses the multiple islands in its transmission path.

For the long term network development scenario, (when end-to-end SDH transmission is prevalent), the jitter performance of the terminating PTE will be the main contributor to jitter on the demultiplexed tributary signal. However, until reaching this stage of development, the network will become filled with SDH islands. A tributary signal's transmission path may involve traversing multiple SDH islands, and the problem of jitter accumulation will exist.

Analysis of the network

In order to specify the jitter limits on a PTE, analysis has been performed to predict the expected jitter accumulation that might occur as a tributary signal passes through multiple SDH islands. The objective of this study is to produce a model that represents a practical worst-case example of a network that may be used to transfer a PDH signal. {A similar study carried out by Bellcore for the SONET world produced a 32 SONET island model, each of which contains 10 pointer processing nodes [1], (Figure 1).}

To ensure that the jitter accumulation does not cause service degradation at the output of the last SDH island, the total network jitter must not exceed that specified for the tributary rate [2]. Therefore, each PTE must not only meet this specification but will have to exhibit a far better performance if the jitter at the output of the last SDH island is to meet this requirement.

Once the size and structure of the network model has been agreed, the allocation of the amount of jitter which can be generated by the various jitter-producing effects will be performed to ensure that the total network jitter does not exceed the specified limit on a tributary signal. As an example of the order of magnitude that is likely to be settled upon, ANSI tackled a similar problem for the DS3 interface which requires that the peak-to-peak jitter shall not exceed 5UI, (in the 10Hz to 400 kHz range).

In order to achieve this with the 32 island model, the maximum jitter from a PTE is limited to 1.3UI. Table 1 shows how this budget has been allocated between mapping jitter, single pointer movements and degraded synchronization conditions.

Characterization of jitter performance

G.783 presently includes pointer test sequences [3]. These sequences are aimed to emulate expected network degradations.

During 1992, Telecom Canada carried out testing to verify the theoretically predicted responses to various types of pointer activity on PTEs [4]. As well as verifying the theoretically predicted responses to variations in pulse stuffing ratios (used to map the tributary signal into the VC), and to single pointer movements, Telecom Canada also showed that the defined tests did not fully represent the pointer sequences that a real network might produce.

With the results from the practical experimentation and the specification of jitter performance in terms of three network conditions, (an example of which is shown in Table 1), ANSI have reviewed the pointer movement sequences [5]. The aim was to produce tests that more closely emulated real network conditions and also allow measurement of the specified jitter thresholds.

Also, as a further result of the experimentation, it has become clear that test methodology guidelines need to be produced in order to achieve accurate and repeatable results.

Liasion between ANSI and ITU has prompted ITU to also review the pointer test sequences. Study Group 13 is, at the time of printing, considering how the sequence in G.783 should be expanded/modified.

Figure 1: Hybrid network model produced for the transfer of DS3 through a SONET Network. ITU Study Group 13 is investigating the generation of a similar model for each of the CEPT rates.

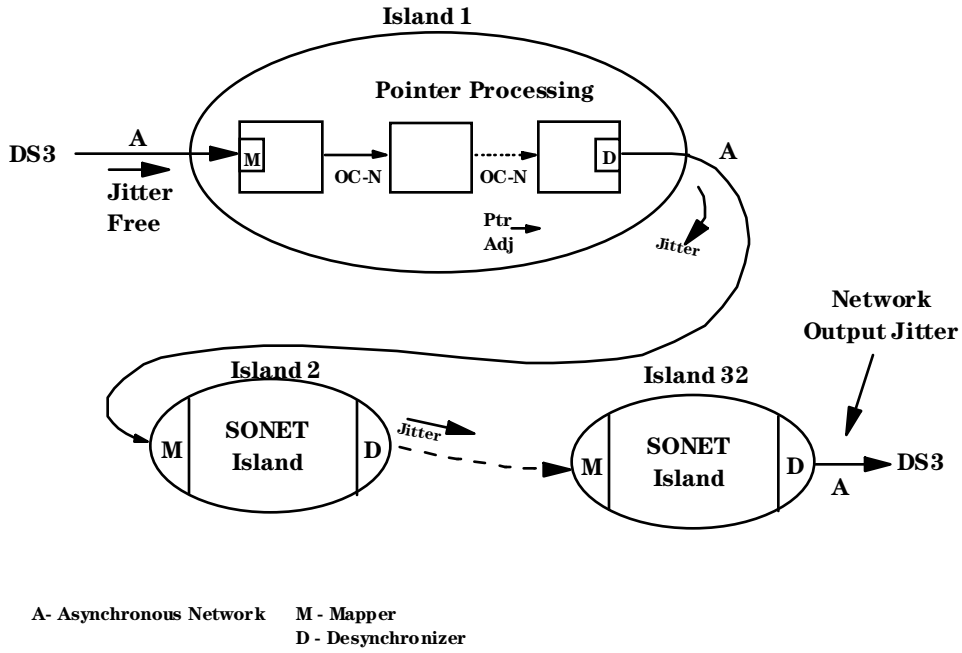


Table 1: ANSI jitter specification for a DS3 signal demultiplexed from a single SDH/SONET island.

Jitter category	Jitter allocation (UI p-p)	
Mapping jitter (Note 1)	A0	0.40
Single isolated pointer	A1	A0 + 0.30
Degraded synchronization conditions	A2	1.3

Notes

1. *Jitter from a SONET island in which there is no pointer activity.*
2. *The DS3 will be jitter free as it enters the SONET island.*

Figure 2(a) : Single isolated pointer test.

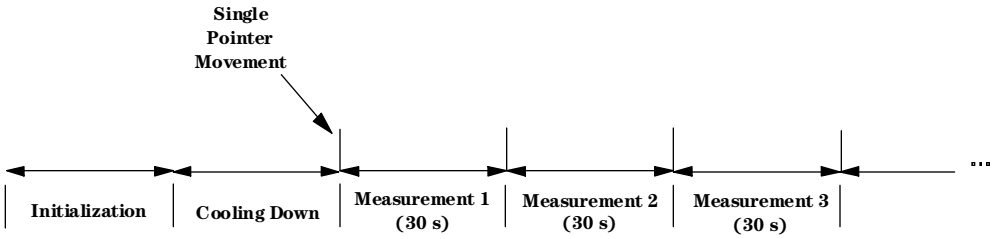
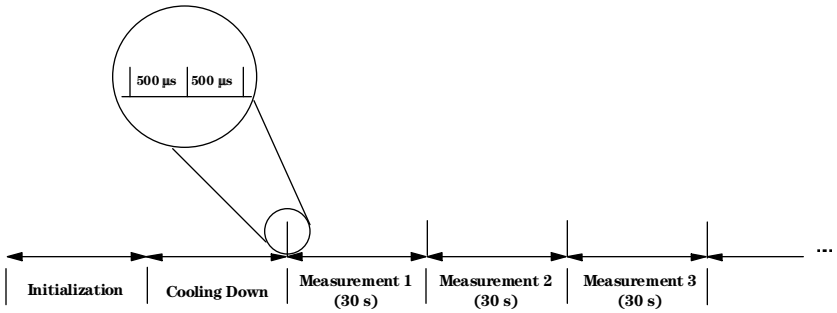


Figure 2(b): Burst-of-3 test.



The new test sequences

The test sequences developed by ANSI have already been accepted for inclusion in G.783 for the North American portions of SDH. It is likely that similar network scenarios will be considered by the Study Group in order to produce test sequences for the CEPT-mapped signal.

The first of the new test sequences was developed to emulate the situation when there is no pointer activity. This test requires the frequency of the tributary signal to be varied to find the maximum jitter produced due to the pulse stuffing ratio used to map the tributary signal into the VC, ie, ***Mapping Jitter.*** This test checks the specification of the maximum jitter on the output due to the process of extracting the tributary signal from the VC.

The second criterion defines the response to a ***Single Isolated Pointer*** movement. This is tested using a sequence which has a single pointer movement every 30 seconds, Figure 2(a). The pointer movements are spaced 30 seconds apart in order to allow time for the effects of each movement to completely die out before another pointer movement is applied. This ensures that the resultant jitter measured is that produced by a single pointer movement.

Two test sequences have been defined to measure the performance of a PTE in a ***Degraded Synchronization Condition.*** The first test emulates the network condition where phase noise in a chain of network elements (eg, ADMs, cross-connects, etc) accumulates to produce a burst of pointers with minimum spacing.

Figure 2(b) shows the test defined to cover this condition. Like the single pointer test, the bursts are set 30 seconds apart to allow time for the effects of each burst to die out before the next burst is applied.

The second test emulates the network condition when the originating PTE loses lock to the system clock. This condition will cause continuous pointer movements to be generated. On top of this background, extra pointer activity may occur due to phase noise from the other nodes of a network. Therefore, on top of the background of continuous pointer movements, an added or canceled perturbation to the background sequence is performed every 30 seconds.

In the original sequences, the clock synchronization loss was represented by continuous evenly spaced pointer movements. However, this is not always the case in practice. Experimentation has shown that gaps are generated in the pointer sequence due to the effects of the positioning of the SDH overhead bytes. For example, when an VC-4 is cross-connected, a repetitive sequence of 87 evenly spaced pointer movements followed by a gap equivalent to 3 missing pointer movements is generated. Table 2 shows the effect on the jitter output from the 87/3 sequence compared to that produced by the original G.783 test.

Similar effects can be predicted for all types of SDH VCs. It is possible by the use of sophisticated pointer processing nodes to remove this effect and produce regular, evenly spaced pointer movements. However, this is not specified as a requirement for the network equipment, and as the most straight forward techniques produce this effect, PTEs will have to be designed to cope with this sequence.

Figure 2(c) shows the new sequence that has been defined to emulate the clock synchronization loss condition for DS3 testing.

Table 2:
Experimental results showing effect of 87/3 sequence.

Pointer sequence	Jitter on demultiplexed DS3 (UIp-p)
G.783 test: regular pointers with one missing pointer	0.15
87/3 sequence	0.60

Notes

1. *In both cases, the pointer spacing was set at 33 ms, equivalent to a frequency offset of 4.6 ppm.*
2. *The results were obtained by testing the DS3 drop port from the HP 37704A SONET test set.*

Figure 2(c): Periodic pointer adjustment test sequence.

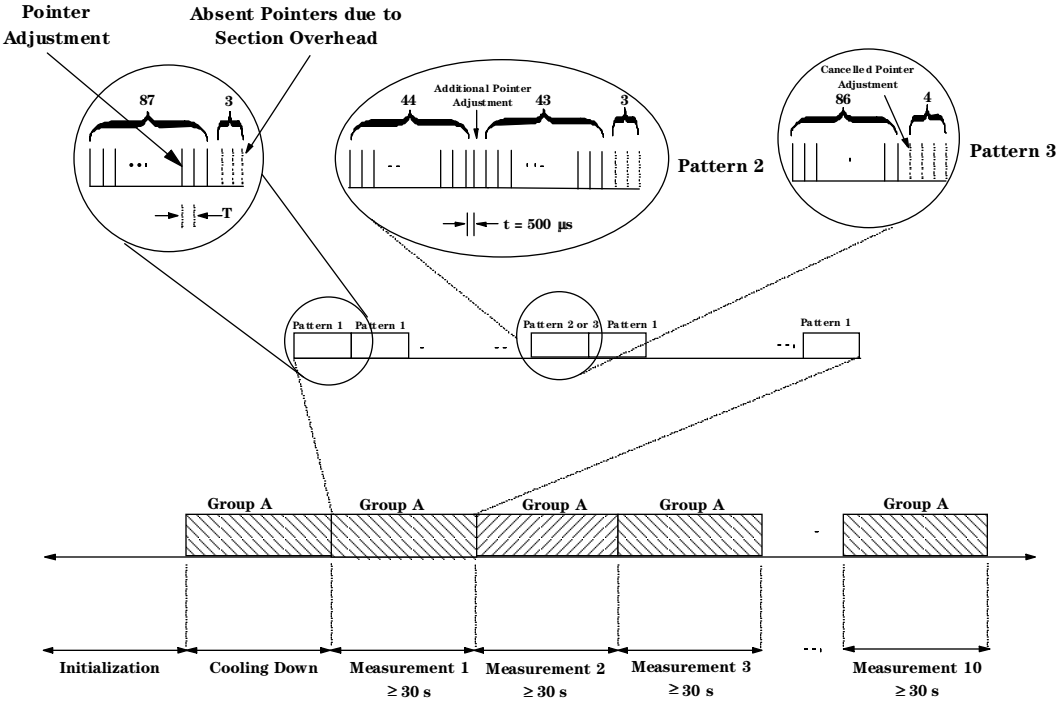


Figure 3: Typical block diagram of a E3 PTE.

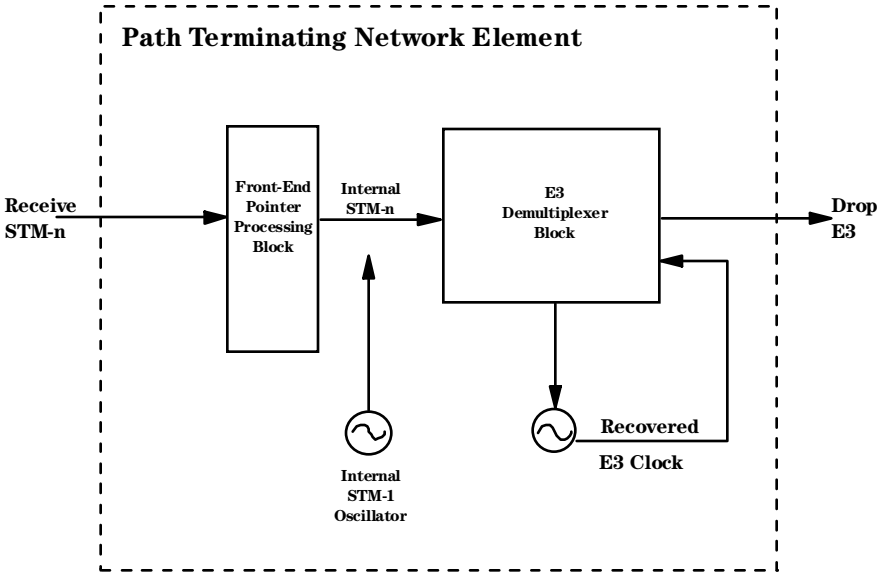
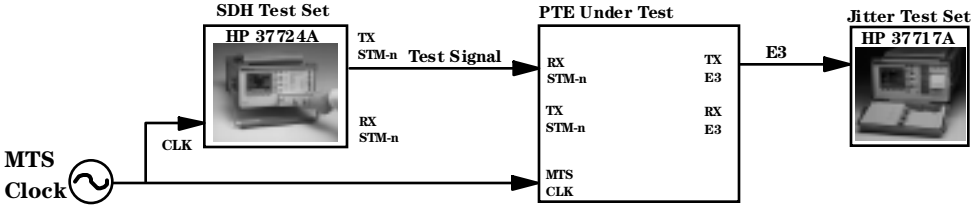
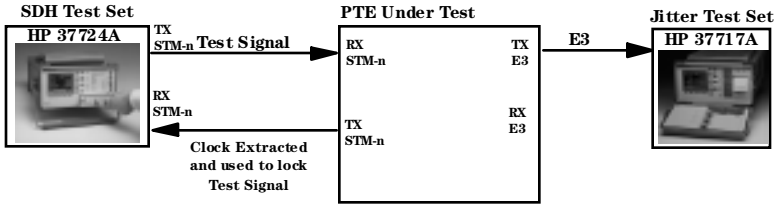


Figure 4: PTE test configuration.



a) Synchronize Test Set to PTE by frequency locking Test Set's Transmitter to the MTS Clock used by PTE.



b) Synchronize Test Set to PTE by frequency locking Test Set's Transmitter to the Clock extracted from the SDH signal generated by the PTE.

Test methodology

As a side-effect of the practical experimentation being carried out, it became clear that there was a need to clarify the test methodology in order to obtain accurate and repeatable measurements. Factors like the number of repetitions of each pointer sequence test are being considered to produce implementation guidelines for each test sequence. Two of the most important requirements arise from the structure of the PTEs available today.

By testing PTEs, it has been found that many contain front-end pointer processing blocks that extract the VC-n from the received signal and pass it into an internally generated STM-n before the signal is demultiplexed to extract the tributary signal, Figure 3.

For effective testing of a PTE with this architecture, it is imperative that the frequency of the internal STM-n signal is locked to the frequency of the test signal being applied to the PTE.
If this is not accomplished, frequency and/or phase differences between the two STM-n signals will produce pointer activity on the internal STM-n signal. These pointer movements will produce spurious spikes of jitter on the tributary signal.
Figure 4 shows two possible test configurations which will synchronize the test signal to the PTE and hence avoid this problem.

The second effect of this structure comes from the elastic store which will be present in the front-end pointer processing block.
This store will absorb some of the pointer activity in the received STM-n signal before producing any pointer movements in the internal STM-n signal. (Cases have been observed where as many as 15 movements are absorbed.)
If a pointer sequence test is performed, it is necessary to prime this elastic store to ensure the pointer sequence applied to the PTE is that which appears at the input to the demultiplexer block. (This can be achieved by applying a test signal containing continuous pointer movements of the same polarity as those used during the testing until jitter spikes are detected on the tributary output each time a pointer movement occurs in the test signal.)

Summary

By tightly specifying the jitter generated by PTEs before there is significant deployment of SDH equipment, network operators can avoid major problems once the multiple SDH island scenario becomes a reality. The definition of sequences which simulate real network conditions, accompanied by test methodology guidelines, will allow network operators to gain confidence that equipment they are installing in their networks will interwork with the existing asynchronous networks both now and in the future.

References

1. T1X1.2, “SONET Hypothetical Reference Circuit (HRC)", T1X1.2/93-015, March 1993.

2. ITU Recommendation G.823, " The Control of Jitter and Wander within Digital Networks which are based on the 2.048 Mbit/s Hierarchy". Vol III - Fascicle III.5, Blue Book.

3. Revised Recommendation G.783, CCITT COM XV-R 110-E, Nov'92.

4 K. Mahon, “Significance of Telecom Canada’s SONET Jitter Accumulation Measurements”, Telecom Canada, T1X1.3/92-129, November 1992.

5. ANSI, "Synchronous Optical Network (SONET): Jitter at Network Interfaces", T1X1.3/ 93-006R3, Aug. '93.

Appendix A

Network emulation model for a SDH test set

Introduction

The fundamental objective of any test set transmitter is to reproduce, in a controllable and repeatable fashion, signals which are true representations of conditions in a real network. To produce a SDH test set which meets these criteria when generating STM-n signals containing pointer movements, the concept of a network emulation model aids in highlighting the important characteristics of such a signal.

An SDH network

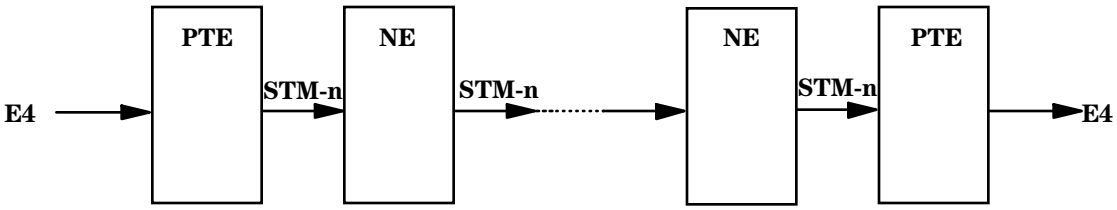
Figure A1 shows a typical SDH transmission network. The tributary signal, which in this example is an E4, enters the network through path terminating equipment (PTE). This element maps the E4 into an VC-4 in the STM-n signal. At the far end, the terminating unit demultiplexes the STM-n signal and reconstitutes the E4 tributary signal. Along the SDH transmission path, the STM-n may pass through various SDH network elements which are pointer processing nodes, eg, digital cross-connects.

At the entry point to the network, the frequency variations from nominal E4 rate are catered for by pulse stuffing the E4 as it is mapped into the VC-4.

There will be no pointer movements in the STM-n signal out of the first element, only variations in pulse stuffing rate (which handles all frequency and phase variations). Pointer movements are induced in the transmission path when an VC-4 is transferred between STM-n signals, ie, as it passes through a network element which is a pointer processing node.

It is important to notice that when a pointer movement is induced in the network, there is no effect on the pulse stuffing ratio used to map the E4 into the VC-4, (as this is always defined at the entry point to the SDH network). Therefore, the pulse stuffing ratio will remain constant during any pointer activity, with this ratio being defined by the long term average VC-4 rate relative to the E4 rate.

Figure A1: Typical SDH transmission network.



Test set emulation model

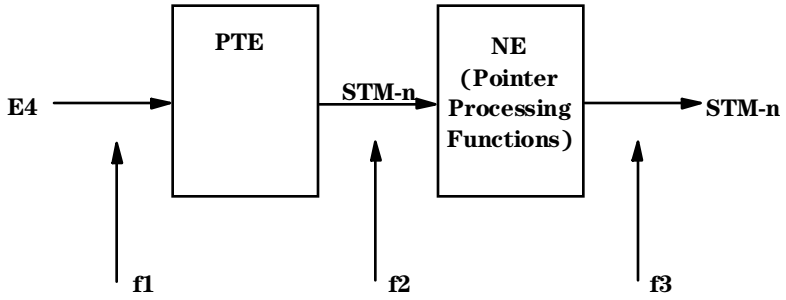
The reduced network model which must be emulated in order to accurately reproduce signals containing pointer movements, consists of a PTE plus a network element which provides pointer processing functions. Figure A2 shows the emulation model. In this model, the pulse stuffing rate is controlled by the relative frequency of the E4 rate (f1) to the internal STM-n line rate (f2). The rate of pointer additions is controlled by the relative frequency of the internal STM-n line rate (f2) to the output STM-n line rate (f3). With this model, (as in the real network), when pointer movements are introduced, there will not be a step change in the pulse stuffing rate around the pointer movement to counteract the apparent step change in VC-4 rate.

The defined pointer test sequences consist of repetitive patterns of pointer movements, all of which are the same polarity. This implies that an offset exists between the line rate (f3) and VC-4 rate (controlled by f2). As the definition for the sequences requires that the line rate remains constant, the internal STM-n (f2) rate must change to generate these pointer movements. Changing f2 will also cause a step change in the pulse stuffing ratio. A step change of this nature would not occur in the network as line frequencies are restricted by network equipment specifications from suddenly changing rate. The cooling down period defined at the start of the sequences provides time for the effects of the step change to die out before the jitter measurements are performed.

Summary

By defining a test set transmitter in terms of a network emulation model, it is possible to highlight, and hence ensure reproduction of the important characteristics of signals containing pointer movements. This model clarifies the need for the pulse stuffing process to be independent from the generation of pointer movements. The implementation of this emulation model in a SDH test set will ensure accurate production of the stimuli required to measure the tributary jitter performance of a terminating PTE.

Figure A2 : Test set emulation model.



Pulse Stuffing Rate controlled by f1 <-> f2

Pointer Movement Rate controlled by f2 <-> f3

Appendix B

Measuring tributary jitter out of an SDH network

SDH tributary jitter characteristics

The innovation of using pointers to track the position of the Virtual Container (VC) within SDH signals has produced many benefits that will minimize the cost and complexity of network equipment. However, due to the large inherent phase step associated with a pointer movement (eg, 24UI per VC-4 pointer movement), compared to that produced by pulse stuffing techniques used in asynchronous multiplexing, the SDH network has the potential of creating large jitter transients in the demultiplexed tributary outputs. Not only are the phase steps much larger, the characteristics of the jitter produced are completely different from these previously experienced in the PDH network.

The effect of pointer movements

Experimentation has confirmed that the jitter created at a demultiplexer output is significantly greater when the SDH signal arriving at the Path Terminating Network Element (PTE) contains pointer movements. One natural phenomenon known as the "87/3" sequence (see Note, Page 14), which occurs in the VC-4 pointer when a node within the SDH network loses timing synchronization, can have the effect of generating large jitter transients. The test results shown in Table 1 highlight the relative magnitude of jitter that can result from each effect.

This table clearly shows the need to test SDH demultiplexing equipment with test signals that contain pointer movements in order to accurately characterize its performance.

Traditional jitter measurement circuits

The jitter that has existed in PDH networks prior to the introduction of SDH has been sinusoidal in nature. Jitter measurement circuits, therefore, were produced that were capable of accurately measuring the peak-to-peak jitter of repetitive waveforms. Figure B.1 shows a typical measurement technique that requires the jitter waveform to be repetitive.

The repetition rate of the jitter transients in the pure PDH network was relatively high (eg, 20 Hz for 2.048 Mbit/s). The carrier frequency recovery circuit, therefore, would track any phase changes at rates less than this bandwidth.

SDH tributary jitter characteristics

A single pointer movement equates to an instantaneous phase step. This causes the output phase of the desychronizer to respond in a similar manner to that shown in Figure B.2. Two effects stop the traditional measurement circuit from giving a true measure of the peak jitter:

1. Positive and negative peaks need to occur within 200 ms of one another, ie, the peak-to-peak value is the difference between the positive reading and the negative reading during a measurement period.

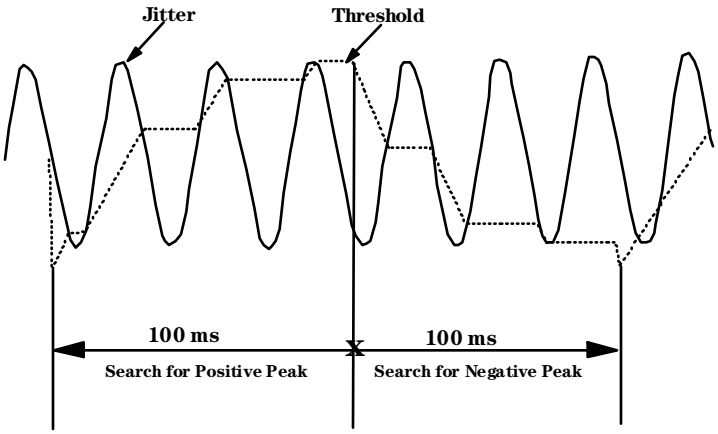
This means that if it is more than 200 ms between the peak values, then the actual peak-to-peak jitter will not be measured.

2. The bandwidth of the circuit used to recover the carrier frequency is such that the recovered clock phase will track transients that last as long as that shown in Figure B.2. When this signal is compared to the input signal in order to measure the jitter, it will not be possible to see the true magnitude of the jitter due to the tracking effect in the reference clock being used.

Table 1:
Experimental results highlighting the relative effect of pointer movements on the tributary jitter.

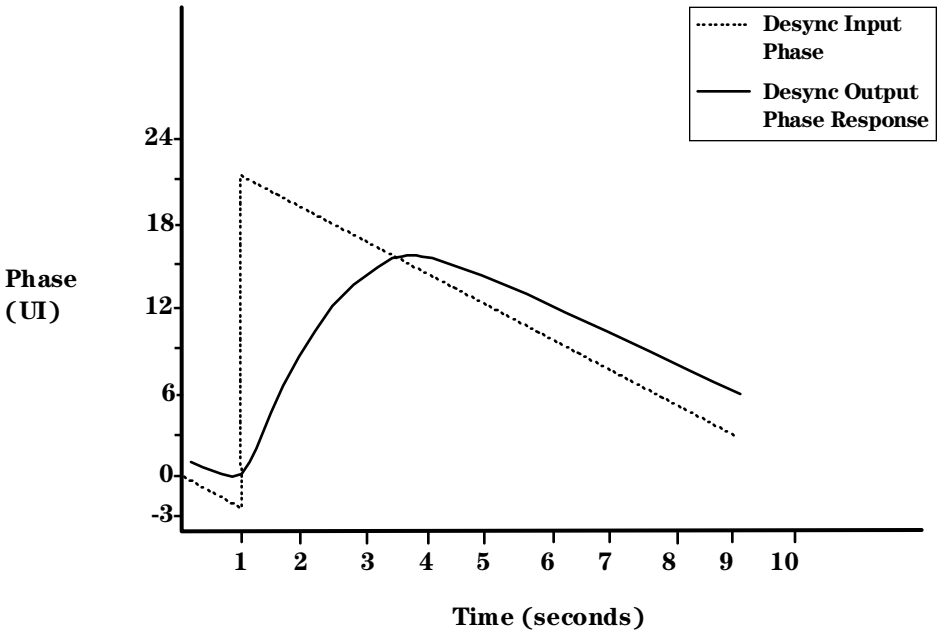
Network condition	Jitter measured (UI p-p)
No pointer movements	0.09
Single pointer movements	0.12
The "87/3" sequence produced when an node is offset by 4.6 ppm	0.60

Figure B.1: Jitter measurement in a PDH network.



The peak-to-peak jitter during the 200 ms measurement interval is the difference between the positive peak in the first 100 ms, and the negative peak during the second 100 ms period. The maximum peak-to-peak jitter during a gating period is the largest value measured during one of the 200 ms measurement intervals.

Figure B.2: Input phase and desynchronizer response in the presence of a single pointer movement.



HP 37717A jitter measurement circuit

The jitter measurement module for the HP 37717A PDH/SDH BER and jitter test set is the first in a new generation of jitter measurement implementations. To allow accurate measurement of jitter created by the SDH network into the PDH network, the following techniques have been employed:

1. The voltage-controlled oscillator (VCO) used to track the carrier frequency signal being received has a bandwidth of 4 Hz. This will provide a better reference for the measurement of long transients produced by pointer activity.

2. Separate positive and negative peak detectors will ensure that all spikes of jitter are captured irrespective of when they occur within the measurement period.

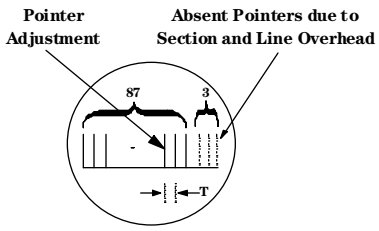
3. The maximum peak-to-peak jitter displayed by the instrument will be the difference between the positive and negative peaks within the *gating period*, ie, the use of fixed measurement periods within the gating period will no longer be employed.

By the use of these techniques, the HP 37717A provides a jitter tester that will give accurate measure of jitter in a PDH signal, irrespective of the network topology that the signal has passed through.

Note

The "87/3" sequence

When a pointer processing node which is cross connecting VC-4 payloads loses lock to the master timing source in the network, the frequency difference between the free-run reference in the network element and the master timing source will have the effect of generating evenly spaced pointer movements, T seconds apart. However, rather than continuously evenly spaced pointer movements, some equipment produces a $90 \times T$ seconds sequence in which a pointer movement occurs during the first 87 periods but no pointer is produced during the last 3 periods, ie, an "87/3" sequence. This effect is caused by the positioning of the Section Overhead within an SDH frame. The cross-connection of other payloads can also have an effect of producing repetitive sequences of unevenly spaced pointer movements.



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