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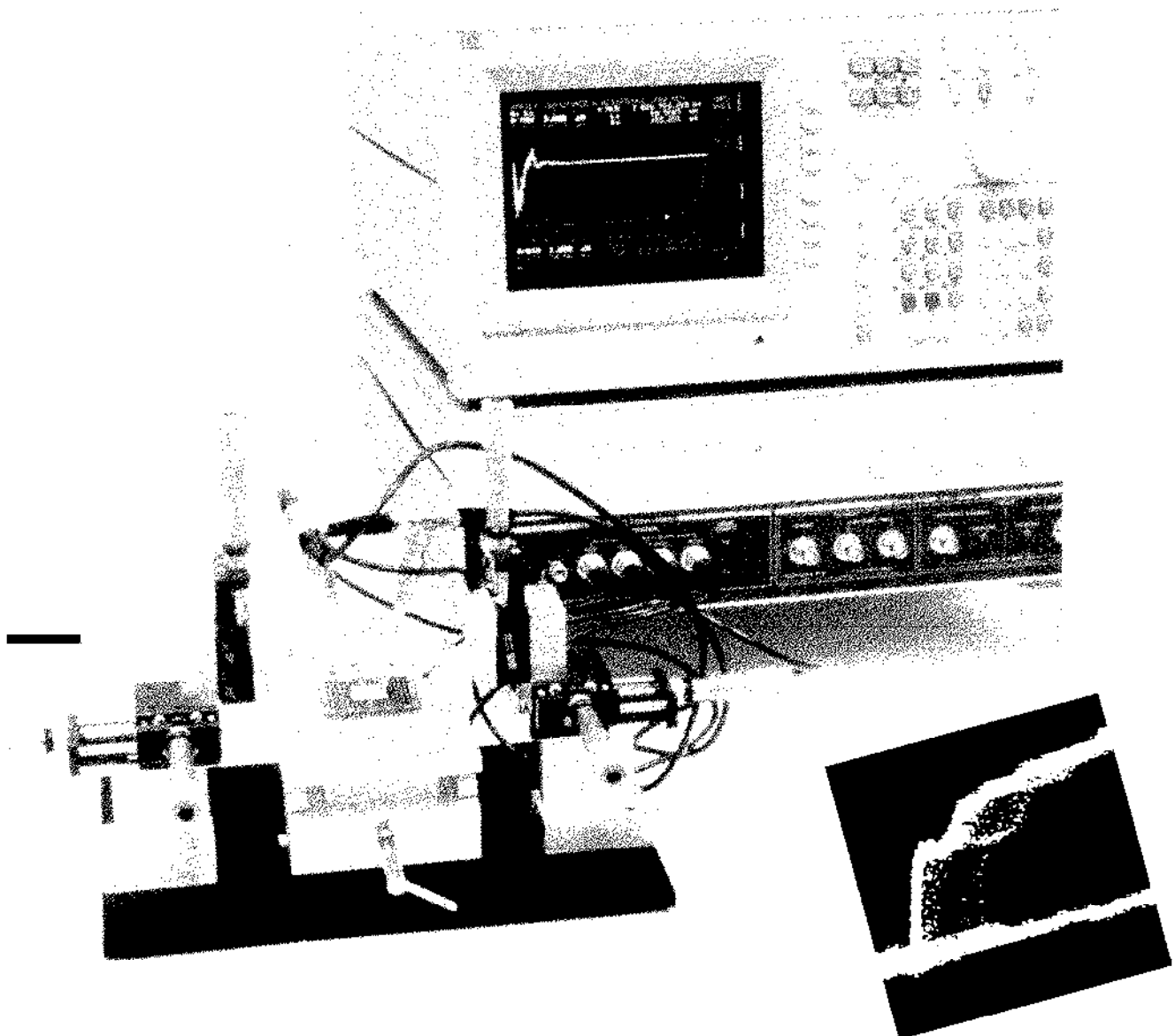
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Characterizing IC Packages with Impedance Measurements and the UTP-3000 Test Fixture

Application Note 1210-1



"Digital Design and Test Solutions from HP"

Characterizing IC Packages Through Impedance Measurements

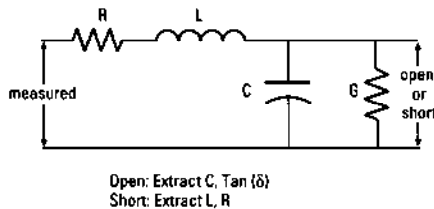


Figure 1. Lumped circuit model of package

Increased clock speeds in digital systems mean that the IC package can no longer be considered electrically transparent. The parasitic effects from adjacent signal traces and power distribution networks affect circuit performance. Propagation delays, simultaneous switching noise, cross talk, and signal integrity are affected by the capacitive and inductive effects of the package. An accurate package model can be used in simulations (such as SPICE) to ensure that the system will meet performance and reliability objectives.

A SPICE compatible IC package model begins with a simple lumped circuit (see figure 1). This model adequately describes the electrical performance of most packages (DIP, QFP, PGA, and LCC) for bandwidths of over 500 MHz.

An impedance analyzer, such as the HP 4194A, can be used to test the package and extract the values of the parasitic elements in the lumped circuit model. These values and the model can be used to generate a SPICE "deck" for electrical simulation of the package.

The impedance analyzer measures the complex current through a device and measures the complex voltage across it. The analyzer uses this data to calculate the complex impedance or admittance for the device. The impedance/admittance data can then be interpreted in terms of a lumped circuit model.

The analyzer is used to probe one end of a trace and the ground plane. If the far end of the trace is open, the trace and ground plane have capacitance. If the far end is shorted, the trace and ground plane form an inductor. Thus, there is only one reactive component for most measurements, and the analyzer can display the results directly as capacitance or inductance versus frequency.

Using an impedance analyzer is straightforward. First, you compensate the analyzer for the parasitics present in the probes and the fixture. Then, you measure the capacitance of an open signal trace and the inductance of a closed signal trace. Finally, you decide whether the values and circuit model describe the package, and determine the maximum frequency for which the model is valid.

The Problem

A design engineer has samples of a PGA package that he is planning to use for a new ASIC. He wants to measure the parasitics of the package and to use the information in a SPICE simulation of the combined package and ASIC.

The Investigation

The engineer used the following instrumentation:

HP 4194A Impedance/Gain-Phase Analyzer
Inter-Continental Microwave UTP-3000 Test Fixture

Before making any measurements, the engineer set up the test fixture and compensated the analyzer for the parasitics present in the probes and fixture. (See "Comments on the Test Setup.")

The engineer needed to measure the parasitic capacitance between a signal trace and ground. He inserted the package into the UTP-3000 test fixture and positioned it so that the probes contacted the signal trace input and the ground lead. The opposite end of the signal trace is left open for this measurement. The circuit model is a simple parallel capacitor, C_p , and resistor, R_p . (At low frequencies, the series inductance and resistance components are negligible.) The HP 4194A FUNCTION menu allows measuring either the C_p - R_p or C_p -D model (D is the dissipation factor).

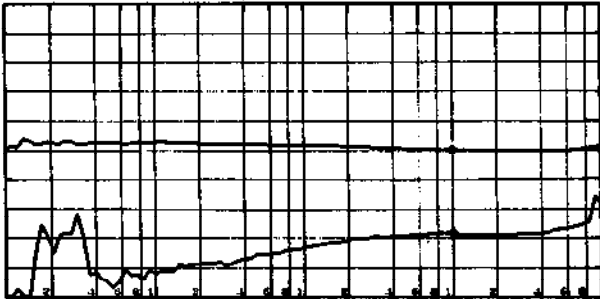


Figure 2. Capacitance of open signal trace

After probing the package, the engineer selected the C_p -D model. The HP 4194A measures the impedance of the device, subtracts the compensation, and displays the result as a function of frequency (see figure 2). The capacitance of this signal trace is 2.52 pF, and it remains constant from 1 kHz to 10 MHz. The flat response shows that the circuit model was adequate for the measured bandwidth. The dissipation factor is 0.022, and is nearly constant above 50 kHz. This is typical of the FR4 material used in this package.

To measure the inductance of the signal trace, he removed the package from the fixture and bonded a wire between the far end of the signal trace and package ground. Now the parallel capacitance and resistance of the trace are shorted out. The circuit model for the modified circuit is a series resistor, R_s , and series inductor, L_s .

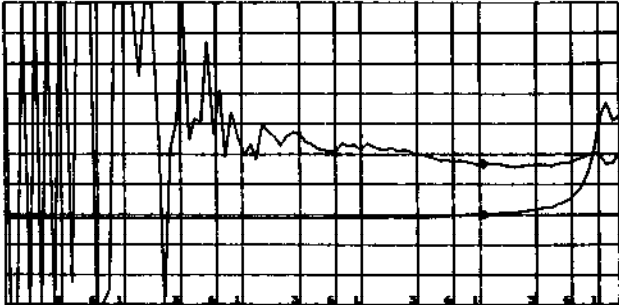


Figure 3. Inductance of signal trace

After inserting the package into the fixture, the engineer selected the L_S - R_S model from the FUNCTION menu. Figure 3 shows the results. Below 10 kHz, the inductance measurement is dominated by system noise. From 10 kHz to 15 MHz, the inductance remains constant at 11.7 nH. Thus, the circuit model is adequate to 15 MHz.

The series resistance, R_S , shown in figure 3, is approximately 0.1 Ω . This is dominated by the contact resistance of the probes, and it is unlikely to affect circuit performance. For most applications, R_S values less than 0.5 Ω will not affect performance. If the series resistance is important, the four terminal mode of the impedance analyzer should be used to make an accurate measurement.

$$Z_0 = \sqrt{L/C}$$

Equation 1. Characteristic impedance

Now that the engineer knew the values of the parasitics for the signal trace, he could calculate additional data and could evaluate the validity of the model. The signal trace was fabricated as a controlled impedance microstrip. Given the measurement results, he used equation 1 to calculate the characteristic impedance of the trace. He used the series resistance (0.1 Ω), series inductance (11.7 nH), and shunt capacitance (2.52 pF) to obtain a characteristic impedance of $Z_0=68 \Omega$.

$$f_{\text{resonance}} = \frac{1}{2\pi\sqrt{LC}}$$

Equation 2. Resonant frequency

The lumped circuit model was verified only to the measurement bandwidth of 15 MHz. However, the engineer knew that the model would be adequate to a bandwidth near the self-resonant frequency of the circuit (see equation 2). The resonant frequency for this particular circuit is over 900 MHz. Therefore, though the measurements were performed at relatively low frequencies, the model is likely to be accurate to well over 500 MHz.

Parasitics present in the package power and ground distribution can affect system performance. They contribute to power supply instability that is reflected in poor signal integrity. The parasitics include capacitance added by the power and ground planes, chip capacitors, via holes, and via pads.

Before measuring these parasitics, the engineer replaced the old sample with a new one. (The bond wire added for the inductance test isn't needed for the power and ground measurements.)

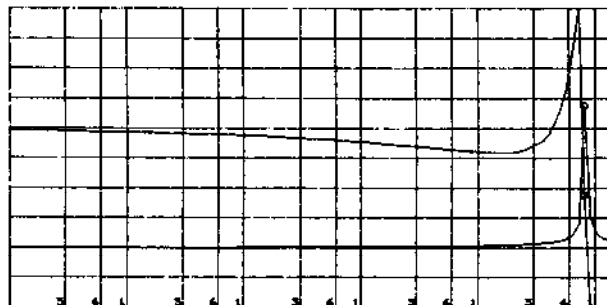


Figure 4. Power/ground capacitance

He inserted the new package in the fixture and probed the power and ground leads. (The inner cavity pads of the package were left open.) The equivalent circuit for the measurement is a simple parallel capacitor and resistor.

The engineer selected the dissipation factor measurement (C_p -D). Figure 4 shows the results. He noticed that for frequencies below 3 MHz, the capacitance was reasonably flat. However, it rose dramatically above 3 MHz, which shows that the simple parallel circuit model breaks down at that frequency. The engineer thought about the problem, and decided that a series R, L, and C circuit would be more appropriate.

The HP 4194A Equivalent Circuit Analysis Function can fit five different lumped circuit models to a data set. The engineer wanted to use this function to find the values of R, L, and C in the new model. First, he displayed the impedance data from the measurement, then selected the EQV-CKT function, and chose the series LCR circuit as the model. The HP 4194A calculated the values as $R=0.053 \Omega$, $L=4.9 \text{ nH}$, and $C=74.3 \text{ nF}$.

To see how well the calculated component values and circuit model fit the data, the engineer pushed the SIM-f button. Figure 5 shows the measured impedance data, with the simulated impedance data for the equivalent circuit model superimposed as dashed lines.

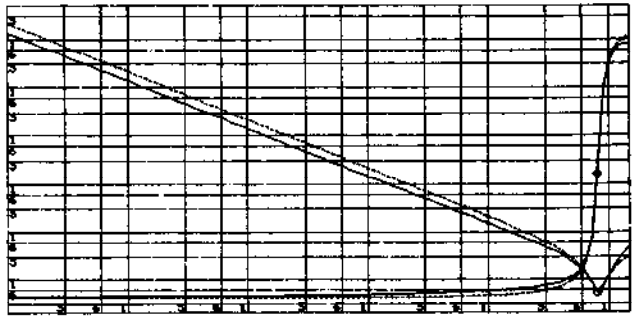


Figure 5. Equivalent circuit matching

The match between the two models was quite good, so the engineer recorded this information for use in the SPICE model.

Summary

By using the HP 4194A Impedance Analyzer to extract parasitic values of a package, the engineer was able to derive a lumped circuit model for SPICE simulation. He determined that the model would be adequate for frequencies beyond 500 MHz.

Using an impedance analyzer to measure package characteristics for use in modeling can help verify performance in real applications. For very high frequencies, Time Domain Reflectometer/Time domain Transmission (TDR/TDT) and Network Analysis techniques can provide more direct verification of package performance.

Complete Electrical Characterization of Packages

The HP 4194A is useful for extracting parameters needed for SPICE models. This application note describes techniques for measuring certain package parameters. You can use similar techniques to get other useful data for models, including lead resistance, the inductance matrix, and the capacitance matrix.

Other techniques can be used to find the frequency dependence of real/imaginary components of the dielectric constant, and the permeability/resistivity of conductors.

Comments on the Test Setup

Typical parasitic values of capacitance and inductance for a package are 10 pF and 10 nH. You must be careful when selecting probes and fixtures for an impedance measurement because these tools will have comparable parasitic values, which can cause significant measurement errors.

To select probes and fixtures, look for low parasitic values, easy adjustability, and rigid geometry. The Inter-Continental Microwave UTP-3000 test fixture is a good example. The fixture has two transitions that are independently adjustable in the X, Y, and Z planes. The pin under test inserts into the test fixture transition, making an accurate RF connection. The device is placed on a platform and raised into position for measurement. Thus, the probes can be positioned, then compensated, which ensures accuracy.

The HP 4194A is a four-terminal instrument. It can be converted to a two-terminal instrument, which simplifies alignment and allows accurate compensation for most impedance measurements. The conversion must be done near the probe tips, and the probe shields must be connected to complete the current path. See the *HP Impedance Measurement Handbook* (HP P/N 5950-3000) for a detailed description.

To compensate for the effects of the probes and fixtures, align the probes with the package leads that will be tested. Then remove the package from the fixture, and press the "open compensation" button on the HP 4194A. This measures the open-circuit capacitance of the test setup. Next, insert the UTP-3000 "short" standard into the fixture and move it into contact with the probes. Press the "short compensation" button. The HP 4194A measures the short-circuit inductance of the setup.

The HP 4194A stores these compensation values. When you make an impedance measurement, the analyzer will automatically subtract these values from the measurement and display the compensated results.

Once you have compensated the fixture for a particular measurement, don't touch or move the probes or leads. This will affect the compensation, causing measurement errors.

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