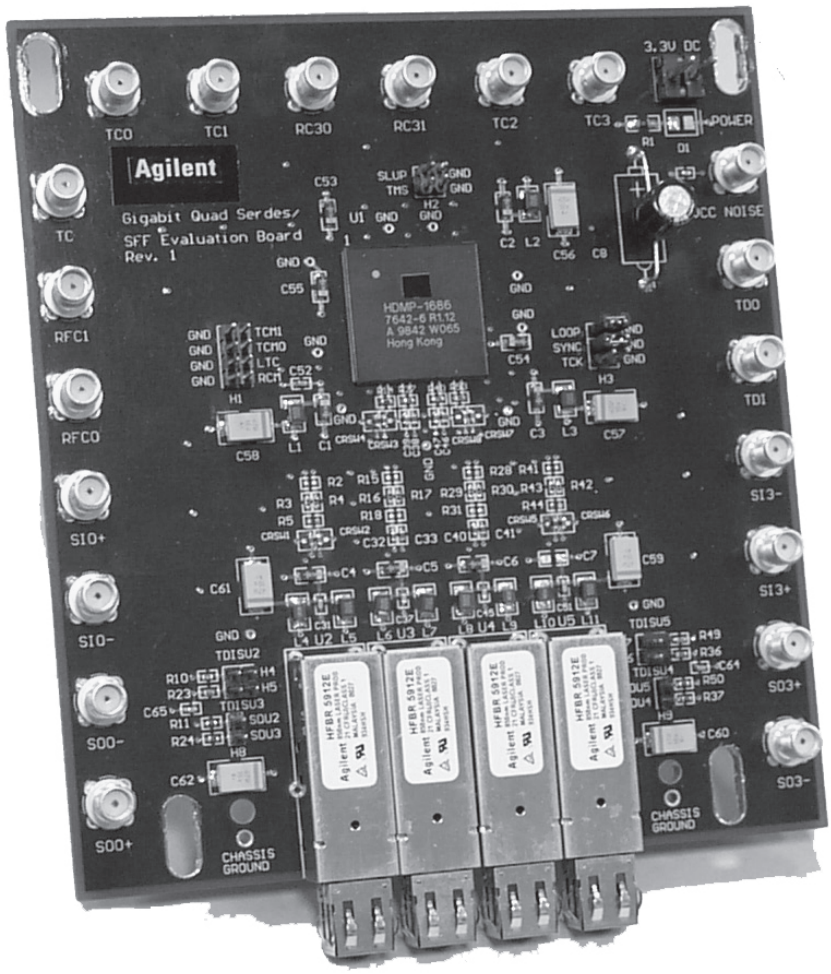
Agilent 1.25 Gb/s Quad SerDes/ Small Form Factor Transceiver Reference Design

Application Note 1200



Reference Board Introduction

The purpose of the 1.25 Gb/s Quad SerDes/Small Form Factor (SFF) transceiver reference board is to demonstrate interoperability between the Agilent HDMP-1687 Quad SerDes IC and the Agilent HFBR/HFCT-5912 SFF's. The board also allows the user to either connect to the SFF or via SMA connectors to the high speed serial ports of the HDMP-1687 IC for individual characterization.

Description

The Agilent HDMP-1687 IC is a complete quad channel 1.25 GBd Gigabit Ethernet transceiver contained within a 208 pin BGA package. The IC contains all the necessary high frequency circuitry, clock recovery and mux/demux functions to perform in accordance with the specification for IEEE 802.3z Gigabit Ethernet. For more information on this component reference should be made to the Agilent technical data sheet.

The Agilent HFBR/HFCT-5912 has an optical transmitter and receiver contained within a new industry standard 2 x 5 DIP style package, with an MT-RJ fiber connector interface. The transceiver performs all light-to-logic functions in accordance with the specification for IEEE 802.3z Gigabit Ethernet. For more information on this component reference should be made to the Agilent technical data sheet.

Figure 1 shows the location of the main components on the reference board, Table 1 shows the component functions and identifications and Figure 2 shows a block diagram of the reference board where each channel of the HDMP-1687 is connected to a corresponding SFF (U2,U3,U4,U5). The serial data output from the SFF is converted to parallel data by the HDMP-1687 and vise-versa. The parallel outputs from the HDMP-1687 are looped back to the parallel inputs. Since the traces of the parallel loop back lines were required to be of approximately equal length the number of board layers was twelve. If these two requirements were eliminated, the number of required board layers would be significantly less.

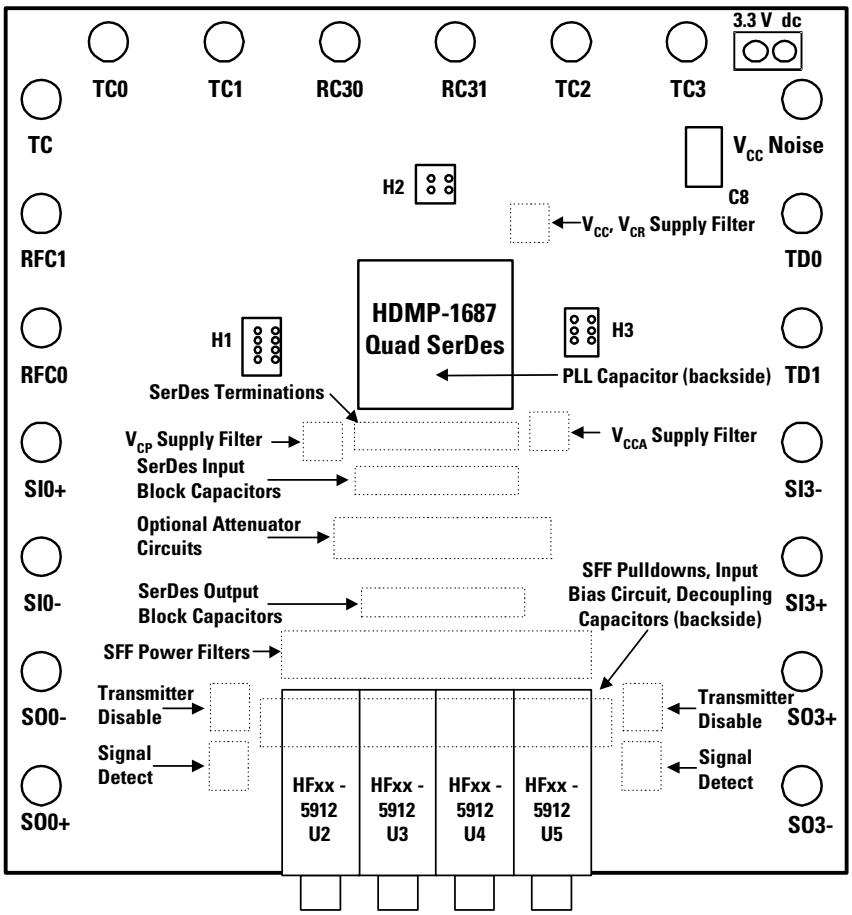


Figure 1. Main Components of the Reference Board

Table 1. Component function and Identification

Function	Component Identification
V_{CC}, V_{CR} Supply Filter	L2, C2
PLL Capacitor	C10
V_{CCA} Supply Filter	L3, C3
V_{CP} Supply Filter	L1, C1
SerDes Terminations	R14, R27, R40, R53
SerDes Input Block Capacitors	CRSW3, CRSW4, CRSW7, CRSW8. C38, C39, C46, C47.
Optional Attenuator Circuit	R2, R3, R4, R5, R15, R16, R17, R18, R28, R29, R30, R31, R41, R42, R43, R44.
SFF Power Filters	C4, C5, C6, C7, C31, C37, C45, C51. L4-11.
SerDes Output Block Capacitors	CRSW1, CRSW2, CRSW5, CRSW6, C32, C33, C40, C41.
SFF Pulldowns, Input Bias Circuit, Decoupling Capacitors	R6-9, R12, R13, R19-22, R25, R26, R32-35, R38, R39, R45-48, R51, R52. C28-30, C34-36, C42-44, C48-50.
Transmitter Disable	H4, H5, H6, H7. R10, R23, R36, R49.
Signal Detect	H8, H9. R11, R24, R37, R50.

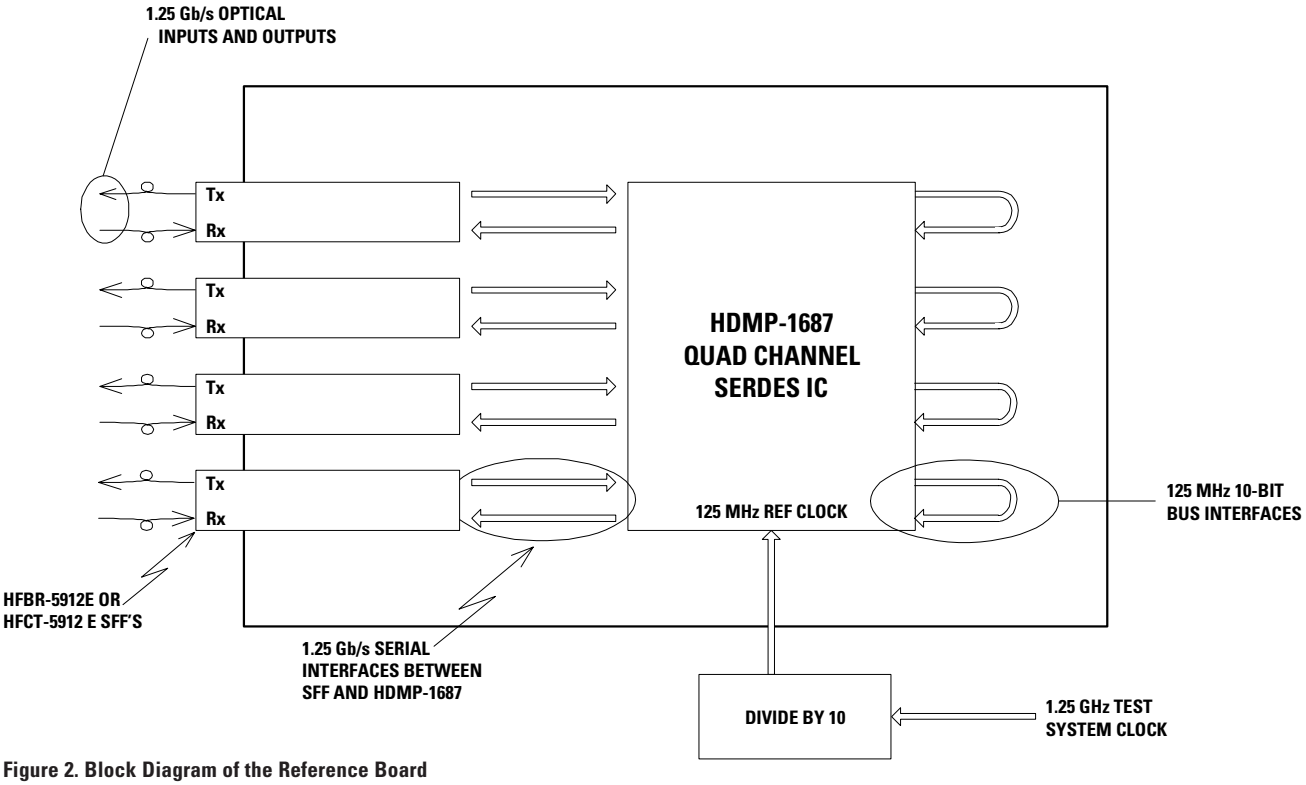


Figure 2. Block Diagram of the Reference Board

Functionality

Tables 2, 3 and 4 describe the available options on the reference board.

For recommended circuit schematics refer to Application Note 1201 Reference Design Guidelines for Gigabit Fiber-Optic Datacom Systems Implemented with MT-RJ Small Form Factor Modules.

Channels U2 and U5 have been configured to enable the user to drive or observe the HDMP-1687 or the SFF separately. This is achieved via capacitors CRSW1, CRSW2, CRSW3 and CRSW4 for channel U2 and via capacitors CRSW5, CRSW6, CRSW7 and CRSW8 for channel U5.

Figure 3 shows the orientation of channel's U2 and U5 capacitors to enable the available user options.

In the following section the corresponding channel U5 capacitor identifications are shown in ( ).

For channel U2 (U5), the capacitors CRSW1 (CRSW5) and CRSW2 (CRSW6) can be placed in three possible positions. In position 'A' the HDMP-1687 Quad SerDes IC is connected to the SFF. In position 'B' the outputs from the HDMP-1687 IC are connected to SMA connectors SO0± (SO3±). In position 'C' the SFF's transmitter inputs (TD±) are connected to SMA connectors SO0± (SO3±).

The remaining channel U2 (U5) capacitors CRSW3 (CRSW7) and CRSW4 (CRSW8) can also be placed in three possible positions. In position 'A' the HDMP-1687 Quad SerDes IC is connected to the SFF. In position 'B' the inputs from the HDMP-1687 IC are connected to SMA connectors SI0± (SI3±). In position 'C' the SFF's receiver outputs (RD±) are connected to SMA connectors SI0± (SI3±).

Table 2. Reference Board SMA Assignments

SMA Name	SMA Function	Comments
RFC1	Reference Clock input.	Use divide by 10 circuit to generate 125 MHz reference clock input from test systems 1.25 GHz clock output.
SO[0,3]±	High Speed Serial Differential SMA connectors for channels U2 and channel U5.	Use to drive SFF Transmitter inputs (TD±) or observe Quad Serdes high speed serial outputs (SO±).
SI[0,3]±	High Speed Serial Differential SMA connectors for channels U2 and channel U5.	Use to drive Quad Serdes' high speed serial inputs (SI±) or observe SFF receiver outputs (RD±).
RC3(0,1)	Channel U5 receivers' byte clocks.	A 125 MHz receiver byte clock appears on RC31 when RCM=1. 62.5 MHz receiver byte clocks appears on RC30/31 when RCM=0.
V_{CC} NOISE	V_{CC} noise input	Input is ac coupled to V_{CC} plane.
RFC0,TC, TC[0-3], TDO, TDI	Unused SMA connectors.	

Table 3. Reference Board Jumper Assignments

Header Name and Number	Header Function	Comments
LOOP (H3)	Loopback Enable Input.	"0"= use jumper for no serial loopback "1"= use no jumper to enable serial loopback..
RCM (H1)	Receivers Clocking Mode (called RCM0 on 1686 chip)	"0"= use jumper for half speed receiver clocks, RCx(1-0). "1"= use no jumper for full speed receiver clock, RCx1
SYNC (H3)	Enable Byte Sync Input.	"0"= use jumper for no comma sync. "1"= use no jumper to enable comma sync.
TDISU2 (H4) TDISU3 (H5) TDISU4 (H6) TDISU5 (H7)	SFF[U2-U5] Transmitter Disable	
SDU2 SDU3 (H8) SDU4 SDU5 (H9)	SFF[U2-U5] Signal Detect	
TCK (H3) SLUP (H2) TMS (H2) TCM[0-1] (H1) LTC (H1)	Unused headers.	

Table 4. Reference Board Power Pin Assignments

Pin Name	Pin Description
3.3 V	Common 3.3 V power supply
DC	Common ground

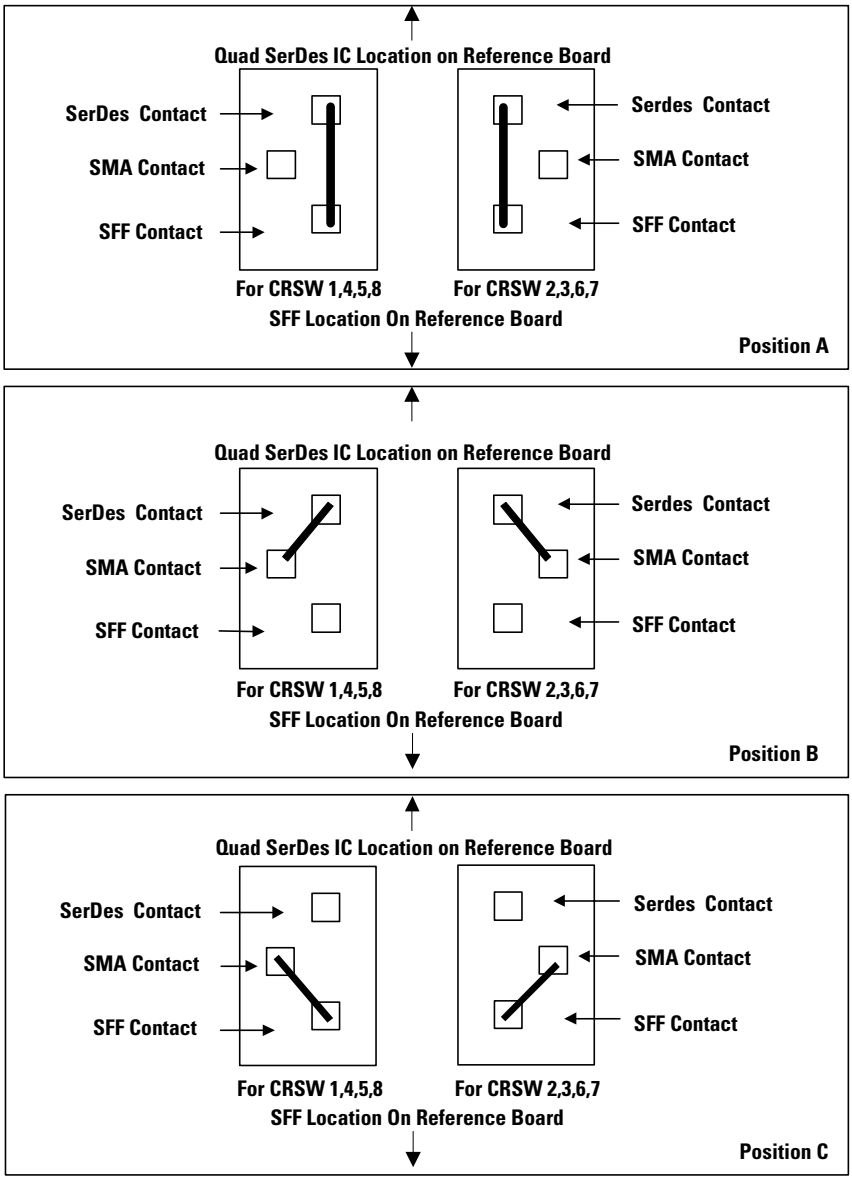


Figure 3. User Available Test Options For Channels U2 and U5.

Reference Board Testing

To start evaluation of this board where electrical input and output from the board is required, the configuration shown in Figure 4 can be used.

A +3.3 V supply should be applied to the '3.3 V' terminal and ground should be applied to the dc terminal. A 125 MHz reference clock (divided down from 1.25 GHz test system clock) should be connected to SMA connector RFC1. An optical cable should be connected between channels' U4 and U5 SFF.

The BERT outputs a serial 2^7-1 PRBS pattern (closest to 8B10B coding used in Gigabit Ethernet) at 1.25 GHz and verifies the same pattern is received back, error free.

A variable delay line may be required to phase shift the Quad SerDes chip's reference clock (RFC1) relative to its transmit data (TX[0-9]). This phase shift may be required to meet the chip's transmit setup and hold times. Usually, this delay is not needed.

In Figure 4 channel U5's transmitter is driven from the BERT and converts the electrical data from the BERT into an optical output. The optical output is then connected to the receiver of channel U4 and converts the optical input into an electrical output for transfer into the Quad SerDes IC. The Quad SerDes converts the received serial data into parallel data and vise versa. Serial data is presented to U4's transmitter for conversion to optical output and this is connected to U5's receiver. The electrical outputs from U5's receiver is routed back to the BERT via SMA connectors SI3±.

For this test configuration capacitors CRSW5, 6, 7, and 8 should be placed in Position C, as shown in Figure 3, so that channel U5's SFF is connected to the SMAs. On header H3, LOOP should be set to '0' by fitment of 'jumper' connector to activate the Quad SerDes high-speed serial ports (SI[3-0]±, SO[3-0]±) and Comma detection should be disabled (SYNC=0). This can be done by applying a jumper onto the "SYNC" header (H3). If "SYNC" is enabled, some bits prior to any comma character could be lost; resulting in the BERT flagging errors.

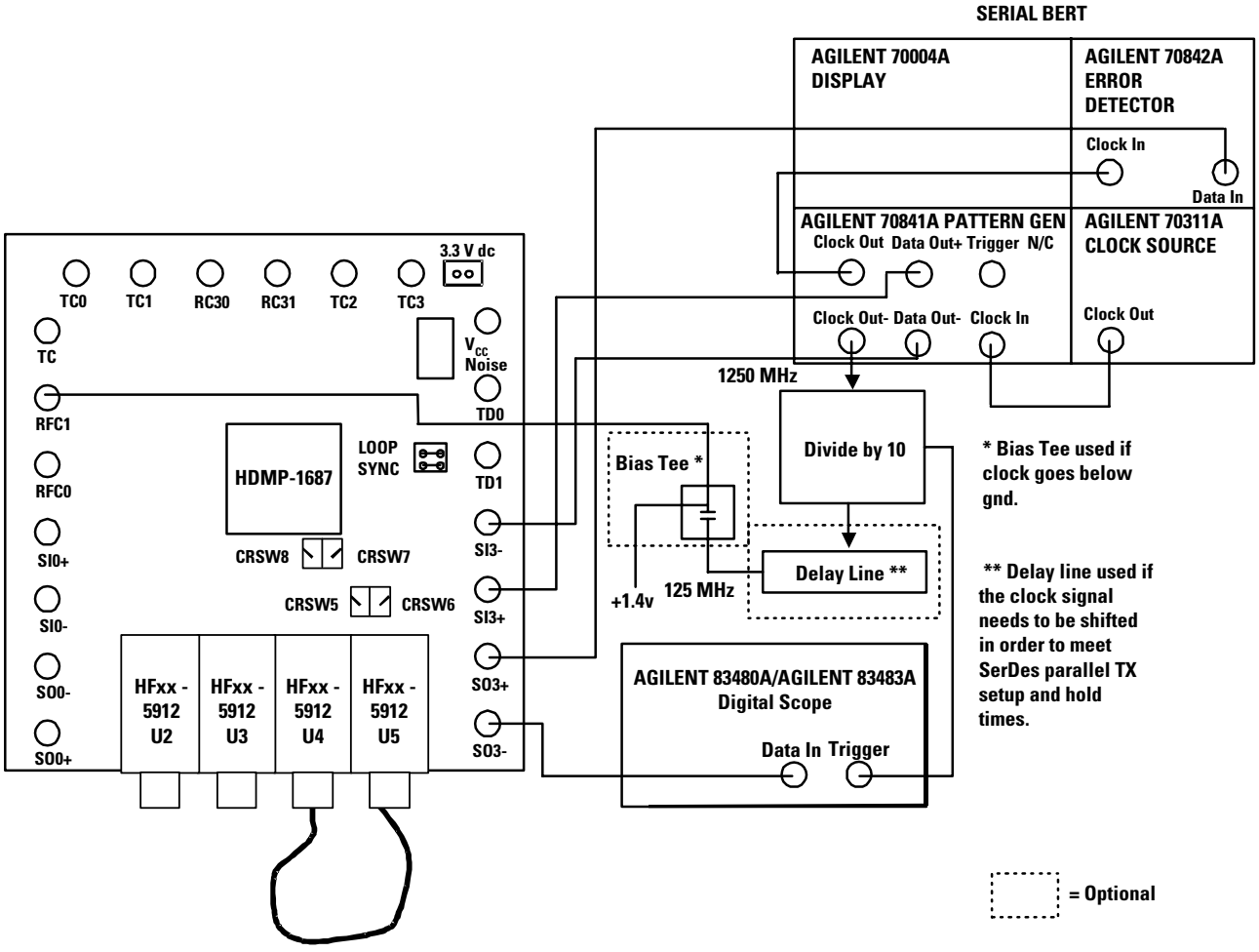


Figure 4. Test Setup with Reference Board

If the BERT reports errors, it is possible that the setup or hold time of the BERT's data input may be violated, or that the setup or hold time of the SerDes' transmitter may be violated. To correct these problems the BERT's data input/clock timing can be adjusted by using the BERT's "CLK_Dat Align" command or the BERT's input data timing can be adjusted by using the BERT's "Dat I/P Delay" command. Alternatively the transmit data timing can be modified by varying the BERT's "Dat O/P Delay", by interrupting the V_{cc} to the evaluation board, or by changing the value of the RFC1 delay line.

Divide By Ten Circuit

Figure 5 shows the circuit schematic for the "Divide by 10" circuit, as used and shown in Figure 4. The circuit uses a Motorola MC12080D prescaler IC (U1) to divide the incoming Clock down from 1.25 GHz to 125 MHz. This is followed by two Motorola MC100ELT21D PECL to TTL converters (U2,U3).

Warning

For the evaluation board to operate properly, the setup and hold times of the Quad SerDes' parallel inputs (TX[3-0]{0-9}) must not be violated. Since the SerDes' parallel I/Os are connected together on this evaluation board, an important factor in avoiding this violation is which ten serial bits are used to generate the parallel word (RX[0-9]) and when this word is sent to the SerDes transmitter inputs. After each power up, the timing of the SerDes' receiver and when the parallel word is sent will be different. As a result, setup and hold time violations may occur when the evaluation board is powered up or when the SerDes' receiver timing is interrupted. These setup and hold time violations may cause bit errors, distorted/poor eye diagrams, or loss of eye. In a user's system, this problem will not occur since the SerDes' parallel I/Os will not be connected together. The evaluation board's setup or hold time violations can be corrected by interrupting the board's dc power supply one or more times.

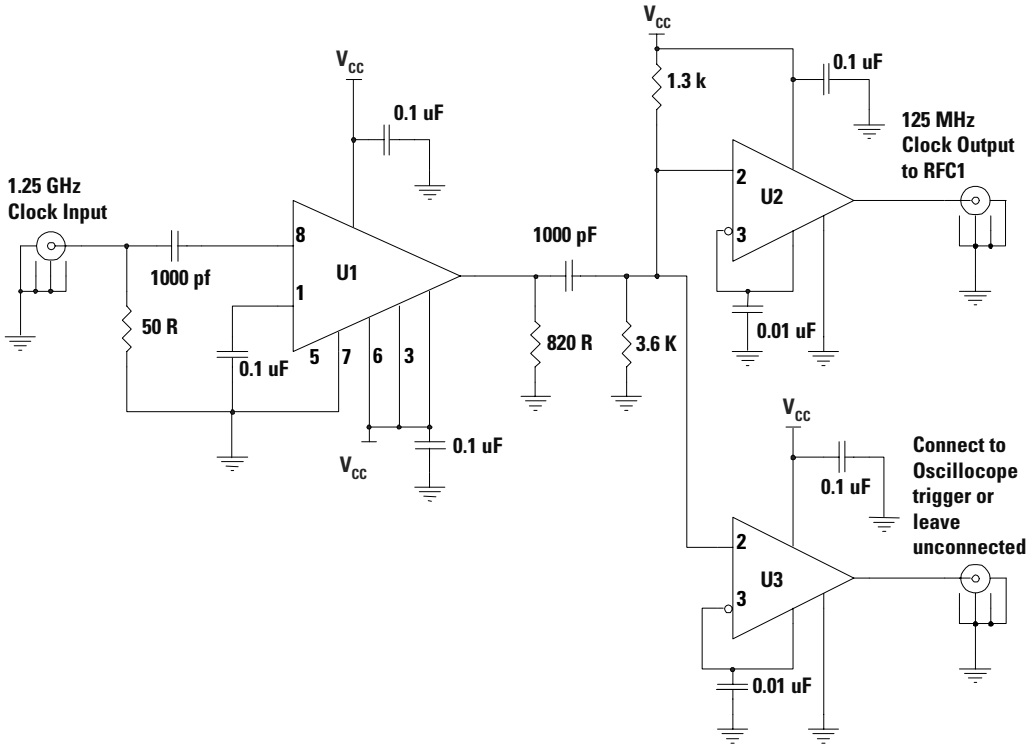


Figure 5. Divide by Ten Circuit.

Testing

The following sections describe the testing carried out for the Small Form Factor (SFF) HFCT-5912E and HFBR-5912E transceivers on the HDMP-1687 Quad SerDes SFF reference design board. Figure 6 shows the test configuration used to collect data presented in the following sections. The multimode 850 nm HFBR-5912E transmitter optical output can be viewed using plug-in module Agilent 83487A on the Digital Communications Analyzer while the Agilent 83486A plug-in module be used with the single mode 1300 nm HFCT-5912E transmitter. Both of these modules have 4th Order Bessel Thompson Filters and were used for measuring transmitter jitter and eye mask compliance.

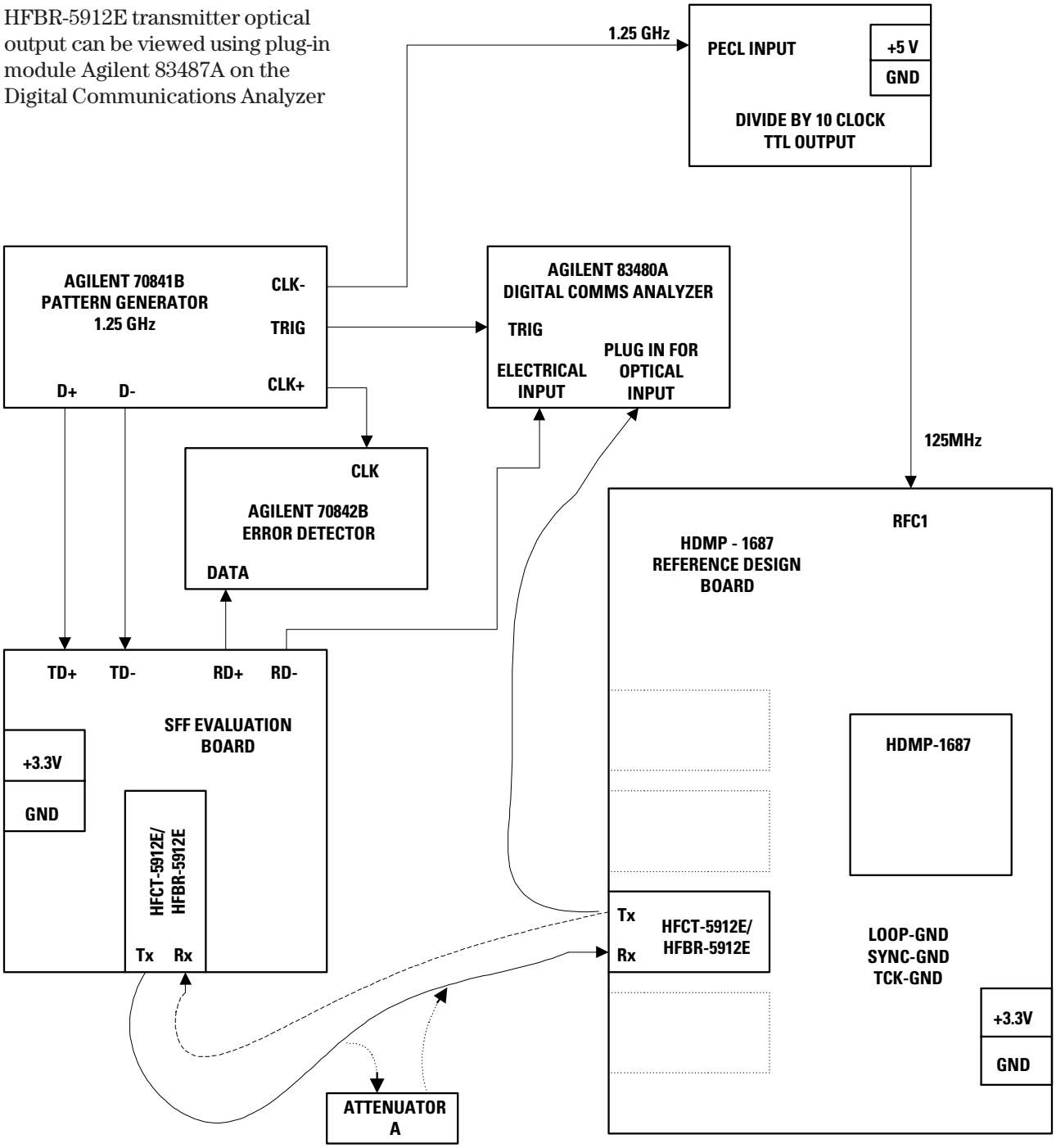


Figure 6. Test Configuration

Transmitter Jitter

The HFCT-5912E and HFBR-5912E total transmitter jitter was measured with the equipment setup shown in Figure 6. Total jitter is composed of both peak to peak deterministic jitter (DJ) and rms random jitter (RJ). Table 5 shows the results measured for transmitter jitter. Total jitter was calculated using the formula:- Total Jitter = Deterministic Jitter + (14 x Worst Case Random Jitter).

The 1000BASE-LX and 1000BASE-SX jitter budget at compliance point TP2* is 345 picoseconds. The Total Jitter results in Table 5 demonstrate the evaluation board has margin on this jitter budget.

*IEEE Draft P802.3z/D5.0 Table 38-10

Eye Mask Compliance

Figures 7 and 8 show the HFCT-5912E and HFBR-5912E compliance to the Gigabit Ethernet transmitter eye mask, when tested using the setup shown in Figure 6.

Table 5. Transmitter Jitter

HDMP-1687 with	DJ (pk-pk)	RJ (RMS)	Total Jitter
HFCT-5912E	110 ps	12.14 ps	280 ps
HFBR-5912E	112.2 ps	12.05 ps	281 ps

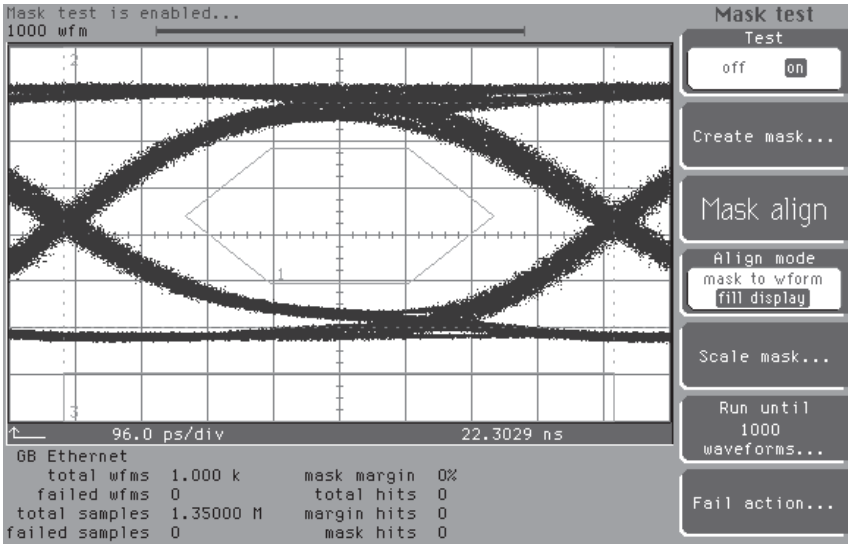


Figure 7. Typical HFCT-5912E Transmitter output eye

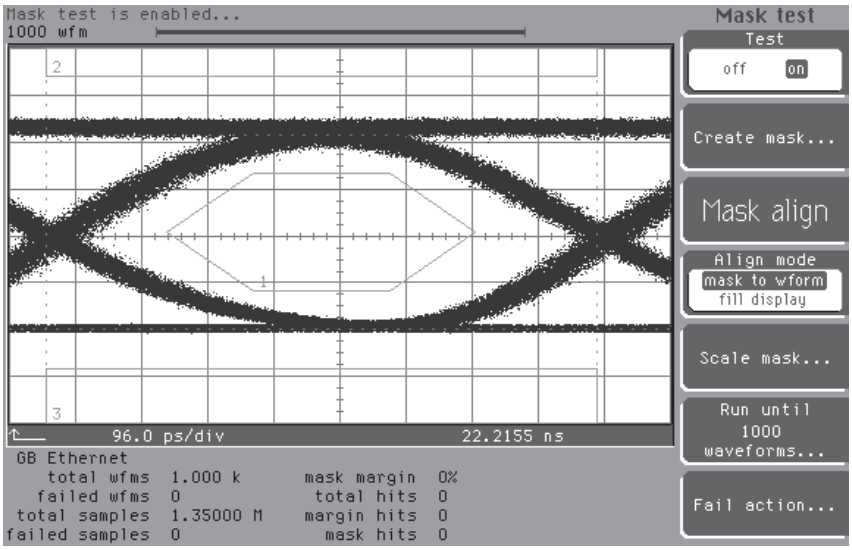


Figure 8. Typical HFBR-5912E Transmitter output eye

Power Supply Noise Immunity
The transceivers and the HDMP-1687 SerDes IC all share the same +3.3 V V_{CC} supply. Recommended power supply filtering has been included for each component as detailed in the appropriate Agilent Data Sheet and Application Note.

When using the recommended filter arrangements the HFCT-5912E will tolerate supply noise >110 mV pk to pk, over a frequency range of 10 Hz to 1 MHz, before a receiver sensitivity penalty of 1.0 dB occurs. The HFCT-5912E transmitter tolerated >300 mV pk to pk before the transmitter eye mask margin was reduced to 10%.

Unfiltered PSNI
In order to demonstrate the transceiver power supply noise immunity the Rx V_{CC} and Tx V_{CC} were isolated in turn from the common +3.3 V supply. For the Rx this was achieved by removing components L7 + C36 and connecting the output of a bias T to the Rx V_{CC} transceiver connection. Figure 9 shows the additional equipment required to perform this test. An optical attenuator in position ATTENUATOR A, of Figure 6 was used to set the Reference Design board receiver optical input to sensitivity + 1 dB. The Tx output from this device was connected directly to another receiver on the SFF evaluation board the output of which was connected to the Error Detector. The maximum supply noise tolerated before a receiver sensitivity penalty of 1.0 dB occurred was recorded.

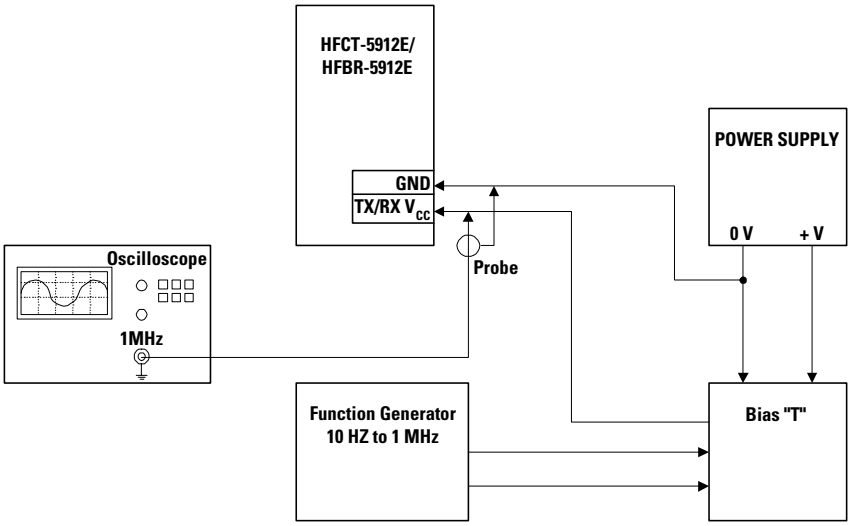
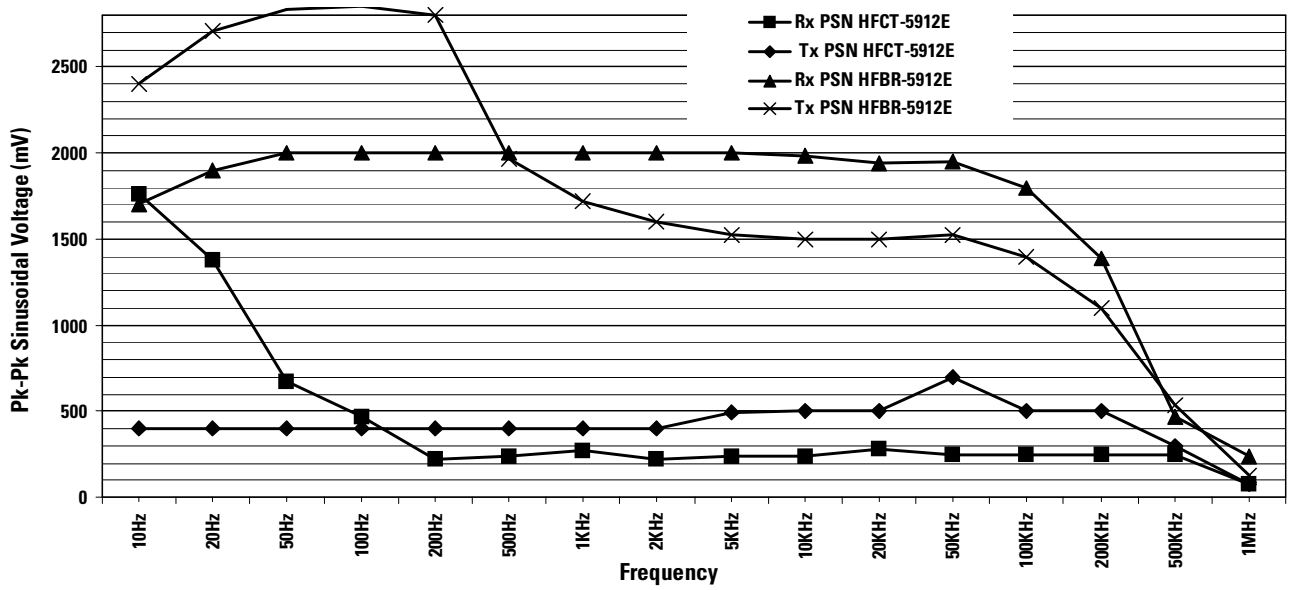


Figure 9. Power Supply Noise Immunity Test Setup

Table 6. Unfiltered Power Supply Noise Immunity Results where Receiver Sensitivity was reduced by 1 dB and Transmitter eye mask margin was reduced to 10%.

Frequency	HFCT-5912E		HFBR-5912E	
	Maximum Rx PSN (mV)	Maximum Tx PSN (mV)	Maximum Rx PSN (mV)	Maximum Tx PSN (mV)
10 Hz	1760	400	1700	2400
20 Hz	1380	400	1900	2710
50 Hz	670	400	2000	2830
100 Hz	470	400	2000	2850
200 Hz	219	400	2000	2800
500 Hz	238	400	2000	1970
1 KHz	269	400	2000	1720
2 KHz	219	400	2000	1600
5 KHz	238	490	2000	1520
10 KHz	239	500	1980	1500
20 KHz	281	500	1940	1500
50 KHz	243	700	1950	1520
100 KHz	246	500	1800	1400
200 KHz	245	500	1390	1100
500 KHz	250	300	470	536
1 MHz	76	80	240	130



Graph 1. Unfiltered Power Supply Noise (PSN) Immunity Results where Receiver Sensitivity was reduced by 1 dB and Transmitter eye mask margin was reduced to 10%.

For the Tx, components L6 + C35 were removed and the output of the bias T connected to the Tx V_{CC} transceiver connection. The maximum supply noise tolerated before the Tx eye opening was reduced to a 10% eye mask margin was recorded.

Results for both the HFCT-5912E and the HFBR-5912E are shown in Table 6 and Graph 1.

EMI Radiation

Measurements of EMI radiation were made with the HDMP-1687 Reference Design board rotated within a GTEM 5305 test chamber. The board was mounted in a metal box with four MT-RJ ports and SMA connections for V_{CC} and the reference clock. All four transceivers were linked in series using MT-RJ patchcords. A further transceiver outside the chamber was used to transmit and receive data. A worst case 1010 input signal was used for this test. The divide by ten board for the reference clock and the +5 V and +3.3 V supplies were kept outside the chamber. The EMI equipment block diagram is shown in Figure 10.

Port emission results demonstrated significant margin to the spec limit for FCC Class B of 54 dBµV/m. Figure 11 shows the HFCT-5912E has 12 dB margin and Figure 12 shows the HFBR-5912E has 10 dB margin against FCC Class B.

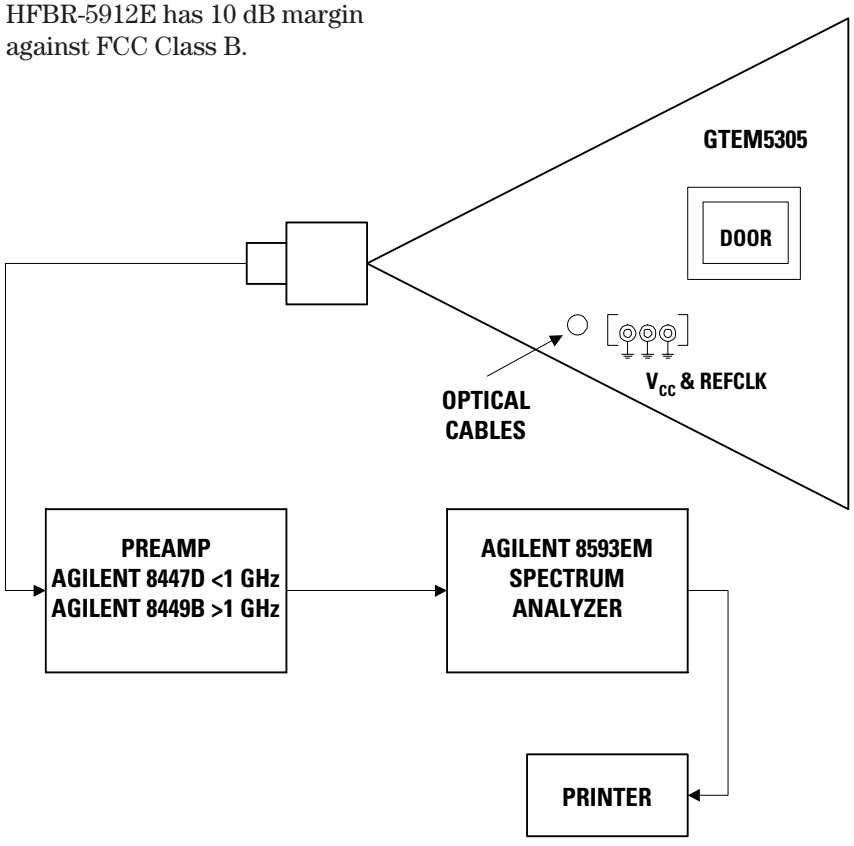


Figure 10. EMI Test Setup

Conclusions

The information presented in this application note will help the designer to quickly and successfully develop an Agilent provided solution for an IEEE 802.3z Gigabit Ethernet compliant reference design, at the first attempt. With common electrical and mechanical interfaces the multimode SFF (HFBR-5912E) and single mode SFF (HFCT-5912E) can be swapped without design changes to the circuit so providing additional design flexibility.

The reported test data and test methods help the designer to understand how best to check performance of their design. Also, the provided guidance assists the designer in printed circuit board layout and in circuit designing with the Agilent SerDes IC and SFF transceivers.

References

[1] HDMP-1680/1687: 1.25 GBd Quad SerDes Chip Data Sheet.

[2] IEEE 802.3z Gigabit Ethernet Specification .

[3] HFCT/HFBR-5912E Small Form Factor MT-RJ Fiber Optic Transceivers for Gigabit Ethernet, Technical Data Sheet

[4] 1.25 Gb Multimode and Single Mode Small Form Factor (SFF) Transceiver, Application Note 1184.

[5] Reference Design Guidelines for Gigabit Fiber-Optic Datacom Systems Implemented with MT-RJ Small Form Factor Modules, Application Note 1201.

Web Sites

www.semiconductor.agilent.com
Agilent Technologies component information.

This evaluation board is intended for evaluation purposes only. Agilent does not guarantee its performance in a production environment.

Information in this application note is subject to change without notice.

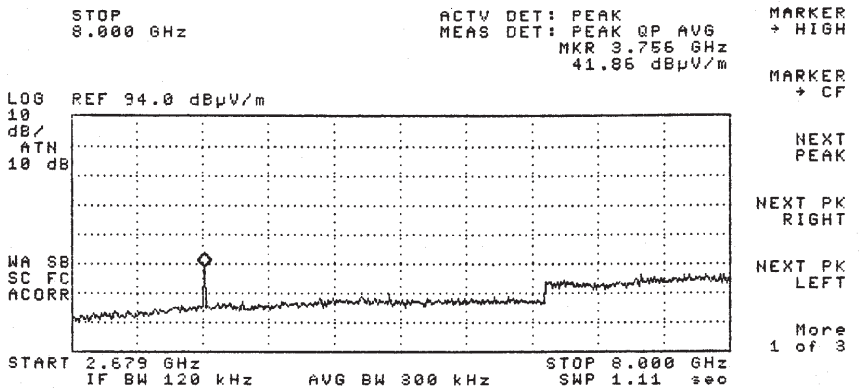


Figure 11. Worst Case Reference Board EMI with four HFCT-5912E's was 41.9d BµV/m @ 3.756 GHz

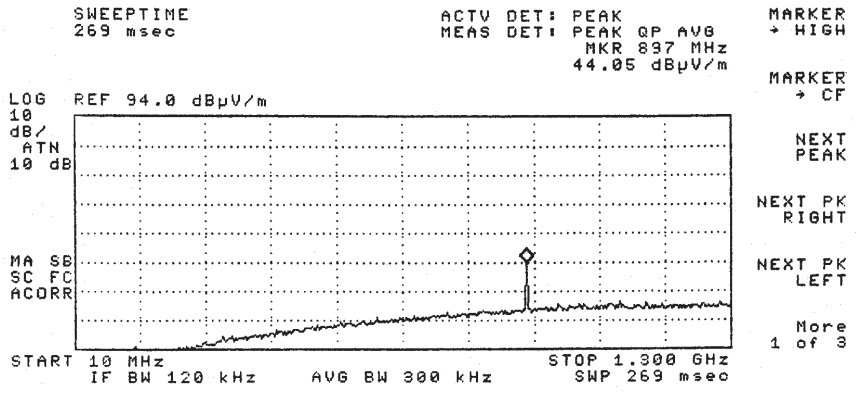


Figure 12. Worst Case Reference Board EMI with four HFBR-5912E's was 44.1d BµV/m @ 897 MHz

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