HEWLETT® PACKARD

155 Mb/s Fiber Optic "Light to Logic"™ Receivers for OC3/STM1

Application Note 1125

RCV1551, RGR1551

Introduction

This application note details the operation and usage of the RCV1551 and RGR1551 Light to Logic SONET/SDH modules. Both models are 155 Mb/s, multi-sourced, SONET/SDH modules, capable of operating in a temperature range of -40°C to +85°C.

The RGR1551 has data and clock recovery function, the RCV1551 does not. Both parts are suitable for long reach applications. They both also have the facility of using independent biasing (0 V or -5 V) of the PIN diode to allow average power in the fiber pigtail to be sensed.

The RCV1551 and RGR1551 convert optical signals into differential positive ECL (PECL) level outputs; they also provide complementary alarms to indicate loss of optical signal.

The receivers are comprised of an InGaAs PIN photodiode. A high sensitivity, wide dynamic range transimpedance amplifier is capacitively coupled, in the case of the RCV1551, to a limiting amplifier stage. In the case of the RGR1551 the transimpedance amplifier is capacitively coupled to a PLL based clock recovery circuit. The latter stages of both parts convert low level signals to complementary PECL levels for RCV1551 data outputs and both data and clock outputs for the RGR1551.

Electrical Characteristics

Tables 5 and 6 provide a description of the function and use of each device pin for the RCV1551 and RGR1551 respectively.

Power Supply

Both receivers require a positive +5 V supply to operate all the internal circuitry. As previously indicated, the receivers have an output pin 10 that can be taken to a negative potential to externally bias the PIN diode. The part also meets specification with pin 10 grounded.

Care should be taken to avoid transients and overvoltage. Overvoltage above the maximum specified in both the RCV1551 and RGR1551 data sheets may cause permanent damage. It should not be assumed that more than one maximum condition can be applied at a time.

In these receivers, the PIN supply provides bias and allows photocurrent measurement for monitoring purposes. It is recommended that a series inductor of at least 500 µH be inserted in the PIN bias line for optimum performance. If this facility is not required, the pin should be connected to the lowest voltage rail.

Noise Immunity

The receiver includes internal circuit components to filter power supply noise.

Under some conditions of EMI and power supply noise, external power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network shown in Figure 1, when positioned in close proximity to the device supply pins, may be used to improve performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Data and Clock Outputs

The RGR1551 provides complementary recovered Clock outputs in addition to the data outputs provided by the RCV1551. These PECL outputs are 10 KH ECL compatible and must be correctly terminated as any mismatch will

significantly degrade performance. Some typical termination techniques are shown in Figure 3.

The receiver's Data (and RGR1551 Clock) outputs are not affected by the status of the loss of light alarm. Under loss of light conditions, the RGR1551 Clock outputs will not remain at their operating speed. Their frequency will vary as the circuit hunts for a signal to lock to. The Data outputs will switch randomly until the input signal rises to a detectable level.

The RGR1551 $\overline{\text{CLOCK}}$ output falling edge occurs coincident with the edges of the Received Data output. The rising edge occurs in the middle of the Received Data baud period as shown in Figure 2.

Layout

Due to the relatively high frequencies and low noise levels involved, it is important that good RF techniques are used for the PCB layout. The use of ground planes and 50 ohm transmission line interconnects is required for PECL outputs.

Jitter Tolerance

SONET standards currently specify jitter tolerance as the jitter amplitude that increase by 1 dB the signal input level at which the network element will operate at a BER of 1 x 10^{-10}. Table 1 shows a typical jitter tolerance performance for the RGR1551. The envelope column represents the minimum amount of jitter the device must tolerate at a given frequency.

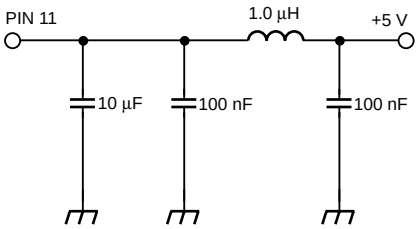


Figure 1.

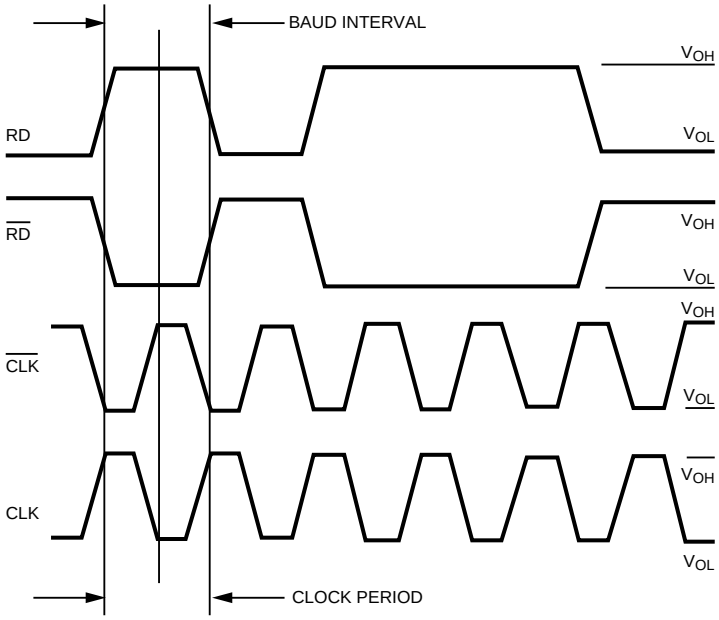
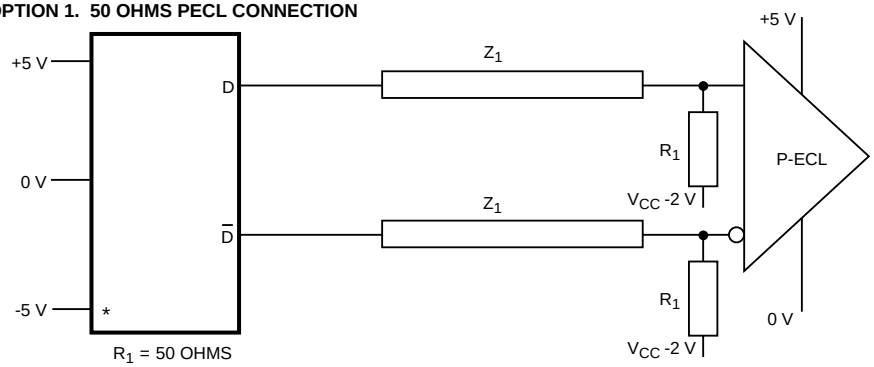


Figure 2. Relative timing relationship between output re-timed Data and Recovered Clock signals

Table 1. Typical Jitter Tolerance Results for RGR1551

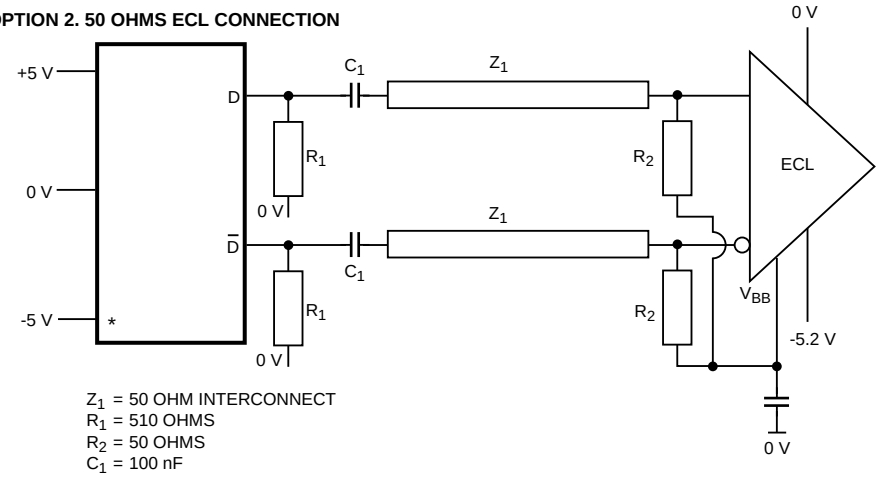
Frequency (kHz)	Envelope (UI)	Results (UI) @ -5 V		
		-40°C	+25°C	+85°C
1	1.5	24	24	24
2	1.5	18	19	17
7	1.5	4.8	4.8	4.4
50	0.15	0.75	0.77	0.71
500	0.15	0.39	0.41	0.39
1000	0.15	0.39	0.41	0.39

OPTION 1. 50 OHMS PECL CONNECTION



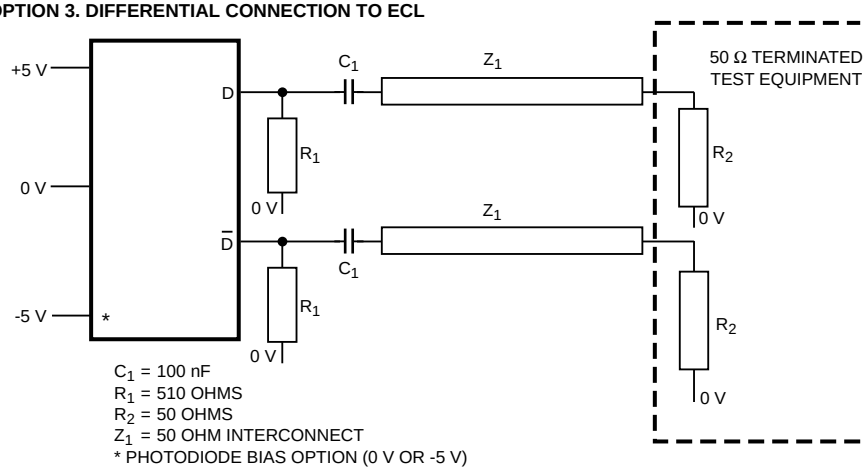
R_1 = 50 OHMS
Z_1 = 50 OHM INTERCONNECT
* PHOTODIODE BIAS OPTION (0 V OR -5 V)

OPTION 2. 50 OHMS ECL CONNECTION



Z_1 = 50 OHM INTERCONNECT
R_1 = 510 OHMS
R_2 = 50 OHMS
C_1 = 100 nF
* PHOTODIODE BIAS OPTION (0 V OR -5 V)

OPTION 3. DIFFERENTIAL CONNECTION TO ECL



C_1 = 100 nF
R_1 = 510 OHMS
R_2 = 50 OHMS
Z_1 = 50 OHM INTERCONNECT
* PHOTODIODE BIAS OPTION (0 V OR -5 V)

NOTE:
1. OPTIONS 1 TO 3 SHOW TERMINATION CONFIGURATIONS FOR DATA AND $\overline{\text{DATA}}$ OUTPUTS. CLOCK AND $\overline{\text{CLOCK}}$ OUTPUTS SHOULD BE TERMINATED IN THE SAME WAY.
2. 50 Ω TO -2V MAY BE REPLACED BY THE THEVENIN EQUIVALENT 82 Ω TO V_{CC} AND 130 Ω TO V_{ee}.

Figure 3. RCV1551 and RGR1551 Termination Options

Alarm Output
The RCV1551 and RGR1551 contain circuitry to detect loss of input optical signal. The circuit monitors signal amplitude at the output of the preamplifier and therefore detects loss of modulation as well as loss of optical signal.

The RGR1551 provides complementary CMOS alarm outputs and requires no output termination. The RCV1551 provides complementary PECL alarm outputs which require standard PECL terminations.

The ALARM outputs (pins 12 and 14) are complementary with a HIGH level indicating normal operation and a LOW level indicating loss of light or modulation.

PIN Photocurrent Monitoring
The current drawn from pin 10 will be proportional to the optical signal level at the device. Additional circuitry may be added to use this as a means of actively monitoring the optical power. The current drawn from pin 10 will be approximately 1 nA for no signal rising to 250 µA at maximum input power. Responsivity of the pin diode is between 0.7 A/W and 1.0 A/W.

Care should be taken to avoid injecting noise onto this pin.

A low impedance current measuring source should be used to minimize voltage drop.

Power Dissipation/Heatsinking
The RCV1551 and RGRI551 are 20 pin DIP packaged components. The maximum operating temperatures are the maximum ambient temperatures. The typical power consumption is shown in Table 2.

Table 2. Typical Power Consumption

	-5 V	+5 V	Total Power Dissipation
-40°C	1 mA	110* mA	555 mW
+25°C	1 mA	120* mA	605 mW
+85°C	1 mA	130* mA	655 mW

* Current with DATA, $\overline{\text{DATA}}$, ALARM, $\overline{\text{ALARM}}$ terminated as shown in Figure 3 is not included.

Table 3. Fiber Pigtail Typical Parameters

Core Diameter	50 µm
Cladding Diameter	125 µm
Concentricity	<3 µm
Nominal Coating Diameter	500 µm
Outer Cladding Diameter	900 µm

Wavelength Range
The RCV1551 and RGR1551 contain a planar InGaAs PIN photodiode and will detect an optical signal in the range 1200 nm to 1600 nm. Over this range the performance is substantially unchanged. However, due to the normal change in the PIN diode responsivity with wavelength, the sensitivity is likely to increase slightly (<1 dB) at 1550 nm compared with 1300 nm.

Fiber
The fiber pigtail is graded index 50/125 µm multimode “floppy” fiber. Typical parameters are shown in Table 3.

Evaluation Board
An evaluation board for the RCV1551 (101207.000) and RGR1551 (105178.003) is available which allows easy usage and evaluation of the RCV1551 and RGR1551.

Regulatory Compliance

The receiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing Certification of Information Technology Equipment (See Table 4). Additional information is available from your Hewlett-Packard sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the receiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the receiver parts. To the extent that the fiber connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These receivers have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these receivers within a well-designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Table 4. Regulatory Compliance - Typical Performance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	> 500 V
Immunity	Variation of IEC 801-3	Typically, the RCV1551 shows less than 0.5 dB degradation in performance at 3 V/m when swept from 27 MHz to 1 GHz (worst case degradation being 0.8 dB), when mounted on a card with no chassis enclosure. The RGR1551 typically shows less than 0.8 dB degradation in performance under the same conditions, worst case degradation being 1.3 dB.

Table 5. RCV1551 Pin Out Table

Pin	Symbol	Description
1	GND	This pin should be connected to the circuit ground.
2	GND	This pin should be connected to the circuit ground.
3	GND	This pin should be connected to the circuit ground.
4	GND	This pin should be connected to the circuit ground.
5	NC	This pin is not connected and should be left open circuit on the application board.
6	GND	This pin should be connected to the circuit ground.
7	DATA	This pin should be terminated using standard PECL techniques, as shown in Figure 3. The DATA output is non-inverting, an optical pulse causes the DATA output to go to the PECL logic high state.
8	GND	This pin should be connected to the circuit ground.
9	$\overline{\text{DATA}}$	This pin should be terminated using standard PECL techniques, as shown in Figure 3. The $\overline{\text{DATA}}$ output is inverting, an optical pulse causes the $\overline{\text{DATA}}$ output to go to the PECL logic low state.
10	PD Bias	This pin must be connected to any voltage from 0 V (GND) to -5 V in order to provide photodiode bias. The current drawn is directly proportional to the average received photocurrent. I = Responsivity x Mean Power, where the responsivity will be between 0.7 and 1.0 A/W.
11	+5 V	This pin should be connected to +5 V supply. The filter network shown in Figure 1 should be placed as close as possible to this pin.
12	ALARM	This pin provides a low light ALARM output. The ALARM output goes to a logic low state when there is insufficient optical power. The optical power must increase to a higher level than the level where the alarm went low before the ALARM will return to logic high. This difference is the alarm hysteresis. This pin should be terminated using standard PECL techniques.
13	GND	This pin should be connected to the circuit ground.
14	$\overline{\text{ALARM}}$	This pin provides a low light ALARM output. The $\overline{\text{ALARM}}$ output goes to a logic low state when there is insufficient optical power. The optical power must increase to a higher level than the level where the alarm went high before the $\overline{\text{ALARM}}$ will return to logic low. This difference is the alarm hysteresis. This pin should be terminated using standard PECL techniques.
15	GND	This pin should be connected to the circuit ground.
16	GND	This pin should be connected to the circuit ground.
17	NC	This pin is not connected and should be left open circuit on the application board.
18	NC	This pin is not connected and should be left open circuit on the application board.
19	NC	This pin is not connected and should be left open circuit on the application board.
20	NC	This pin is not connected and should be left open circuit on the application board.

Table 6. RGR1551 Pin Out Table

Pin	Symbol	Description
1	GND	This pin should be connected to the circuit ground.
2	GND	This pin should be connected to the circuit ground.
3	GND	This pin should be connected to the circuit ground.
4	CLOCK	This pin should be terminated using standard PECL techniques, as shown in Figure 3.
5	$\overline{\text{CLOCK}}$	This pin should be terminated using standard PECL techniques, as shown in Figure 3.
6	GND	This pin should be connected to the circuit ground.
7	DATA	This pin should be terminated using standard PECL techniques, as shown in Figure 3. The DATA output is non-inverting, an optical pulse causes the DATA output to go to the PECL logic high state.
8	GND	This pin should be connected to the circuit ground.
9	$\overline{\text{DATA}}$	This pin should be terminated using standard PECL techniques, as shown in Figure 3. The $\overline{\text{DATA}}$ output is inverting, an optical pulse causes the $\overline{\text{DATA}}$ output to go to the PECL logic low state.
10	PD Bias	This pin must be connected to any voltage from 0 V (GND) to -5 V in order to provide photodiode bias. The current drawn is directly proportional to the average received photocurrent. I = Responsivity x Mean Power, where the responsivity will be between 0.7 and 1.0 A/W.
11	+5 V	This pin should be connected to +5 V supply. The filter network shown in Figure 1 should be placed as close as possible to this pin.
12	ALARM	This pin provides a low light ALARM output. The ALARM output goes to a logic low state when there is insufficient optical power. The optical power must increase to a higher level than the level where the alarm went low before the ALARM will return to logic high. This difference is the alarm hysteresis. No termination is required.
13	GND	This pin should be connected to the circuit ground.
14	$\overline{\text{ALARM}}$	This pin provides a low light ALARM output. The $\overline{\text{ALARM}}$ output goes to a logic low state when there is insufficient optical power. The optical power must increase to a higher level than the level where the alarm went high before the $\overline{\text{ALARM}}$ will return to logic low. This difference is the alarm hysteresis. No termination is required.
15	GND	This pin should be connected to the circuit ground.
16	GND	This pin should be connected to the circuit ground.
17	NC	This pin is not connected and should be left open circuit on the application board.
18	NC	This pin is not connected and should be left open circuit on the application board.
19	NC	This pin is not connected and should be left open circuit on the application board.
20	NC	This pin is not connected and should be left open circuit on the application board.

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