900 and 2400 MHz Amplifiers Using the AT-3 Series Low Noise Silicon Bipolar Transistors

Application Note 1085

1. Introduction

Discrete transistors offer low cost solutions for commercial applications in the VHF through microwave frequency range. Today's silicon bipolar transistors offer state-of-the-art noise figure and gain performance with low power consumption.

This application note discusses the design techniques and performance of the Hewlett-Packard AT-3 series of silicon bipolar transistors as used in typical low noise amplifiers for use in the various commercial markets.

Although specific designs are presented for 900 and 2400 MHz, the techniques are applicable to other applications in the VHF through S Band frequency range. This would include the 450 MHz (Mobile Radio), 900 MHz (Cellular and Pager), 1.2 and 1.5 GHz (GPS), 1.9 GHz (PCN), 2.1 to 2.7 GHz (MMDS and ITFS) and the 2.4 GHz (ISM) markets.

Generally, silicon bipolar devices are easier to work with at the lower frequencies because of their inherently lower impedances. However, today's state-of-the-art low current bipolar transistors have considerably higher impedances making them comparable to GaAs FETs at these frequencies. Similar design techniques must be used with these devices to assure good performance. Appropriate design techniques will be presented.

This application note will begin with an overview of noise parameters and definitions and then lead into general design considerations for building low noise amplifiers. Two amplifier designs will be presented along with measured results. The application note will finish with a discussion of matching network losses and their effect on amplifier noise figure. Touchstone™ circuit files and simulated results for both amplifiers are included in the Appendix.

2. Noise Parameter Measurements

A typical test set-up for measuring noise parameters is shown in Figure 1. The device under test (DUT) is normally inserted into a test fixture that includes 50 ohm input and output transmission lines whose effect can be calibrated out for the particular frequency. As a minimum, a double stub tuner or

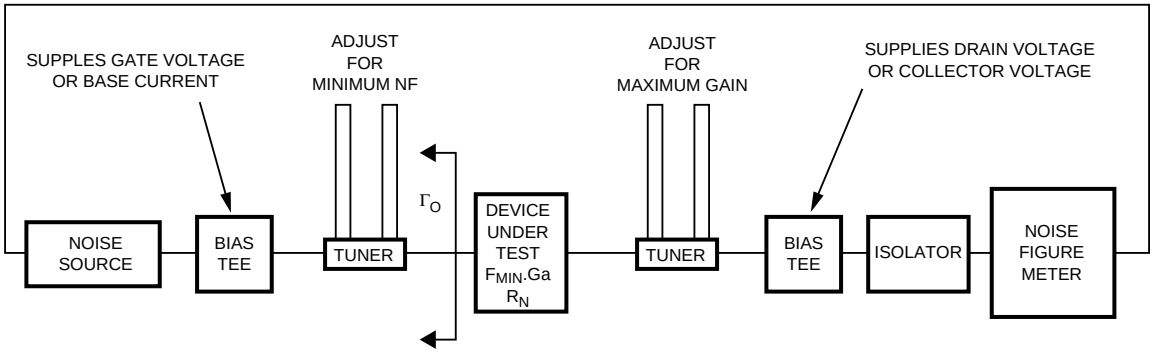


Figure 1. Typical Noise Parameter Measuring Test Set-up.

equivalent must be used at the input to the DUT to present the required Gamma Opt., Γ_O, to the device for it to achieve its minimum noise figure. Although not always required, a tuner can be inserted at the output of the DUT. Providing a conjugate match at the output of the DUT while the input is presented with Γ_O provides a means of measuring associated gain at minimum noise figure. One particular manufacturer of automatic noise measuring equipment uses a tuner on the input and terminates the output in 50 Ω and then measures the resultant S_{22}. A calculation then provides the associated DUT gain. Bias Tees are used at the input and output of the DUT to bias the device. A noise source with a low Excess Noise Ratio, ENR, such as the Hewlett-Packard HP346A, is desired as it minimizes test error by minimizing the range over which the noise figure meter must remain linear. The HP346A noise source also has minimal change in reflection coefficient between the "on" and "off" states. This minimizes the ability of the DUT to change its gain with varying input termination. Any change in DUT gain will increase the measurement error. An isolator placed at the input of the noise figure meter is always desirable but may not be possible at the lower frequencies where size becomes more of an issue.

The noise figure of a linear two port is given by equation (1) shown in the table below.

In equation (1),

NF_{min} is the device minimum noise figure when terminated in Y_{on},

Y_{on} is the generator admittance at which minimum noise figure occurs,

Y_g is the generator admittance presented to the input of the device,

R_n is the noise resistance which gives an indication of the sensitivity of noise figure to termination, and

G_g is the real part of the generator impedance.

The equation can be transformed into an equivalent equation involving the source reflection coefficient, Γ_S, and the reflection coefficient required for minimum noise figure, Γ_O. See equation (2) below.

Once Γ_O has been determined and NF_{min} determined, the R_n can be determined by making a 50 Ω noise figure measurement and calculating R_n. This procedure only works well if Γ_O can be determined by a single measurement. A more accurate method would be to pick 4 reflection coefficients (4 terminating impedances) in the vicinity of where one believes Γ_O to be and then solve 4 equations and 4 unknowns. This method has become a more accurate industry standard.

The input tuner must be capable of transforming the customary 50 ohm source impedance to that required for the device to achieve its rated noise figure. As an example, for the Hewlett-Packard AT-30511 operated at a V_{CE} of 1 volt and I_C of 1 mA, Γ_O has a magnitude of 0.76 increasing to 0.96 at 500 MHz. These numbers represent impedances that can be increasingly difficult to match with low loss. Losses of the tuner become more questionable as the Γ_O increases, plus the ability to design and build a low loss matching network becomes more of a challenge. An early paper by Strid[1] discusses tuner losses as well as losses in matching networks. The problem with tuner losses is that the tuner has a different loss for every tuner setting and this effect is more pronounced at higher reflection coefficients. The user must rely on calibration data supplied by the manufacturer and this data may not be guaranteed much above a reflection coefficient of 0.6 to 0.7.

If the tuner's calibration were accurately known and relatively constant with tuner setting then it would be a simple matter to adjust the tuner and DUT for lowest noise figure and then subtract out the tuner loss to obtain the DUT minimum noise figure, NF_{min}. With varying loss in the tuner, it is difficult to determine if adjusting the tuner and DUT for minimum noise figure minimizes the DUT noise figure or the tuner loss. The alternative of presenting 4 known impedances to the device and solving 4 equations and 4 unknowns is preferred.

Equations

$$NF = NF_{min} + \frac{R_n}{G_g} \left| Y_g - Y_{on} \right|^2 \qquad (1)$$

$$NF = NF_{min} + \frac{4 R_n}{Z_o} \frac{|\Gamma_s - \Gamma_o|^2}{(|1 + \Gamma_o|^2)(1 - |\Gamma_s|^2)} \qquad (2)$$

3. General Design Considerations

Implementing the input match can take on any of a variety of circuit topologies depending on the frequency and the space allowed for implementing the network. Alternatives may include:

- Lumped element network,
- Microstripline network, or
- Cavity filter match

A lumped element network can be either high pass, low pass, or bandpass and generally 2 or 3 elements. Below 2 GHz these networks will generally be lower loss than a microstripline circuit because of substrate losses. Above 2 GHz, the lumped element topology will be very difficult to synthesize with realizable components. The cavity filter approach is probably the lowest loss matching network but cost and size generally make it prohibitive for most commercial applications.

Losses of actual input matching circuits have been measured at nearly 0.5 dB at VHF frequencies when attempting to match the high impedances of MESFETs. Similar impedances can be encountered when using low current silicon bipolar transistors. Matching a device for lowest noise performance does not necessarily guarantee the best input VSWR and performance tradeoffs need to be made. A solution is the use of inductance in the emitter leads to create negative feedback which can bring Γ_O and S_{11}* closer in value[2,3,4]. The amount of inductance must be carefully weighed against its effect on other circuit parameters such as gain and stability. An improperly chosen amount of inductance can cause out-of-band oscillations that can prohibit an amplifier from delivering its rated performance. Other techniques such as resistive feedback and resistive loading can improve stability but can limit power output capability.

An often overlooked part of an amplifier is the bias decoupling network that must be invisible to the RF matching networks. Generally they provide a low loss method of biasing the devices but in some situations can actually be used to provide some resistive loading for stability both in-band and out-of-band. Properly designed bias decoupling networks can also be used to provide some form of band pass or high pass filtering that could help reduce low frequency out-of-band gain. A poorly designed amplifier with very high low-frequency gain that may be unconditionally stable according to the computer simulation may actually oscillate if the output can radiate back to the input. The enclosure that houses the amplifier must be designed to offer enough isolation around the circuit such that it does not make the amplifier circuit unstable at any frequency.

The manner in which circuit elements are implemented will affect the overall amplifier performance. The use of etched circuit elements as opposed to surface mount discrete elements offers a cost benefit but may affect losses. Surface mount components offer small size but parasitics and device Q must be understood if their effect on circuit performance is to be properly analyzed.

4. 900 MHz Silicon Bipolar Amplifier

The 900 MHz amplifier uses an AT-32033 which is in the industry standard SOT-23 package. The AT-32033 is one of a series of silicon bipolar transistors that are fabricated using an optimized version of Hewlett-Packard's 10 GHz f_t Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device-to-device uniformity is guaranteed in fabrication by the use of ion-implantation, self aligned techniques, and gold metalization.

The AT-3 series of devices has a 3.2 micron emitter-to-emitter pitch and has been fabricated in a variety of geometries for various applications. The 20 emitter finger interdigitated geometry yields an easy to match device capable of moderate power at low to moderate current. The 10 emitter finger geometry offers higher gain at low current while the 5 emitter finger geometry offers the highest gain at lowest current consumption. The smaller devices at very low current present very high impedances that can make them more of a challenge to design with. The impedances associated with very low current transistors at 900 MHz are very similar to those presented by 500 micron MESFETs at 900 MHz.

The 900 MHz AT-32033 amplifier is designed for a nominal 1 dB noise figure and 10 dB associated gain at 2 mA collector current. Although the device is capable of sub 1 dB noise figures, most applications do not require much below 1.5 dB. Starting out with a device that has such a low NF_{min} allows the designer to make tradeoffs between noise figure, gain, stability, etc.

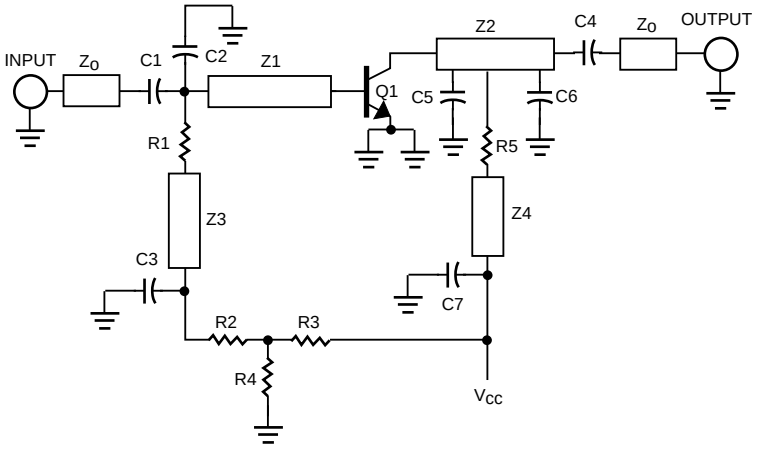
The schematic diagram of the 900 MHz amplifier is shown in Figure 2. The input noise match consisting of a low pass network in the form of C2 and Z1 provides a low Q broad band match. A small wound inductor could replace

transmission line Z1. A value in the range of 15 to 20 nH would be a good substitute. In the actual circuit it was found that the input shunt capacitor was not required. Adding a shunt capacitor at this point will allow the designer to make tradeoffs between noise figure and input VSWR.

The output match consists of a 3 element low pass network. The 3 element network allowed a shorter length of series transmission line to be used as compared to a 2 element match. The series inductive element can be etched onto the printed circuit board or a low cost wound inductor can be used if board space is limited. A suggested value would be in the range of 20 to 25 nH. The artwork and component placement guide are shown in Figures 3 and 4. A small amount of emitter inductance is used to improve in-band stability. This value must be carefully chosen such that an excessive amount is not used, otherwise high frequency oscillations could be produced. Out-of-band oscillations will severely limit the ability of the device to produce its rated performance. Resistor R1 provides very low frequency stability while resistor R5 enhances overall stability, including in-band performance. A current source consisting of resistor R2 connected to the resistive divider consisting of resistors R3 and R4 provide the necessary base current to produce the desired 2 mA collector current.

Actual measured noise figure of the amplifier with a micro-stripline input is shown in Figure 5. The amplifier provides a nominal 1.25 dB noise figure from 800 to 1000 MHz. The noise figure will improve slightly with the use of a wound inductor in place of the microstripline. Pay careful attention to the parasitic capacitance of the wound inductor as it could limit amplifier noise figure and affect out-of-band stability. Actual measurements of the microstripline input match circuit indicates a 0.26 dB loss. Subtracting this loss from the measured amplifier noise figure suggests a 1 dB device noise figure which is as predicted by the computer simulation. One of the advantages of using a device with a 0.78 dB NF_{min} is that compromises can be made between noise figure, gain, and input match.

Actual measured amplifier gain is shown in Figure 6. The amplifier has a nominal 11 dB gain from 750 to 900 MHz.



C1–10 pF CHIP CAPACITOR
C2 – 1 pF CHIP CAPACITOR (ADJ FOR NF/VSWR)
C3, C7–1,000 pF CHIP CAPACITOR
C4–100 pF CHIP CAPACITOR
C5–1 pF CHIP CAPACITOR
C6–2.7 pF CHIP CAPACITOR
Q1 – HEWLETT-PACKARD AT-32033 SILICON BIPOLAR TRANSISTOR
R1 – 50 OHM CHIP RESISTOR
R2 – 47 K OHM CHIP RESISTOR (ADJ FOR RATED Ic)
R3, R4 – 15 K OHM CHIP RESISTOR
R5, – 150 – 180 OHM CHIP RESISTOR (ADJ FOR STABILITY/POUT)
Z_O – 50 OHM MICROSTRIPLINE
Z1–Z2 – ETCHED MICROSTRIPLINE CIRCIITRY (MAY SUBSTITUTE INDUCTOR)
Z3–Z4 – MICROSTRIP BIAS DECOUPLING LINES

Figure 2. Schematic Diagram of AT-30233 900 MHz Amplifier.

The etched microstriplines can be replaced by a pair of lumped inductors as shown in Figure 7 with a 0.1 dB improvement in noise figure.

Once the circuit has been optimized for best noise figure, gain and input/output VSWR, it is then necessary to take a look at output power. The 900 MHz amplifier was first tested for P_{1dB} and then for IP_3. Initial results for P_{1dB} were less than those as specified on the data sheet. The major difference is that the amplifier being evaluated was conjugately matched at the output. Most device manufacturers specify P_{1dB} at a "power match" and not a "conjugate match". This implies that tuners are used at the input and output of the device to maximize

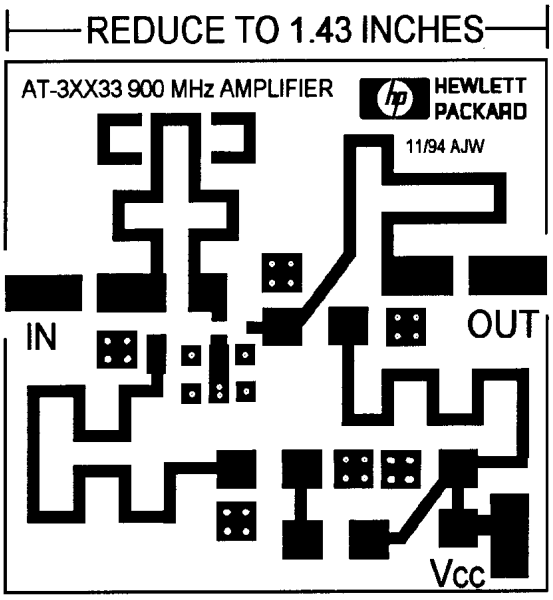


Figure 3. 2X artwork for 900 MHz Amplifier using 0.062 inch thick FR-4.

gain and power output. Maximum power output rarely occurs when any device's output port is conjugately matched. How much improvement can be achieved by power matching?

Initially, the 900 MHz amplifier was tuned for best output VSWR at 850 MHz. Greater than 20 dB return loss was obtained. The measured 1 dB compression point referenced to the output was -5.5 dBm with the device biased at a V_{CE} of 2.7 volts and 2 mA I_C. Close examination of the output matching network suggested that possibly the 180 Ω resistor used in the output bias decoupling line might be

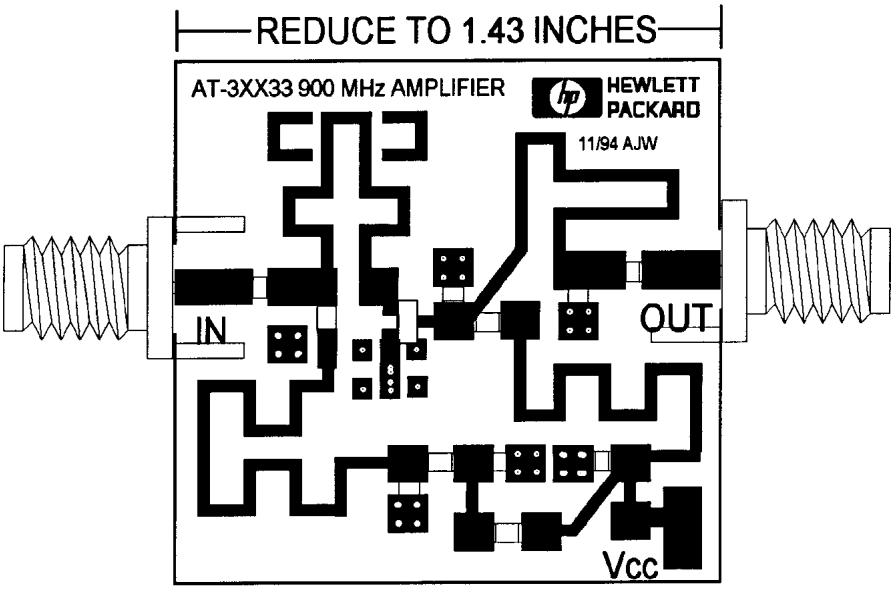


Figure 4. Component Placement for 900 MHz Amplifier using 0.062 inch thick FR-4.

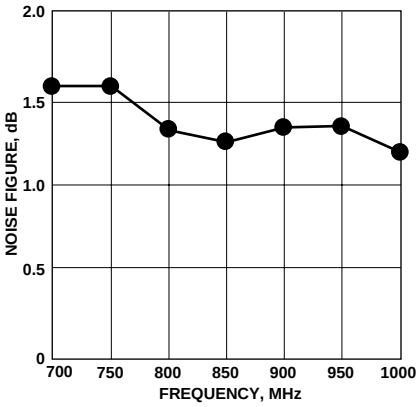


Figure 5. AT-32033 Amplifier Noise Figure.

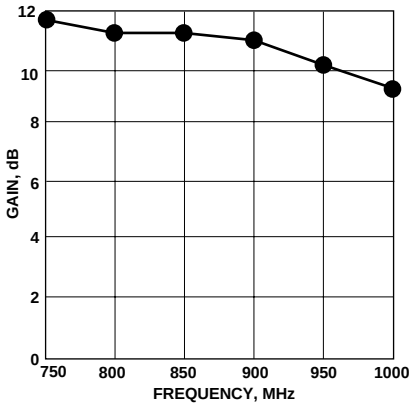


Figure 6. AT-32033 Amplifier Gain.

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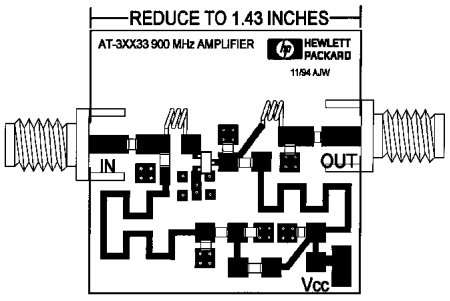


Figure 7. 900 MHz Amplifier showing the Placement of Wound Inductors in place of Microstripline Networks.

absorbing some of the power. This resistor was placed in the circuit to raise in-band stability. Placing a short across this resistor and re-measuring the 1 dB compression point showed an improvement of 3.5 dB! Also observed was an increase in collector current when the device is driven toward compression. An increase in current causes an increase in the voltage drop across the 180 Ω resistor causing the collector voltage to sag. Minimizing the value of this resistor will tend to keep V_{CE} high when the device is driven hard and will also minimize power absorption in the circuit. The drawback could be decreased stability. Some compromise with respect to output loads may have to be instituted if additional power output is desired.

A P_{1dB} of -2 dBm is still slightly lower than the data sheet specification. However, the output is still conjugately matched and not power matched. In order to provide a power match, one must provide an alternative output match. In order to prove that a power match will provide greater power output, a lab exercise can be set-up. A double stub tuner is connected in series with the existing conjugately matched amplifier output circuitry and the power meter. The tuner is then adjusted for greatest power output while driving the input circuit higher. A spectrum analyzer can be useful here to determine that harmonics are not high enough in level to distort the power meter measurement. In small steps increase the input power and then retune the output tuner for maximum fundamental power. After retuning the output for a power match, it was found that the P_{1dB} increased to nearly 2 dBm with a reduction in gain of 1 dB over the small signal conjugate match. In order to revise the output match to provide a power match would require breaking the circuit at the collector port of the device and measuring the new Gamma Load (Γ_L) presented by the existing circuit plus the external tuner. It is interesting to note that the output return loss which was greater than 20 dB at 850 MHz is now only 8.5 dB at the power match condition.

In addition to measuring P_{1dB} at all output matches, the two tone third order intercept point (IP_3) was also measured. For each test, two tones were introduced at the input to the amplifier which are separated by 10 MHz. The resultant third order products were then measured and averaged and IP_3 was calculated. The results are shown in Table 1.

The results show a consistent 20 to 21 dB of difference between P_{1dB} and IP_3. This is somewhat greater than has been measured on other larger geometry small signal devices but it does appear to be repeatable.

5. 2400 MHz Silicon Bipolar Amplifier

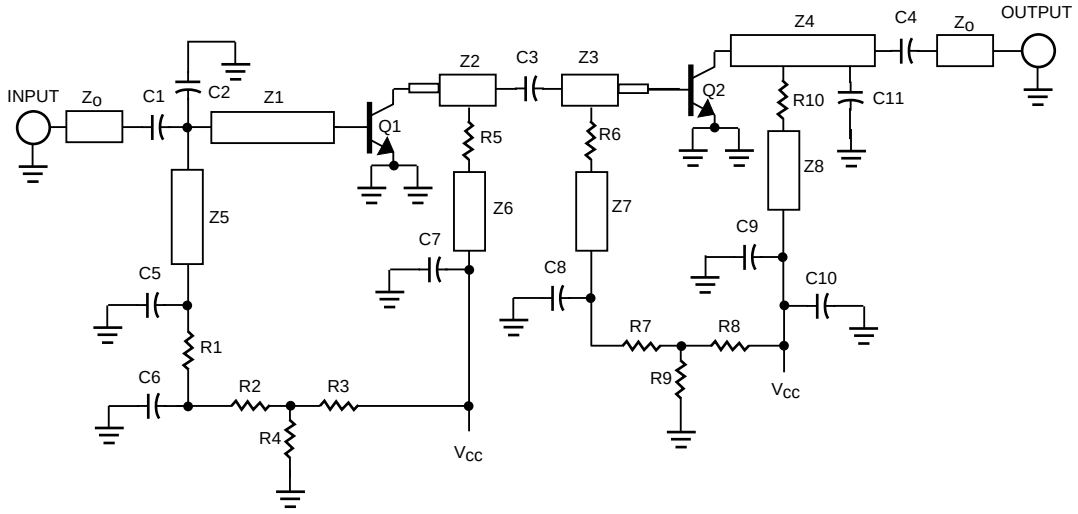
The 2400 MHz amplifier is designed around the Hewlett-Packard AT-31011. The 10 emitter finger geometry plus the SOT-143 package with the two emitter leads offers improved performance at frequencies above 2 GHz. At a rated current of 1 mA, the AT-31011 provides a device noise figure of 1.7 dB at 2400 MHz with an associated gain of 10 dB.

The schematic diagram of the 2400 MHz amplifier is shown in Figure 8. The input noise match consisting of a low pass network in the form of C2 and Z1 provides a low Q broad band match. The capacitor at C2 can be optimized for either a noise or conjugate match.

The output match consists of a 2 element low pass network while the interstage network consists of two short transmission lines and a series capacitor. The artwork and component placement guide are shown in Figures 9 and 10. Minimal emitter inductance is used to preserve in-band gain without sacrificing stability. Resistor R1 provides low frequency stability while resistors R5 and R10 enhance overall stability, including in-band performance. Two current sources (resistor R2 connected to the resistive divider consisting of resistors R3 and R4 and R7 connected to the resistive divider consisting of R8 and R9) provide the necessary base current to produce the desired 1 mA collector current in each device.

Table 1. 900 MHz Amplifier Power Output Summary.

Condition	P_{1dB}	IP_3
Conjugate Match	-5.5 dBm	+16 dBm
Conjugate Match w/o resistor	-2.0 dBm	+18 dBm
Power Match	+2 dBm	+23 dBm



C1, C4, C5, C9 –10 pF CHIP CAPACITOR
C2 – 1.3 pF CHIP CAPACITOR
C3–1.5 pF CHIP CAPACITOR
C6, C7, C8, C10,–1,000 pF CHIP CAPACITOR
C11– 2 pF CHIP CAPACITOR (ADJUST FOR MIN OUTPUT VSWR)
Q1, Q2 – HEWLETT-PACKARD AT-31011 SILICON BIPOLAR TRANSISTOR
R1, R10 – 50 OHM CHIP RESISTOR
R5, R7 – 47 K OHM CHIP RESISTOR (ADJUST FOR RATED Ic)
R3, R4, R8, R9, 15 K OHM CHIP RESISTOR
R5, 16 OHM CHIP RESISTOR
R6, 1 K OHM CHIP RESISTOR
Z_O – 50 OHM MICROSTRIPLINE
Z1–Z4 – ETCHED MICROSTRIPLINE CIRCIITRY
Z5–Z8 – MICROSTRIP BIAS DECOUPLING LINES

Figure 8. Schematic Diagram of AT-31011 2400 MHz Amplifier.

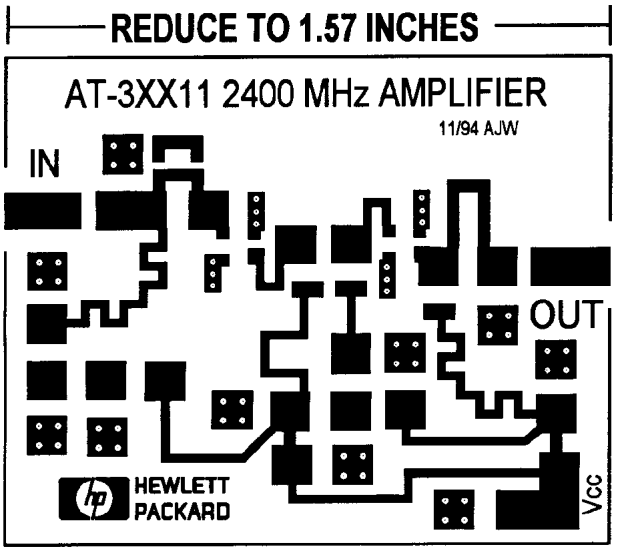


Figure 9. 2X artwork for 2400 MHz Amplifier using 0.062 inch thick FR-4.

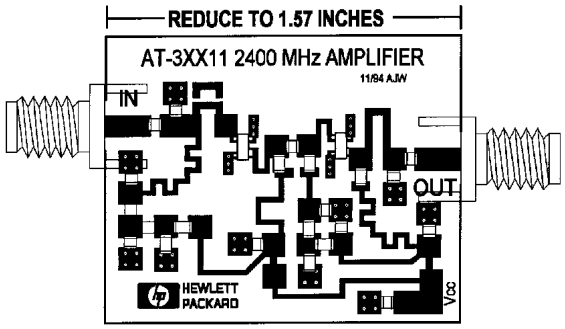


Figure 10. Component placement for 2400 MHz Amplifier (Drawing not to scale).

The amplifier has a measured noise figure between 1.9 and 1.95 dB from 2400 to 2500 MHz with a nominal associated gain of 20 dB at a total current consumption of 2 mA for both devices. Measured output 1 dB gain compression point is -4.5 dBm with an associated IP_3 of +7 dBm. See Figures 11 and 12.

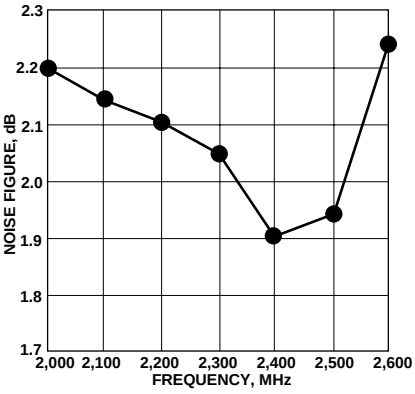


Figure 11. AT-31011 Amplifier Noise Figure.

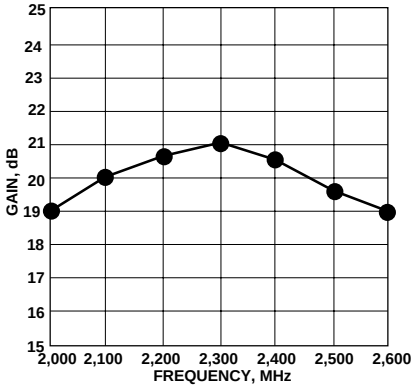


Figure 12. AT-31011 Amplifier Gain.

6. Other Applications

The low current bipolar transistors can also be used in frequency converter applications. Although not optimum, the 900 MHz amplifier circuit shown in Figure 4 can be used to demonstrate mixer operation. The amplifier circuit can be modified for use as a downconverter to a 10.7 MHz IF by simply coupling out the IF by attaching a 0.1 to 0.3 µH coil to the output circuit. The point to couple to should be at the junction of C4 and C6 (reference Figure 2). Ultimately, the IF should also have a dc blocking capacitor but it was not required for this simple test. The LO is injected into the output port of the amplifier and the amplifier input port is the RF input port. With a nominal +3 dBm LO, the circuit without any optimization provides a nominal 6 dB conversion gain and less than 12 dB noise figure. Optimization of the bias and matching structures will improve performance. Generally, higher LO increases conversion gain but there is generally a nominal LO power that produces the lowest noise figure. Bias voltage and current can be critical, especially for lowest noise operation.

7. Matching Circuit Losses

The losses associated with the input matching structure can be calculated with the help of equation (3) shown in the table below. The available gain of a two port is shown.

The power delivered to the load is simply the power that would be delivered if the load were conjugately matched to the network. With the input to the network being 50 ohms, $\Gamma_S = 0$, equation (3) reduces to equation (4).

The measurement of S_{21} is nothing more than a 50 ohm available gain measurement. It is imperative that the source and load presented to the device be as near a perfect 50 ohm impedance as possible as this is the reference impedance for the reflection coefficient. Both the numerator and the denominator use only the magnitude of S_{21} and Γ_L or S_{11} so it is only necessary to measure accurately the magnitude and not phase. With a network with a very high reflection coefficient, S_{22} becomes very large and S_{21} very lossy. With a low reflection coefficient, S_{22} is smaller and loss becomes very low.

Several circuits are analyzed for loss and the results are shown in Table 2. The first circuit is a simple series inductor and blocking capacitor providing a noise match for a 900 MHz amplifier. Loss calculated to be 0.23 dB. The second circuit is a simple L network consisting of a variable series capacitor and a shunt inductor which transforms a 50 ohm source impedance to an S_{22} of 0.94 at 500 MHz. This is a typical reflection coefficient required to match both silicon and GaAs devices for lowest

Equations

$$G_a = \frac{|S_{21}|^2 \ (1 - |\Gamma_S|^2)}{|1 - S_{11}\ \Gamma_S|^2 \ (1 - |\Gamma_L|^2)} \qquad (3)$$

$$G_a = |S_{21}|^2 / (1 - |\Gamma_L|^2) \qquad (4)$$

Table 2. Losses of Various Matching Networks.

Circuit Number	Freq. (MHz)	Circuit	S21 (dB)	S21	S22 (dB)	S22	Loss (dB)
1	900	L	-5.8	0.513	-1.4	0.85	0.23
2	500	L/C	-9.8	0.324	-0.54	0.94	0.45
3	150	Cap coupled tank	-5.8	0.513	-1.4	0.85	0.23
4	900	AT-32033 Microstrip	-0.5	0.944	-12.7	0.23	0.26
5	2400	AT-31011 Microstrip	-2.2	0.776	-4.75	0.58	0.44
6	2400	ATF-10236 Microstrip	-1.1	0.881	-7.0	0.45	0.14

noise figure at 500 MHz. Compared to circuit number 1, the measured loss has increased 0.2 dB because of the losses associated with matching to a higher impedance. The third circuit is a parallel tuned circuit with a series input capacitor used to provide the high impedance transformation to a reflection coefficient of 0.85 at 150 MHz. Notice that the measured loss is the same as circuit number 1 with a similar reflection coefficient but at a different frequency. Circuits 4, 5, and 6 are micro-stripline designs for 900 and 2400 MHz.. Circuit 4 is the input network for the 900 MHz amplifier using the AT-32033 previously described. Subtracting the 0.26 dB for the input loss reduces the noise figure to 1 dB which is the noise figure as predicted without circuit losses. The loss of the input match for the 2400 MHz AT-31011 amplifier was measured at 0.44 dB. This is as a result of using lossy FR-4/G-G10 at 2 GHz and a higher reflection coefficient. Contrast this result with circuit number 6 which is a noise match for the ATF-10236 FET etched on ER = 2.2 material[6].

8. Calculating Circuit Losses

The calculation of circuit losses is only as accurate as the models of the individual circuit elements. The inductor in matching circuit #1 will be analyzed.

The inductor used is an air wound solenoid with 5 turns #26 guage enamel wire with a 0.075" I.D. The inductance is calculated as [7,8] :

$$L\ (\mu H) = \frac{n^2 \bullet r^2}{9\,r + 10\,l}$$

where n = number of turns
r = radius
l = length

Solving yields L ~ 20 nH

The unloaded Q can be calculated as follows:

$$Qu = 2\,r\,A\,f^{1/2}$$

where r = radius
A = 100 - 130 for 1/r from 2 to 20
f = frequency in MHz

Solving yields Qu = 259.

Actual measurements of Q suggest that a Qu of 100 to 200 might be a better value for maximum Qu. The equivalent series R_S can now be calculated. Based on a Qu of 200 :

$$Qu = \frac{j\,\omega\,l}{Rs}$$

$$\text{Therefore } Rs = \frac{j\,\omega\,l}{Qu}$$

Solving yields R_S = 0.565 Ω. This is the equivalent series resistance of the 5 turn coil.

The loaded Q of the circuit, Ql, can now be calculated or measured with the device terminating the matching network and a 50 Ω source termination. The loaded Q can be found by dividing the 3 dB bandwidth into the nominal center frequency, f_O. Another alternative is to plot Z_{in} of the network terminated with the device. Any point on the Smith Chart represents an impedance consisting of both real and reactive components. Dividing the reactive part into the real part provides the Q of the network. The Ql is approximately 1 for this network. Network insertion loss can now be calculated with the following equation:

Insertion Loss I.L. =
-20 log [(Qu - Ql) / Qu]

Solving yields an insertion loss of 0.043 dB. If the Qu of the inductor is only 100 then the loss would calculate at 0.087 dB, which is probably more consistent with the measured results. Other factors such as radiation loss, microstripline loss and capacitor Q can make up the difference in the calculated versus measured loss.

Some packaged and molded inductors have a Qu of only 25 and with a higher Ql the loss can approach 0.5 dB!

9. Conclusions

At low bias currents, the AT-3 series of devices can have a Γ_O as high as 0.94 at sub 1 dB noise figures. This allows the designer more flexibility in making tradeoffs and still achieving 1 to 1.5 dB noise figures at 900 MHz with silicon. In addition to concern over tuner losses and their effect ultimately on the accuracy of the noise parameter measurement, the losses associated with actual noise matching structures can approach 0.5 dB unless attention is paid to component Q.

References

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Appendix I.

AT-32033 900 MHz Low Noise Amplifier Touchstone Circuit File

```
!SINGLE STAGE DESIGN
!A.J.WARD 11-28-94
!REVISED 06-15-95
DIM
        FREQ    GHZ
        IND     NH
        CAP     PF
        LNG     IN
VAR
        W1=.03                  !INPUT LINE WIDTH
        L1\1.11529 !INPUT LINE LENGTH
        C1=0.7          !INPUT SHUNT CAPACITOR,
        !               TRADEOFF NOISE FIGURE AND INPUT VSWR
        W3=.03          !OUTPUT LINE WIDTH
        L3=1                    !OUTPUT LINE LENGTH
        LL1=.05         !EMITTER LEAD LENGTH, UP TO .1
                        STILL OK ON STABILITY
CKT
        MSUB    ER=4.8 H=.062 T=.0014 RHO=1 RGH=0
        TAND    TAND=.002
        MLIN    1       2       W=.1 L=.05
        SLC     2       3       L=.25C=10
        MLIN    3       4       W=.1 L=.2
        SLC     4       5       L=.25 C^C1
        VIA     5       0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   4       6       W1=.1 W2^W1
        MLIN    6       7       W^W1 L^L1
        !IND    6       7       L#0 14.82035 30  !OPTIONAL INDUCTOR
        RES     4       10      R=50
        MLIN    10      11      W=.1 L=.1
        MSTEP   11      12      W1=.1 W2=.03
        MLIN    12      13      W=.03 L=1.5
        SLC     13      14      L=.4C=1000
        VIA     14      0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   7       16      W1^W1 W2=.1
        MLIN    16      17      W=.1            L=.1
        MSTEP   17      18      W1=.1 W2=.02
        MLIN    18      19      W=.02 L=.01
        DEF2P   1       19      INPUT

        S2PA    1       2       3 C:\S_DATA\BJT\T320333A.S2P
        DEF3P   1       2       3  DEVICE

        MLIN    1       2       W=.02 L^LL1
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P 1                 EMITTER

        MLIN    1       2       W=.02L=.030
        MSTEP   2       3       W1=.02 W2=.1
        MLIN    3       4       W=.1 L=.1
        CAP     3       5       C=1
        VIA     5       0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   4       6       W1=.1           W2^W3
        MLIN    6       7       W^W3 L^L3!OUTPUT SERIES
                                MICROSTRIPLINE
```

Appendix I. (continued)

```
        CAP     7       8 C=3.3
        VIA     8       0 D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   7       9 W1=.03 W2=.1
        MLIN    9       10W=.1 L=.2
        SLC     10      11 L=.25 C=100    !OUTPUT BLOCKING CAPACITOR
        MLIN    11      12 W=.1 L=.2
        !IND    6       7 L=19            !OPTIONAL INDUCTOR
        RES     4       15R=180           !OUTPUT BIAS RESISTOR
        MLIN    15      16 W=.1 L=.1
        MSTEP   16      17 W1=.1 W2=.03
        MLIN 17 18W=.03 L=1.1             !OUTPUT BIAS DECOUPLING LINE
        SLC     18      19 L=.4 C=1000
        VIA     19      0 D1=.03 D2=.03 H=.062 T=.0014
        DEF2P   1       12 OUTPUT

        INPUT   1       2
        DEVICE  2       3       4
        EMITTER 4
        OUTPUT  3       5
        DEF2P   1       5       AMP

FREQ
        !SWEEP  .8      .95     .05
        SWEEP   1       6       .05
        !STEP   .9
OUT
        AMP     DB[S11]
        AMP     DB[S21]
        AMP     DB[S12]
        AMP     DB[S22]
        AMP     NF
        AMP     K
        AMP     B1
```

Appendix II.
AT-32033 900 MHz Low Noise Amplifier Touchstone Output File

FREQ	**DB[S11]**	**DB[S21]**	**DB[S12]**	**DB[S22]**	**NF**	**K**	**B1**
GHz	**AMP**	**AMP**	**AMP**	**AMP**	**AMP**	**AMP**	**AMP**
0.10000	-1.498	3.372	-48.108	-4.199	130.814	15.358	1.061
0.20000	-4.645	8.046	-38.108	-4.383	116.859	6.328	0.874
0.30000	-5.827	10.157	-32.273	-4.526	9.236	2.837	0.850
0.40000	-5.057	11.257	-28.176	-4.861	4.600	1.600	0.891
0.50000	-5.110	11.791	-25.061	-5.606	3.035	1.301	0.885
0.60000	-6.812	11.983	-23.273	-6.637	2.162	1.350	0.830
0.70000	-10.037	11.955	-21.702	-8.525	1.483	1.396	0.810
0.80000	-11.427	11.658	-20.392	-12.403	1.076	1.375	0.879
0.85000	-9.606	11.353	-19.889	-15.993	0.998	1.342	0.945
0.90000	-7.482	10.904	-19.526	-20.742	0.988	1.303	1.018
0.95000	-5.781	10.462	-19.357	-19.366	1.038	1.247	1.081
1.00000	-4.585	9.866	-19.343	-14.305	1.141	1.199	1.120
1.10000	-3.556	8.190	-19.893	-7.571	1.602	1.136	1.059
1.20000	-4.059	5.508	-21.451	-4.013	2.792	1.228	0.814
1.30000	-5.057	2.124	-23.713	-2.238	5.002	1.539	0.549
1.40000	-5.778	-1.342	-26.059	-1.382	7.892	2.089	0.367

Appendix II. (continued)

FREQ GHz	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1 AMP
1.50000	-6.267	-4.557	-28.154	-0.931	10.447	2.849	0.254
1.60000	-6.700	-7.319	-29.959	-0.663	10.898	3.700	0.182
1.70000	-7.272	-9.781	-31.482	-0.485	9.234	4.597	0.132
1.80000	-8.057	-11.963	-32.742	-0.359	7.568	5.409	0.096
1.90000	-9.156	-13.736	-33.692	-0.267	7.705	5.855	0.070
2.00000	-10.786	-15.080	-34.236	-0.200	8.002	5.759	0.050
2.10000	-13.299	-15.845	-34.236	-0.152	7.700	5.023	0.037
2.20000	-17.541	-16.048	-33.689	-0.119	6.549	3.940	0.028
2.30000	-20.689	-15.868	-32.776	-0.099	5.263	2.960	0.023
2.40000	-14.810	-15.587	-31.776	-0.088	4.265	2.305	0.020
2.50000	-10.236	-15.354	-30.873	-0.082	3.532	1.907	0.019
2.60000	-7.580	-15.320	-30.189	-0.078	3.052	1.695	0.017
2.70000	-6.082	-15.405	-29.640	-0.073	2.768	1.574	0.016
2.80000	-5.301	-15.439	-29.055	-0.071	2.674	1.488	0.015
2.90000	-4.989	-15.228	-28.241	-0.074	2.759	1.417	0.015
3.00000	-5.043	-14.562	-26.985	-0.087	2.998	1.356	0.017
3.10000	-5.584	-13.034	-24.930	-0.129	3.383	1.297	0.026
3.20000	-7.307	-10.196	-21.582	-0.287	4.065	1.281	0.062
3.30000	-15.000	-5.276	-16.166	-1.248	5.426	1.335	0.274
3.40000	-2.598	-5.918	-16.327	-1.502	8.299	1.488	0.355
3.50000	-2.766	-12.438	-22.380	-0.413	14.667	1.770	0.117
3.60000	-3.838	-17.043	-26.530	-0.195	110.890	2.230	0.058
3.70000	-5.109	-20.831	-29.874	-0.114	114.890	3.038	0.034
3.80000	-6.263	-24.588	-33.198	-0.073	118.632	4.665	0.022
3.90000	-7.069	-28.352	-36.539	-0.053	122.715	8.177	0.015
4.00000	-7.852	-31.840	-39.612	-0.044	127.408	15.485	0.012
4.10000	-8.982	-34.760	-42.171	-0.041	131.902	28.677	0.011
4.20000	-10.107	-37.081	-44.142	-0.041	135.443	48.112	0.010
4.30000	-8.786	-39.067	-45.788	-0.041	139.553	71.206	0.011
4.40000	-5.200	-41.421	-47.811	-0.042	148.837	96.903	0.012
4.50000	-2.572	-44.864	-50.932	-0.043	164.320	135.388	0.015
4.60000	-1.317	-49.706	-55.460	-0.044	182.941	238.949	0.017
4.70000	-0.831	-56.880	-62.327	-0.045	206.724	820.446	0.019
4.80000	-0.676	-83.878	-89.025	-0.046	230.000	999.900	0.020
4.90000	-0.655	-59.586	-64.440	-0.048	216.606	1.2e+03	0.020
5.00000	-0.688	-53.587	-58.153	-0.049	198.890	317.261	0.021
5.10000	-0.746	-49.788	-54.070	-0.050	187.575	142.025	0.021
5.20000	-0.820	-46.540	-50.543	-0.052	177.777	73.514	0.022
5.30000	-0.924	-43.271	-47.000	-0.053	167.832	38.986	0.022
5.40000	-1.100	-39.630	-43.087	-0.056	156.799	20.311	0.023
5.50000	-1.501	-35.333	-38.519	-0.061	144.303	10.651	0.024
5.60000	-2.652	-30.545	-33.463	-0.077	132.566	6.353	0.027
5.70000	-3.785	-27.790	-30.441	-0.103	128.475	4.930	0.035
5.80000	-2.526	-28.273	-30.658	-0.106	130.063	4.583	0.038
5.90000	-1.797	-28.389	-30.506	-0.114	130.625	4.174	0.042
6.00000	-1.406	-26.574	-28.423	-0.153	128.556	3.283	0.058

Appendix III.
AT-31011 2400 MHz Low Noise Amplifier Touchstone Circuit File

```
!AT-31011 2400 MHz LOW NOISE AMPLIFIER !
!A.J.WARD 9-12-94
!REVISED 06-15-95

DIM
        FREQ    GHZ
        IND     NH
        CAP     PF
        LNG     IN

VAR
        W1=.03                  !INPUT LINE WIDTH
        L1=.15                  !INPUT LINE LENGTH
        C1=1.3                  !INPUT SHUNT CAPACITOR
        C2=1.5                  !INTERSTAGE BLOCKING CAPACITOR
        W2=.02                  !INTERSTAGE LINE WIDTH
        L2=.178                 !INTERSTAGE LINE LENGTH
        W3=.03                  !OUTPUT LINE WIDTH
        L3=.4                   !OUTPUT LINE LENGTH
        LL1=.02
        LL2=.02

CKT
        MSUB ER=4.8 H=.062 T=.0014 RHO=1 RGH=0
        TAND TAND=.002
        MLIN    1       2       W=.1 L=.05
        SLC     2       3       L=.25C=10
        MLIN    3       4       W=.1 L=.05
        MCROS   4 5 6 7         W1=.1 W2=.02W3^W1 W4=.1
        MLIN    6       8       W^W1 L^L1
        MLIN    7       14      W=.1 L=.03
        SLC     14      15      L=.25C^C1
        VIA     15      0       D1=.03 D2=.03 H=.062 T=.0014
        MLIN    5       16      W=.02 L=.68
        MSTEP   16      17      W1=.02 W2=.1
        MLIN    17      18      W=.1 L=.1
        SLC     18      19      L=.25 C=10
        VIA     19      0       D1=.03 D2=.03 H=.062 T=.0014
        RES     18      20      R=50
        SLC     20      21      L=.4 C=1000
        VIA     21      0       D1=.03 D2=.03 H=.062 T=.0014
        MSTEP   8       9       W1^W1 W2=.1
        MLIN    9       10      W=.1            L=.1
        MSTEP   10      11      W1=.1 W2=.02
        DEF2P   1       11      INPUT

        S2PA    1 2 3           C:\S_DATA\BJT\T310113A.S2P
        DEF3P   1 2 3 DEV1

        MLIN    1       2       W=.02 L^LL1
        MLIN    1       3       W=.02 L^LL1
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P   1               Q1EM
```

Appendix III. (continued)

```
        MLIN    1       2       W=.03 L=.03
        MSTEP   2       3       W1=.03 W2^W2
        MLIN    3       4       W^W2        L^L2
        MSTEP   4       5       W1^W2         W2=.1
        MLIN    5       6       W=.1        L=.1
        RES     6       7       R=20                            !Q1 OUTPUT BIAS RESISTOR
        MLIN    7       8       W=.08 L=.04
        MSTEP   8       9       W1=.08 W2=.02
        MLIN    9       10      W=.02 L=.45             !Q1 BIAS DECOUPLING LINE
        MSTEP   10      11      W1=.02 W2=.1
        MLIN    11      12      W=.1 L=.1
        SLC     12      13      L=.4 C=1000
        VIA     13      0       D1=.03 D2=.03 H=.062 T=.0014
        SLC     6       20      L=.25 C^C2              !INTERSTAGE BLOCKING CAP
        MLIN    20      21      W=.1        L=.1
        MSTEP   21      22      W1=.1         W2^W2
        MLIN    22      23      W^W2        L^L2
        MSTEP   23      24      W1^W2W2=.03
        MLIN    24      25      W=.03 L=.03
        RES     20      30      R=1000 L=1              !Q2 INPUT BIAS RESISTOR
        MLIN    30      31      W=.08 L=.04
        MSTEP   31      32      W1=.08 W2=.02
        MLIN    32      33      W=.02 L=.1  !Q2 BIAS DECOUPLING LINE
        SLC     33      35      L=.4C=1000
        VIA     35      0       D1=.03 D2=.03 H=.062 T=.0014
        DEF2P   1       25      INTER

        S2PA    1 2 3
        DEF3P   1 2 3           DEV2

        MLIN    1       2       W=.02 L^LL2
        MLIN    1       3       W=.02 L^LL2
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     2       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        VIA     3       0       D1=.030 D2=.030 H=.062 T=.001
        DEF1P   1               Q2EM

        MLIN    1       2       W=.03L=.01
        MSTEP   2       3       W1=.03 W2^W3
        MLIN    3       4       W^W3L^L3                !OUTPUT SERIES MICROSTRIPLINE
CAP     4       0       C=2
        SRL     3       5       R=50 L=1    !OUTPUT BIAS RESISTOR
        MLIN    5       6       W=.08 L=.04
        MSTEP   6       7       W1=.08 W2=.02
        MLIN    7       8       W=.02  L=.68  !OUTPUT BIAS DECOUPLING LINE
        SLC     8       9       L=.4C=1000
        VIA     9       0       D1=.03 D2=.03 H=.062 T=.0014
        SLC     4       10      L=.25C=10   !OUTPUT BLOCKING CAPACITOR
        MLIN    10      11      W=.1 L=.1
        DEF2P   1       11      OUTPUT

        INPUT   1       2
        DEV1    2 3 4
        Q1EM    4
        INTER   3 5
        DEV2    5 6 7
        Q2EM    7
```

Appendix III. (continued)

```
        OUTPUT 6  8
        DEF2P  1   8   AMP

FREQ
        !SWEEP   .8  .95 .05
        SWEEP    .1  6  .1
        !STEP     2.4
        !SWEEP 2.3 2.5  .05

OUT
        AMP       DB[S11]
        AMP       DB[S21]
        AMP       DB[S12]
        AMP       DB[S22]
        AMP       NF
        AMP       K
        AMP       B1
```

Appendix IV
AT-31011 2400 MHz Low Noise Amplifier Touchstone Output File

FREQ	DB[S11]	DB[S21]	DB[S12]	DB[S22]	NF	K	B1
GHZ	AMP	AMP	AMP	AMP	AMP	AMP	AMP
0.10000	-1.062	-25.182	-127.386	-1.469	187.514	1.3e+06	0.512
0.20000	-2.238	-17.107	-107.059	-5.097	167.325	2.2e+05	1.103
0.30000	-3.106	-14.030	-96.733	-9.769	157.806	7.9e+04	1.332
0.40000	-4.179	-11.418	-88.924	-11.791	147.718	3.0e+04	1.291
0.50000	-6.116	-5.838	-79.275	-9.303	125.694	6.0e+03	1.098
0.60000	-9.158	1.884	-68.806	-6.720	9.221	767.412	0.883
0.70000	-5.916	8.755	-59.488	-4.902	6.045	86.657	0.849
0.80000	-1.510	13.302	-52.728	-3.672	3.465	8.081	0.969
0.90000	-0.759	15.839	-48.162	-2.926	3.126	2.195	0.874
1.00000	-3.086	16.219	-47.144	-2.533	3.617	4.467	0.630
1.10000	-6.211	15.194	-46.967	-2.233	4.244	6.010	0.494
1.20000	-6.775	13.557	-47.433	-1.901	4.767	6.667	0.439
1.30000	-6.028	12.114	-47.732	-1.606	5.052	6.605	0.400
1.40000	-5.436	11.090	-47.632	-1.372	5.045	6.050	0.361
1.50000	-5.146	10.504	-47.111	-1.189	4.777	5.198	0.326
1.60000	-5.020	10.311	-46.304	-1.062	4.350	4.298	0.298
1.70000	-5.087	10.495	-45.119	-0.970	3.884	3.392	0.275
1.80000	-5.332	11.064	-43.545	-0.909	3.469	2.560	0.256
1.90000	-5.833	12.146	-42.197	-0.880	3.131	1.993	0.242
2.00000	-6.630	13.619	-40.444	-0.908	2.882	1.547	0.236
2.10000	-7.811	15.390	-38.208	-1.045	2.689	1.228	0.250
2.20000	-9.439	17.534	-35.567	-1.562	2.498	1.096	0.329
2.30000	-10.168	19.528	-33.040	-3.547	2.290	1.218	0.602
2.40000	-8.117	19.730	-32.267	-10.820	2.112	1.677	1.043
2.50000	-6.692	17.784	-33.774	-13.923	2.025	2.396	1.159
2.60000	-6.057	14.779	-36.308	-7.421	2.002	3.569	1.039
2.70000	-5.351	11.596	-38.988	-4.821	2.072	5.294	0.889
2.80000	-4.538	8.423	-41.626	-3.415	2.260	7.682	0.753
2.90000	-3.765	5.290	-44.192	-2.529	2.595	10.856	0.637
3.00000	-3.103	2.218	-46.669	-1.934	3.095	14.941	0.540
3.10000	-2.538	-0.665	-49.149	-1.506	3.745	19.792	0.458
3.20000	-2.079	-3.453	-51.487	-1.209	4.545	25.637	0.394
3.30000	-1.706	-6.114	-53.649	-0.999	5.455	32.402	0.345
3.40000	-1.401	-8.621	-55.612	-0.849	6.469	39.855	0.306
3.50000	-1.151	-10.953	-57.357	-0.740	7.804	47.556	0.277

Appendix IV. (continued)

FREQ GHZ	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1 AMP
3.60000	-0.944	-13.090	-58.869	-0.662	8.831	54.827	0.255
3.70000	-0.772	-15.018	-60.137	-0.606	10.646	60.822	0.239
3.80000	-0.628	-16.729	-61.158	-0.567	23.033	64.789	0.228
3.90000	-0.510	-18.237	-61.950	-0.542	108.229	66.692	0.221
4.00000	-0.424	-19.592	-62.567	-0.529	115.275	68.719	0.218
4.10000	-0.415	-20.849	-62.734	-0.525	121.982	78.852	0.217
4.20000	-0.885	-21.223	-62.032	-0.532	123.681	154.792	0.209
4.30000	-0.164	-22.151	-61.899	-0.545	129.046	35.679	0.232
4.40000	-0.112	-23.504	-62.207	-0.566	135.252	30.737	0.241
4.50000	-0.096	-24.905	-62.579	-0.589	141.063	33.882	0.251
4.60000	-0.092	-26.441	-63.104	-0.613	146.946	42.347	0.260
4.70000	-0.092	-28.146	-63.815	-0.630	153.040	56.771	0.267
4.80000	-0.092	-30.047	-64.740	-0.635	159.418	78.833	0.269
4.90000	-0.091	-32.170	-65.904	-0.622	166.132	111.562	0.264
5.00000	-0.089	-34.519	-67.313	-0.590	173.204	159.859	0.252
5.10000	-0.086	-37.057	-68.927	-0.544	180.576	230.188	0.233
5.20000	-0.082	-39.651	-70.616	-0.490	187.968	325.612	0.212
5.30000	-0.077	-42.024	-72.099	-0.435	194.686	428.636	0.189
5.40000	-0.073	-43.798	-73.002	-0.384	199.757	486.771	0.168
5.50000	-0.068	-44.848	-73.196	-0.339	202.939	467.729	0.149
5.60000	-0.064	-45.563	-73.071	-0.300	205.529	420.440	0.132
5.70000	-0.062	-46.692	-73.375	-0.265	209.831	424.844	0.117
5.80000	-0.063	-49.524	-75.397	-0.232	219.639	657.731	0.103
5.90000	-0.068	-58.864	-83.940	-0.198	230.000	4.8e+03	0.088
6.00000	-0.078	-50.536	-74.829	-0.166	224.833	618.737	0.074