Dimming HDSP-213X Displays

To Meet Night Vision Lighting Levels

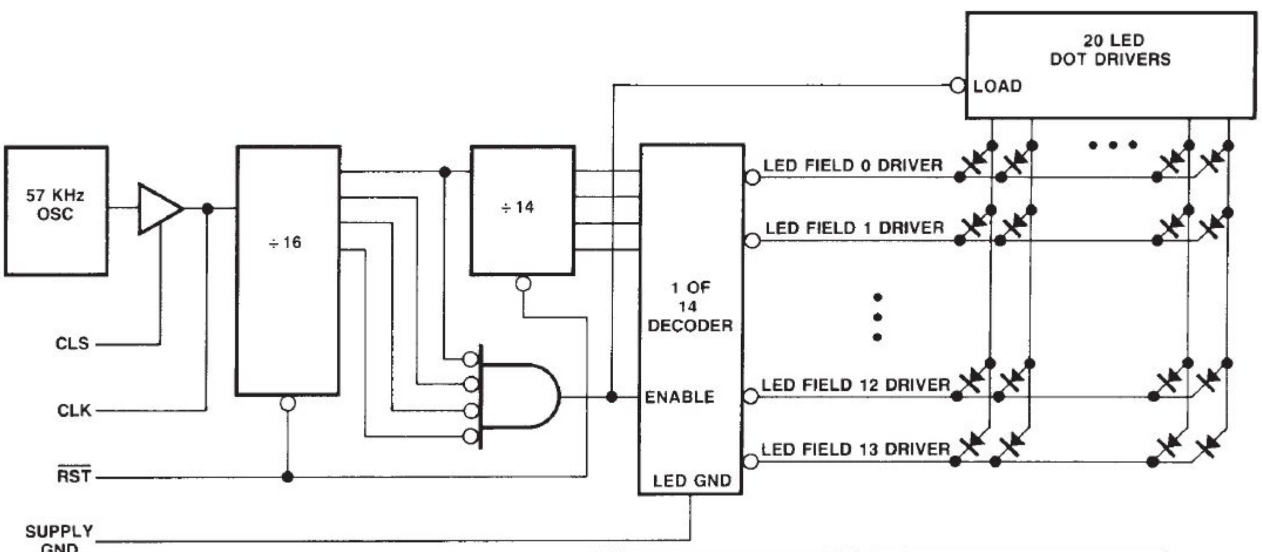
Application Note 1039

Introduction

The seven programmable dimming levels available with the HDSP-213X military grade displays are enough for many applications. However, night vision imaging system (NVIS) applications require the display to be dimmed well below the lowest programmable dimming level. This application note describes a circuit that will dim HDSP-213X displays to luminance levels which meet NVIS lighting requirements.

The Dimming Concept

The key to dimming the HDSP-213X display is to synchronize an external pulse width modulation (PWM) circuit with the internal LED driver refresh circuit. The 280 LED pixels are organized into 14 fields of 20 LEDs per field. The on-board IC illuminates the display by sequentially turning ON each of the 14 fields. The external circuit enables each field driver for a very short amount of time and disables it for the remaining time.



STROBING TRUTH TABLE

Divide By 16	Divide By 14	LED Field Driver
0	0	All LED Field Drivers off. Load Dot Data for LED Field 0 Driver
1-15	0	LED Field 0 Driver on
0	1	All LED Field Drivers off. Load Dot Data for LED Field 1 Driver
1-15	1	LED Field 1 Driver on
▼	▼	▼

Figure 1. HDSP-213X Internal Refresh Circuit Block Diagram

Figure 1 shows the HDSP-213X internal refresh circuit block diagram. The refresh circuit is controlled either by an internal 57 kHz clock or by an external clock. The CLS pin selects the clock source. The CLK pin either inputs the external clock or outputs the internal clock. The clock frequency is first divided by 16 and then by 14. The four outputs from the divide by 14 counter select each of the 14 LED field drivers. The outputs from the divide by 16 counter provide interdigit blanking between the field drivers. Each field driver is selected for 16 clock pulses. The first clock pulse blanks the LED field drivers while data is loaded into the LED driver register. The next 15 clock pulses turn ON one field driver. Thus, each field driver is ON for 15 clock cycles out of a possible 16 (100% brightness level only). The process is repeated for each of the 14 fields of LEDs. To maintain a uniform appearance a PWM circuit must enable each field driver for the same amount of time. Therefore, an external circuit must synchronize an external divide by 16 counter to the display internal divide by 16 counter. This is accomplished by using a common external clock and by resetting both counters with a common reset signal.

Figure 2 shows the block diagram of a synchronized external dimming circuit.

A common clock synchronizes the display refresh circuit and the external dimming circuit. A common reset pulse synchronizes the counters. After four clock pulses, the external counter triggers a variable one-shot. This causes the LED drivers to turn ON for a known period. The display brightness is directly proportional to the amount of time that the LEDs are ON.

An HDSP-213X display has two electrically isolated ground pins, one for the IC logic and the other for the LEDs. The supply ground can be independently raised to V_{DD} with respect to the display logic and system ground. This causes the LEDs to turn OFF and blank the display without effecting the IC operation. Therefore, the display can be dimmed to very low luminance levels by pulse width modulating the supply ground with an external dimming circuit.

The minimum display brightness is determined by the minimum display refresh rate and the minimum time needed to enable the field driver. A display refresh rate of 100 Hz or faster ensures flicker free operation. Thus, the external clock frequency should be greater than or equal to 14 x 16 x 100 Hz = 22.4 kHz. At this frequency and 100% brightness level each field driver would be ON for (15) (1/22.4 kHz) = 670 µs. The minimum time needed to enable the field drivers is 350 ns. Therefore, the minimum achievable dimming level is 350 ns / 670 µs x 100 = 0.05%.

The programmable dimming level must be set at full brightness when using the external dimming circuit. This is accomplished by setting Control Word bits 0, 1, and 2 to logic low.

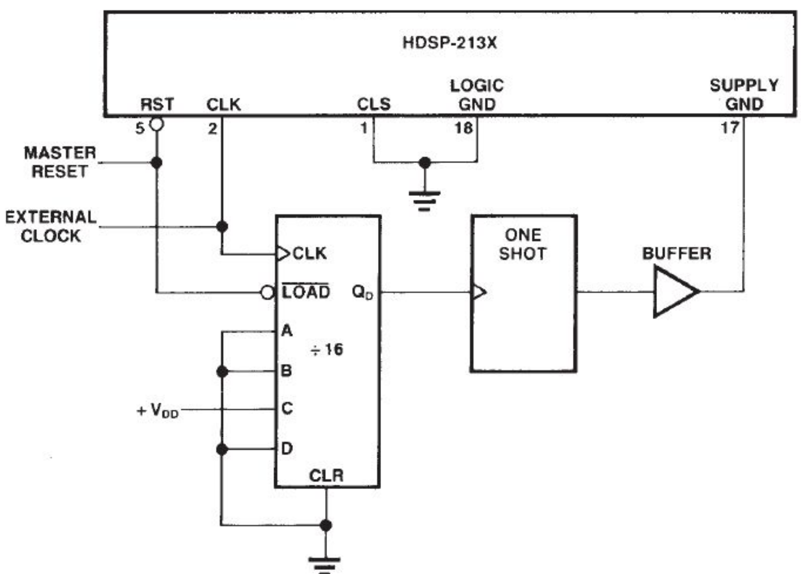


Figure 2. Block Diagram for a Synchronized External Dimming Circuit

Description of the Dimming Circuit

Figure 3 shows an external NVIS dimming circuit. The master reset synchronizes the circuit and the display. The master reset should be pulsed low after power-up and after each control word clear. The external clock simultaneously increments the 74LS193 four-bit synchronous binary counter and the display. When the 74LS193 increments from 0111 to 1000 the Q_D output from the 74LS193 switches from a logic low to a logic high. This rising edge triggers the 74LS221 one-shot to enable the display for a fixed time. The duration of this pulse is determined by a variable logarithmic timing resistor and capacitor. The output pulse from the one-shot is buffered by a 2N3904 and a 2N3054 high current power transistor.

One 2N3054 high current power transistor is required for each HDSP-213X display to act as the LED supply ground switch. Because this pulse occurs once each 16 clock cycles, each of the 14 LED field drivers is pulsed identically.

The use of an external clock is recommended. Since the on-board oscillator operates at 57 kHz, the minimum achievable dimming level is 350 ns/ 263 µs x 100 = 0.13%. This level is too high for NVG operation. Secondly, the frequency of the internal oscillator frequency varies with temperature. This causes the display intensity to vary with temperature. The performance of this circuit has been tested using a 22.4 kHz external clock. An HDSP-2133 display was filtered with an NVG/DV filter and viewed through GEN II and GEN III night vision goggles. One-shot pulses from 350 ns to 1000 ns have been found to provide the best performance.

For additional information see Application Note 1030, *LED Displays and Indicators and Night Vision Imaging System (NVIS) Lighting.*

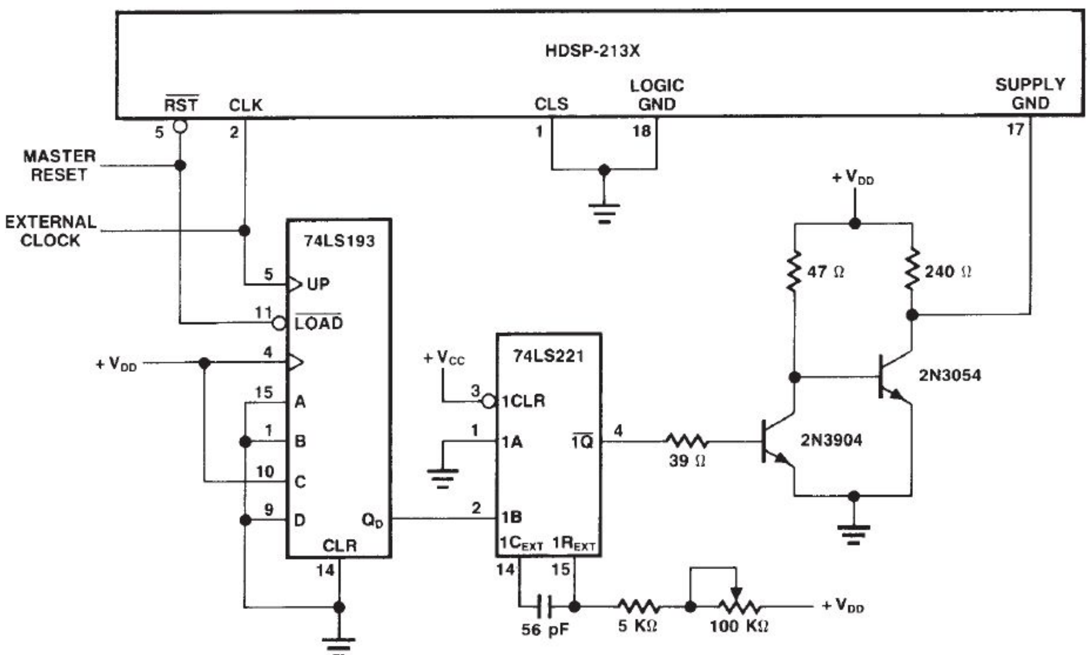


Figure 3. External NVG Dimming Circuit for the HDSP-213X

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

5952-0708EN - July 14, 2010