HEWLETT PACKARD

APPLICATION NOTE 1033

Designing with the HDSP-211X Smart Display Family

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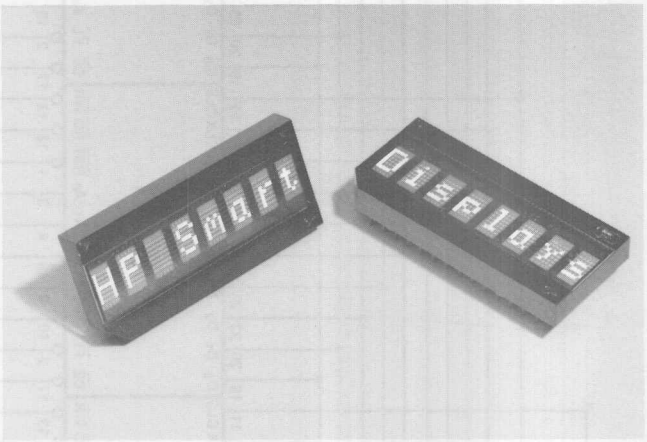

INTRODUCTION

Hewlett-Packard's smart alphanumeric display, the HDSP-211X, is built to optimize the user's display design. Each HDSP-211X has an on-board CMOS IC which displays eight alphanumeric characters. The CMOS IC consists of an eight byte Character RAM, an 8 bit Flash RAM, a 128 character ASCII decoder, a 16 symbol User-Defined Character (UDC) RAM, a UDC Address Register, a Control Word Register and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 x 7 dot matrix characters. Designers should treat the HDSP-211X as a RAM, whose purpose is to store and display a combination of ASCII characters, UDC symbols and control information.

This application note is intended to serve as a design and application guide for users of the HDSP-211X. The user is assumed to be familiar with the HDSP-211X data sheet or to have a copy available. The information presented will cover interfacing the HDSP-211X to either a Motorola 6808 or an Intel 8085 microprocessor. The 6808 and 8085 microprocessors have been selected as typical 8 bit microprocessors. The 6808 has a single R/$\overline{W}$ line and does not multiplex the address and data bus. The 8085 has separate $\overline{Read}$ and $\overline{Write}$ lines and does multiplex the address and data lines. These approaches may be used with most microprocessor systems. Different length display systems may be created with simple modifications to the hardware and software described in this application note.

6808 HARDWARE INTERFACE

The circuit in Figure 1 illustrates how to interface an HDSP-211X to a Motorola 6808 microprocessor. The display interfaces directly to the 6808 bus with the addition of a 74LS138 decoder and a 74LS373 transparent latch.

The 74LS138 is used to generate individual Chip Enables for each of the HDSP-211X displays. These Chip Enables are generated by ANDing a combination of the higher order address bits (A_8, A_9, and A_{10}) with E and VMA. Based on the circuit shown in Figure 1, the displays are memory mapped at locations 0400h, 0500h, 0600h and 0700h. Since the address bus is only partly decoded, other address combinations can also access the display.

The 74LS373 is used to generate the address information for the HDSP-211X displays. The 74LS373 is used to hold this address information stable after the Chip Enable goes high. VMA and E are used to gate the latch enable to ensure that valid address information is stored in the latch.

Figure 2 shows how the six low order address lines are connected to the display. The latch outputs corresponding to microprocessor outputs A_0-A_4 are connected to the same display address inputs. The output corresponding to A_5 is connected to the display $\overline{FL}$ input. Thus each display requires 64 bytes of memory space.

Separate Read and Write signals are generated for the display by using an inverter on the microprocessor R/$\overline{W}$

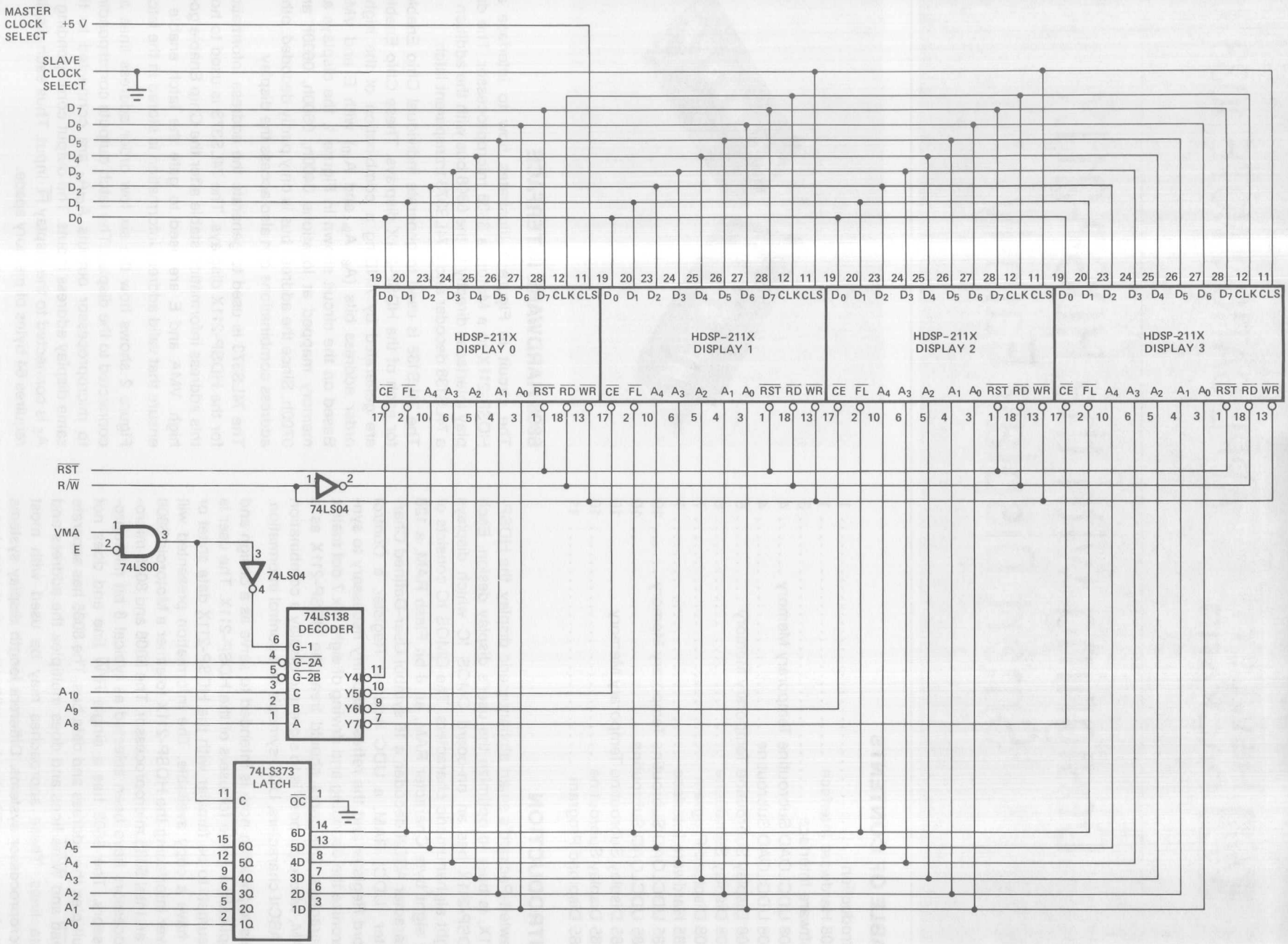

Figure 1. 32 Character Interface to 6808 Microprocessor

A_5	A_4	A_3	A_2	A_1	A_0	Microprocessor Address line	
FL	A_4	A_3	A_2	A_1	A_0	Display Inputs	
0	X	X	0	0	0	Flash RAM	LeftMost Digit of the Display
0	X	X	1	1	1	Flash RAM	RightMost Digit of the Display
1	0	0	X	X	X	UDC Address Register	
1	0	1	0	0	0	UDC RAM	Top Row
1	0	1	1	1	0	UDC RAM	Bottom Row
1	0	1	1	1	1	Ignored	
1	1	0	X	X	X	Control Word Register	
1	1	1	0	0	0	Character RAM	LeftMost Digit of the Display
1	1	1	1	1	1	Character RAM	RightMost Digit of the Display

Figure 2. Mapping of the Lower Order Microprocessor Address Lines

output. Although the display read function is selected even when the display is not addressed, since the Chip Enable is high, the display data lines are tristated. Information is passed on the microprocessor data bus, D_0-D_7, to the display data lines, D_0-D_7, when either the Read or the Write input is held low and the display Chip Enable is held low.

The Reset, Clock I/O and Clock Select lines are used to synchronize systems with multiple displays. The circuit is drawn so that the clock of the first display is the master clock for the other displays. The Reset lines are connected to make a display master reset. The displays will be synchronized after the system has been reset by holding the master reset low for at least 300 ns.

The display system may be lengthened by adding HDSP-211X displays and connecting the display pins to the appropriate microprocessor pins. The Chip Enable pin has to be connected to an unused output from the 74LS138 decoder. The display system can be shortened by removing HDSP-211X displays from the system.

SOFTWARE INTERFACE

The HDSP-211X is easy to program. There are five blocks (Control Word register, UDC Address register, UDC RAM, Flash RAM, and Character RAM) within the IC which influence the operation of the display. The designer can control the operation of these blocks through his software program. The recommended sequence to program these blocks is to set the programmable features (Control Word register); store the custom characters (UDC Address register and UDC RAM); set the individual characters to be flashed (Flash RAM); and load the message to be displayed (Character RAM). Using this sequence ensures that the message appears on the display as expected. Described in the following paragraphs are a series of software programs written to load custom characters into the UDC RAM and to load ASCII text into the Character RAM. This sequence can be encoded using a main program and two subroutines. One subroutine is used to load custom characters from a table to the display UDC RAM. The other subroutine is used to load character data from another table to the display Character RAM.

```
SOURCE STATEMENTS                    COMMENTS
DISP0FL     EQU     0400h            Flash RAM Display 0
DISP1FL     EQU     0500h            Flash RAM Display 1
DISP2FL     EQU     0600h            Flash RAM Display 2
DISP3FL     EQU     0700h            Flash RAM Display 3

DISP0UA     EQU     0420h            UDC Addr. Reg Display 0
DISP1UA     EQU     0520h            UDC Addr. Reg Display 1
DISP2UA     EQU     0620h            UDC Addr. Reg Display 2
DISP3UA     EQU     0720h            UDC Addr. Reg Display 3

DISP0UD     EQU     0428h            UDC RAM Display 0
DISP1UD     EQU     0528h            UDC RAM Display 1
DISP2UD     EQU     0628h            UDC RAM Display 2
DISP3UD     EQU     0728h            UDC RAM Display 3

DISP0CW     EQU     0430h            Control Word Display 0
DISP0CW     EQU     0530h            Control Word Display 1
DISP0CW     EQU     0630h            Control Word Display 2
DISP0CW     EQU     0730h            Control Word Display 3

DISP0CH     EQU     0438h            Character RAM Display 0
DISP1CH     EQU     0538h            Character RAM Display 1
DISP2CH     EQU     0638h            Character RAM Display 2
DISP3CH     EQU     0738h            Character RAM Display 3
```

Figure 3. Address Locations and Labels Associated With Each Block in a 32 Character Message System

To program each display it is necessary to know the address of each block within each display. Figure 3 shows the address locations and the labels associated with each block for the 32 character addressing schemes shown in Figure 1 and 15. A_6 and A_7 are not decoded so each display occupies 256 bytes of memory. The display is memory mapped at location XXYY hex. The most significant byte, XX, is the HDSP-211X location and the least significant byte, YY, is the location of a block within the display. The four displays are located at memory locations 04YYh, 05YYh, 06YYh, and 07YYh, where 04YYh is the location of the leftmost display and 07YYh is the location of the rightmost. Flash RAM data is stored from location XX00h to location XX07h, where XX00h is associated with the leftmost character of a display and XX07h is the rightmost character of a display. The UDC Address register is located in location XX20h. The top row of the UDC RAM is located at location XX28h and the bottom row at location XX2Eh. The Control Word register is located XX30h. Character data is stored from XX38h to XX3Fh, where XX38h is the leftmost character of the display and XX3Fh is the rightmost character of the display.

Figure 4 shows the location and labels for the main program, subroutines and data. DISPLOAD is the main program which calls and passes information to the subroutines. UDCLOAD is a subroutine which loads 16 Custom Characters into one HDSP-211X. TABLEDOT is the location of the top row of the first UDC symbol. DISPLAY is a subroutine which loads the Character RAM of one HDSP-211X. CHAR is the location of the leftmost character in the message.

6808 UDCLOAD SUBROUTINE TEMPORARY MEMORY

Figure 5 shows four memory locations that are used for temporary storage by the UDCLOAD subroutine. Three locations are used to store information passed from the main program to the subroutine. The fourth is used as an internal counter.

UDCADDR stores the memory location of the UDC Address register (XX20h) for the UDCLOAD subroutine. The content of UDCADDR will be XX20h when the subroutine finishes execution.

UDCRAMR stores the memory location of the top row of the UDC RAM (XX28h) for the UDCLOAD subroutine. The content of the UDCRAMR will be XX28h when the subroutine finishes executing.

UDCDATAT stores the location of the first character in TABLEDOT (0820h) for the UDCLOAD subroutine. The content of UDCDATAT will be 088Fh when the subroutine has finished execution.

COUNT is used by the UDCLOAD to keep track of which character is being loaded into the UDC RAM. The user does not need to initialize COUNT prior to executing UDCLOAD.

6808 UDCLOAD SUBROUTINE

Figure 6 shows the program listing for the UDCLOAD subroutine. This routine transfers UDC dot data from main memory to one display UDC RAM. Two loops are used to load the UDC RAM. The outer loop, labeled NUDC, is repeated 16 times, one time for each UDC RAM location. COUNT Is used to keep track of the number of times NUDC has been executed. NUDC loads the UDC Address register with the address of a UDC symbol. The inner loop, labeled NROW, is executed seven times for each execution of NUDC. NROW loads data into the UDC RAM row by row starting with the top row and ending with the bottom row. Three pieces of information are passed to the subroutine. They are the memory locations of the UDC Address register (UDCADDR), the UDC RAM (UDCRAMR) and the UDC data table (UDCDATAT).

```
SOURCE STATEMENTS                    COMMENTS
DISPLOAD    EQU     0100h    Displays 32 char. Message
UDCLOAD     EQU     0200h    Subroutine to load UDC RAM
TABLEDOT    EQU     0820h    Dot Information for UDC RAM
DISPLAY     EQU     0000h    Subroutine to load Char. RAM
CHAR        EQU     0300h    32 Character Message
```

Figure 4. Location and Labels for the Main Program, Subroutines and Data

```
LOC                     ORG     $0250h
0250    UDCADDR         RMB     2       UDC Address Register Data
0252    COUNT           RMB     1       UDC pointer
0253    UDCDATAT        RMB     2       UDC dot data
0255    UDCRAMR         RMB     2       UDC row
```

Figure 5. Memory Location Used to Pass Information from the Main Program to the Subroutines.

```
LOC  OBJECT CODE      ORG      $0200h
0200 C6   00    UDCLOAD LDA  B   I,$00
0202 FE   0250  NUDC    LDX      E, UDCADDR   Load UDC Address Register with pointer
0205 E7   00            STA  B   X,$00
0207 5C                 INC  B
0208 F7   0252          STA  B   E,COUNT      Store character counter
020B C6   00            LDA  B   I,$00        Load row counter
020D FE   0253  NROW    LDX      E,UDCDATAT   Load Accumulator A with dot data
0210 A6   00            LDA  A   X,$00
0212 08                 INX                   Store address of next dot data
0213 FF   0253          STX      E,UDCDATAT
0216 FE   0255          LDX      E,UDCRAMR    Store dot data in UDC RAM
0219 A7   00            STA  A   X,$00
021B 08                 INX                   Store address of next row
021C FF   0255          STX      E,UDCRAMR
021F 5C                 INC  B                Last row of character? No — get next row.
0220 C1   07            CMP  B   I,$07        Yes — adjust UDCRAMRT to top
0222 26   E9            BNE      NROW         row of char
0224 F6   0256          LDA  B   E,UDCRAMR+1
0227 CO   07            SUB  B   I,$07
0229 F7   0256          STA  B   E,UDCRAMR+1
022C F6   0252          LDA  B   E, COUNT     Last character? No — load
022F C1   10            CMP  B   I,$10        next character. Yes — return
0231 26   CF            BNE      NUDC
0233 39                 RTS
```

Figure 6. Subroutine to Load the UDC RAM with Custom Symbols

Memory table "TABLEDOT" is organized as shown in Figure 7. Each of the 16 symbols is specified in a block of seven memory locations. The first symbol is stored in UDC RAM location 0 hex and the last symbol is stored in UDC RAM location F hex. The first location within a block is the top row of a symbol and the last location in a block is the bottom row.

Figure 8 shows how a greater than or equal to, "≥", sign can be created as a UDC symbol. Executing the UDCLOAD subroutine with 0420h stored at UDCADDR, 0428h stored at UDCRAMR and 0820 stored at UDCDATAT will cause the "≥" sign to be stored in of the leftmost display UDC RAM location 0h. The subroutine will also load the fifteen

MEMORY LOCATION	UDC CHARACTER	ROW
0820	0h	1
0821	0h	2
:		
:		
0827	0h	7
:		
:		
0889	Fh	1
088F	Fh	7

Figure 7. Organization of UDC Data to be Used with the UDCLOAD Routine

MEMORY LOCATION	HEX DATA	1 D4	2 D3	3 D2	4 D1	5 D0		Oh UDC CHARACTER
0820	08	0	1	0	0	0	ROW 1	*
0821	04	0	0	1	0	0	ROW 2	*
0822	02	0	0	0	1	0	ROW 3	*
0823	04	0	0	1	0	0	ROW 4	*
0824	08	0	1	0	0	0	ROW 5	*
0825	00	0	0	0	0	0	ROW 6	
0826	1F	1	1	1	1	1	ROW 7	* * * * *

0 = logic 0; 1 = logic 1; * = illuminated LED

Figure 8. Data to load "≥" into the UDC RAM

other UDC RAM locations. To display this symbol, 80 hex has to be stored in the Character RAM of the leftmost display.

6808 DISPLAY SUBROUTINE TEMPORARY MEMORY

Figure 9 shows two memory locations which are used for temporary storage by the DISPLAY subroutine.

TABLECH stores the memory location of the leftmost character of the message (0300h) to be displayed for the DISPLAY subroutine. After the execution of DISPLAY, the value stored in TABLECH will have been incremented by 8. Thus, for systems consisting of multiple HDPS-211Xs, TABLECH needs to be initialized only for the leftmost display.

DISPL stores the memory location of the Character RAM (XX38h) for the DISPLAY subroutine. The contents of DISPL will be XX3F when the subroutine finishes execution.

```
0257 TABLECH    RMB 2 Character pointer
0259 DISPL      RMB 2 Character RAM address
```

Figure 9. Memory Location Used to Pass Information from the Main Program to the Subroutines.

6808 DISPLAY SUBROUTINE

Figure 10 shows the program listing for the DISPLAY subroutine. This routine transfers character data from main memory to the Character RAM of one display. The program loads all 8 Character RAM locations by executing the loop labeled "NCHAR" 8 times. The leftmost character is loaded first and the rightmost is loaded last. Two pieces of information are passed to the subroutine. They are the location of the Character RAM (DISPL) and the location of the message (TABLECH). For display systems using more than one HDSP-211X, the subroutine will remember the location of the next 8 byte block of the message. Figure 11 shows the organization of a 32 character message.

MEMORY LOCATION	DISPLAY ADDRESS
0300	0438
0307	043F
0308	0538
:	
:	
:	
031F	073F

Figure 11. Organization of a 32 Character Message used with the Display Routines

```
LOC  OBJECT CODE        ORG     $0000
0000 C6   08   DISPLAY  LDA  B  I, $08
0002 FE   0257 NCHAR    LDX     E,TACLECH   Load character into
0005 A6   00            LDA  A  X,$00       Accumulator A
0007 08                 INX                 Set pointer to address of next
0008 FF   0257          STX     E,TABLECH   character
000B FE   0259          LDX     E,DISPL     Store character in display
000E A7   00            STA  A  X,$00       Character RAM
0100 08                 INX                 Set display address to next
0011 FF   0259          STX     E,DISPL     location
0014 5A                 DEC  B              End of Display? NO — get next
0015 C1   00            CMP  B  I,$00       character. Yes — return to main
0017 26   E9            BNE     NCHAR       program.
0019 39                 RTS
```

Figure 10. Subroutine to Load Character RAM

Figure 12 shows how a 32 character message is stored in memory for use with the DISPLAY subroutine. Figure 13 shows how this message will look after executing the DISPLOAD program.

MEMORY LOCATION	ASCII DATA	ASCII CHARACTER	DISPLAY ADDRESS
0300	54	T	0438
0301	68	h	0439
0302	69	i	043A
0303	73	s	043B
0304	20	(space)	043C
0305	73	s	043D
0306	68	h	043E
0307	6F	o	043F
0308	77	w	0538
0309	73	s	0539
030A	20	(space)	053A
030B	63	c	053B
030C	75	u	053C
030D	73	s	053D
030E	74	t	053E
030F	6F	o	053F
0310	6D	m	0638
0311	20	(space)	0639
0312	63	c	063A
0313	68	h	063B
0314	61	a	063C
0315	72	r	063D
0316	61	a	063E
0317	63	c	063F
0318	74	t	0738
0319	65	e	0739
031A	72	r	073A
031B	73	s	073B
031C	20	(space)	073C
031D	80	≥	073D
031E	21	!	073E
031F	20	(space)	073F

Figure 12. ASCII Data Stored in Memory for Use by the Display Routine

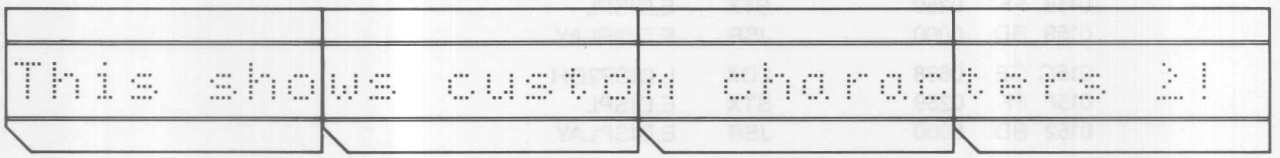

Figure 13. 32 Character Message

6808 DISPLOAD PROGRAM

Figure 14 shows listing of the DISPLOAD program. This program loads the UDC RAMs of four HDSP-211X displays and displays a 32 character message. The UDCLOAD subroutine is executed four times to load the UDC RAMs of all displays. The DISPLAY subroutine is executed four times to load a 32 character message.

The DISPLOAD program is written to load the UDC RAM and display a message. For each display in the system, the UPCLOAD subroutine must be executed once per display to load the UDC RAM. To display a message, the DISPLAY subroutine has to be executed once for each display in the system. The UDC RAM of each display in the system has to be loaded with UDC data before the first DISPLAY subroutine is executed.

8085 HARDWARE INTERFACE

The circuit in Figure 15 shows how to interface an HDSP-211X to an INTEL 8085 microprocessor. The display interfaces directly to the 8085 bus with the addition of a 74LS138 decoder.

The 74LS138 is used to generate individual Chip Enables for each of the HDSP-211X displays. These Chip Enables are created by decoding the higher order address bits (A_8, A_9, and A_{10}). Based on the circuit shown in Figure 15, the displays are memory mapped at location 04YYh, 05YYh, 06YYh and 07YYh. Since the address bus is only partly decoded, other address combinations can also access the display.

Figure 2 shows how the six lower order microprocessor address lines are connected to the display. Each display uses 64 memory locations. The display Address inputs must be held stable after the Chip Enable signal goes high. The 8085 multiplexes A_0-A_7 and D_0-D_7 on the same bus. A latch is required to isolate A_0-A_7 from D_0-D_7. This latch provides the necessary hold time. The latch outputs corresponding to microprocessor outputs A_0-A_4 are connected to the same display Address inputs. The output corresponding to A_5 is connected to the display $\overline{FL}$ input.

The 8085 has separate Read and Write lines which are connected directly to the display Read and Write lines. Information is passed on the microprocessor data bus, D_0-D_7, to the display data lines, D_0-D_7, when either the Read or the Write inpute is held low and the display Chip Enable is held low.

The Reset, Clock I/O and Clock Select lines are used to synchronize systems with multiple displays. The circuit is drawn so that the clock of the first display is the master clock for the other displays. The Reset lines are connected to make a display master reset. The display will be synchronized after the system has been reset by holding the master reset low for at least 300 ns.

```
LOC  OBJECT CODE      ORG    $0100
0100 CE  0420 DISPLOAD LDX    I,DISP0UA
0103 FF  0250          STX    E,UDCADDR
0106 CE  0428          LDX    I,DISP0UD
0109 FF  0255          STX    E,UDCRAMR
010C CE  0820          LDX    I,TABLEDOT
010F FF  0253          STX    E,UDCDATAT     Load leftmost Display
0112 BD  0200          JSR    E,UDCLOAD      UDC RAM

0115 CE  0520          LDX    I,DISP1UA
0118 FF  0250          STX    E,UDCADDR
011B CE  0528          LDX    I,DISP1UD
011E FF  0255          STX    E,UDCRAMR
0121 CE  0820          LDX    I,TABLEDOT
0124 FF  0253          STX    E,UDCDATAT
0127 BD  0200          JSR    E,UDCLOAD

012A CE  0620          LDX    I,DISP2UA
012D FF  0250          STX    E,UDCADDR
0130 CE  0628          LDX    I,DISP2UD
0133 FF  0255          STX    E,UDCRAMR
0136 CE  0820          LDX    I,TABLEDOT
0139 FF  0253          STX    E,UDCDATAT
013C BD  0200          JSR    E,UDCLOAD

013F CE  0720          LDX    I,DISP3UA
0132 FF  0250          STX    E,UDCADDR
0135 CE  0728          LDX    I,DISP3UD
0138 FF  0255          STX    E,UDCRAMR
013B CE  8720          LDX    I,TABLEDOT
013E FF  0253          STX    E,UDCDATAT     Load rightmost Display
0141 BD  0200          JSR    E,UDCLOAD      UDC RAM

0144 CE  0300          LDX    I,CHAR
0147 FF  0257          STX    E,TABLECH
014A CE  0438          LDX    I,DISP0CH
014D FF  0259          STX    E,DISPL        Load leftmost Display
0150 BD  0000          JSR    E,DISPLAY      Character RAM

0153 CE  0300          LDX    I,DISP1CH
0156 FF  0259          STX    E,DISPL
0159 BD  0000          JSR    E,DISPLAY

015C CE  0638          LDX    I, DISP2CH
015F FF  0259          STX    E,DISPL
0162 BD  0000          JSR    E,DISPLAY

0165 CE  0738          LDX    I,DISP3CH
0168 FF  0259          STX    E,DISPL        Load rightmost Display
016B BD  0000          JSR    E,DISPLAY      Character RAM
```

Figure 14. Main Program to Call UDCLOAD and DISPLAY Subroutines

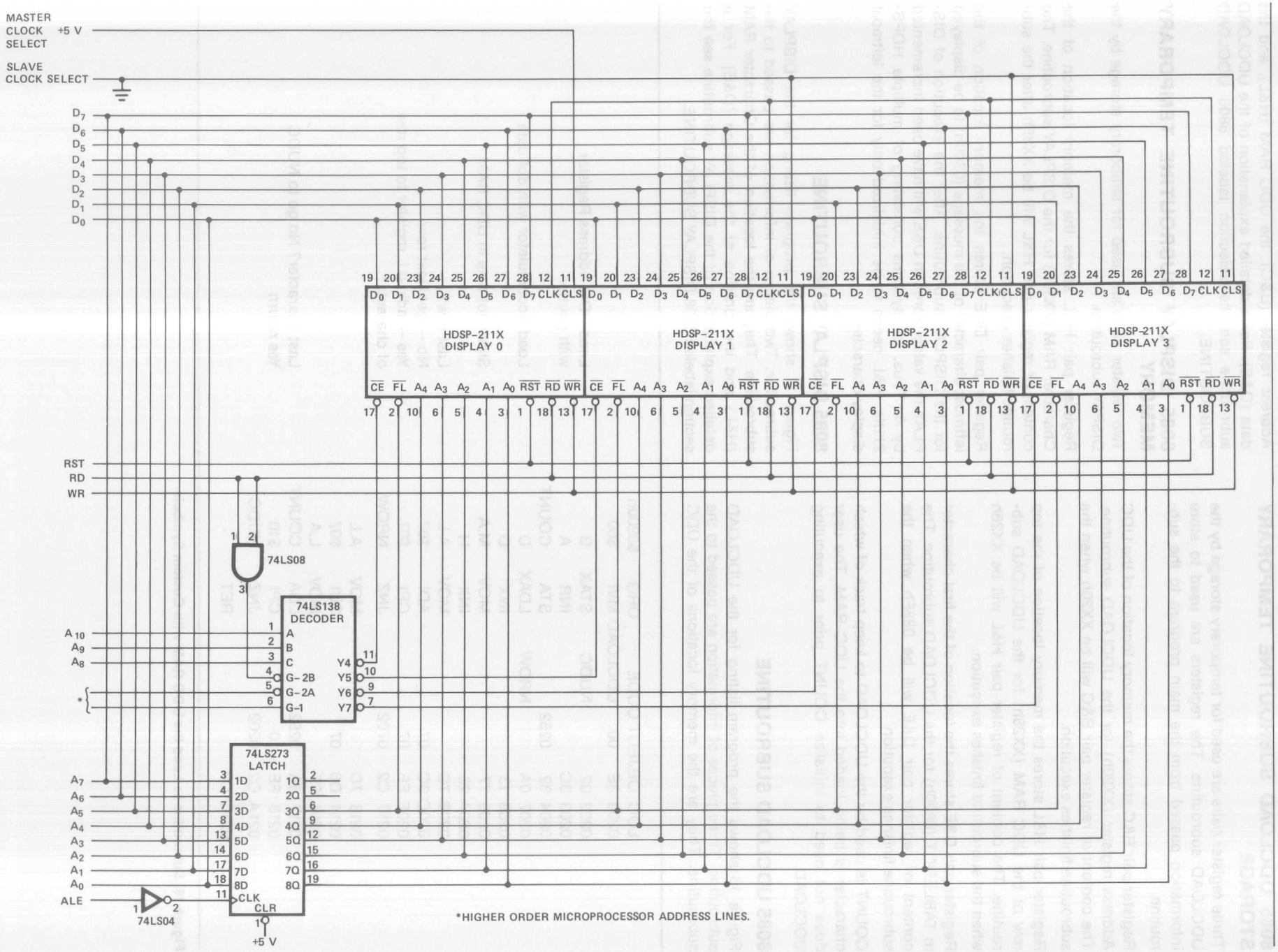

Figure 15. Character Interface to 8085 Microprocessor

8085 UDCLOAD SUBROUTINE TEMPORARY STORAGE

Three register pairs are used for temporary storage by the UDCLOAD subroutine. The registers are used to store information passed from the main program to the subroutine.

Register pair B&C stores the memory location of the UDC Address register (XX20h) for the UDCLOAD subroutine. The content of register pair B&C will be XX20h when the subroutine finishes execution.

Register pair H&L stores the memory location of the top row of the UDC RAM (XX28h) for the UDCLOAD subroutine. The content of register pair H&L will be XX28h when the subroutine finishes execution.

Register pair D&E stores the location of the first character in TABLEDOT (0820h) for the UDCLOAD subroutine. The content of register pair D&E will be 088Fh when the subroutine finishes execution.

COUNT is used by the UDCLOAD to keep track of which character is being loaded into the UDC RAM. The user does not need to initialize COUNT prior to executing UDCLOAD.

8085 UDCLOAD SUBROUTINE

Figure 16 shows the program listing for the UDCLOAD subroutine. Three pieces of information are passed to the subroutine. They are the memory locations of the UDC Address register (B&C), the UDC RAM (H&L), and the data (D&E). For a detailed explanation of the UDCLOAD subroutine see the selection labeled 6808 UDCLOAD SUBROUTINE.

8085 DISPLAY SUBROUTINE TEMPORARY MEMORY

Two register pairs are used for temporary storage by the DISPAY subroutine.

Register pair H&L stores the memory location of the Character RAM (XX38h) for the DISPLAY subroutine. The content of register pair H&L will be XX3Fh after the subroutine finishes execution.

Register pair D&E stores the memory location of the leftmost character of the message (0300h) to be displayed for the DISPLAY subroutine. After the execution of DISPLAY, the value stored in D&E will have been incremented by 8. Thus, for systems consisting of multiple HDPS-211Xs, H&L needs to be initialized only for the leftmost display character.

8085 DISPLAY SUBROUTINE

Figure 17 shows the program listing for the DISPLAY subroutine. Two pieces of information are passed to the subroutine. They are the location of the Character RAM (H&L) and the location of the message (D&E). For a detailed explanantion of the DISPLAY subroutine see the section labeled 6808 DISPLAY SUBROUTINE.

```
LOC  OBJECT CODE        ORG    $0200h
0200 3E   00    UDCLOAD MVI    $00
0202 02         NUDC    STAX   B        Load UDC Address Register
0203 3C                 INR    A        with pointer
0204 32   0252          STA    COUNT
0207 0A         NROW    LDAX   D        Load Accumulator with dot data
0208 13                 INX    D
0209 77                 MOV    M,A      Store dot data in UDC RAM
020A 23                 INX    H
020B 7D                 MOV    A,L      Last row?
020C 3C   07            ADI    $07      No — get Next row
020E FE   07            CPI    $07      Yes — adjust L register to top row
0210 C2   0702          JNZ    NROW     of character
0213 7D                 MOV    A,L
0214 D6   07            SUI    $07
0216 6F                 MOV    L,A
0217 3A   0252          LDA    COUNT    Last character? No go to NUDC
0218 FE   10            CPI    $10      Yes return
021A C2   0202          JNZ    NUDC
021D C9                 RET
```

Figure 16. Subroutine to Load the UDC RAM with Custom Symbols

```
LOC  OBJECT CODE        ORG    $0100
0100 06   00    DISPLAY MVI    B, $00
0102 1A         NCHAR   LDAX   D       Load Accumulator with character data
0103 77                 MOV    M,A     Store data in Character RAM
0104 13                 INX    D       Next character data location
0105 23                 INX    H       Next character RAM location
0106 04                 INR    B
0107 78                 MOV    A,B
0108 FE   08            CPI    $08     Last character? No — go to NEXT
010A C2   0201          JNZ    NCHAR   Yes — return
010D C9                 RET
```

Figure 17. Subroutine to Load Character RAM

8085 DISPLOAD PROGRAM

Figure 18 shows listing of the DISPLOAD program. This program loads the UDC RAMs of four HDSP-211X displays and displays a 32 character message. The UDCLOAD subroutine is executed four times to load the UDC RAMs of all displays. The DISPLAY subroutine is executed four times to load a 32 character message.

The DISPLOAD program is written to load the UDC RAM and display a message. For each display in the system, the UDCLOAD subroutine must be executed once per display to load the UDC RAM. To display a message, the DISPLAY subroutine has to be executed once for each display in the system. The UDC RAM of each display in the system has to be loaded with UDC data before the first DISPLAY subroutine is executed.

```
LOC  OBJECT CODE        ORG    $0000
0000 01   0420  DISPLOAD LXI    B,DISP0UA
0003 11   0820         LXI    D,TABLEDOT
0006 21   0428         LXI    H,DISP0UD
0009 CC   0200         CALL   UDCLOAD

000C 01   0520         LXI    B,DISP1UA
000F 11   0820         LXI    D,TABLEDOT
0012 21   0528         LXI    H,DISP1UD
0015 CC   0200         CALL   UDCLOAD

0018 01   0620         LXI    B,DISP2UA
001B 11   0820         LXI    D,TABLEDOT
001E 21   0628         LXI    H,DISP2UD
0021 CC   0200         CALL   UDCLOAD

0024 01   0720         LXI    B,DISP3UA
0027 11   0820         LXI    D,TABLEDOT
002A 21   0728         LXI    H,DISP3UD
002D CC   0200         CALL   UDCLOAD

0030 11   0300         LXI    D,CHAR
0033 21   0438         LXI    H,DISP0CH
0036 CC   0100         CALL   DISPLAY

0039 21   0538         LXI    H,DISP1CH
003C CC   0100         CALL   DISPLAY

003F 21   0638         LXI    H,DISP2CH
0042 CC   0100         CALL   DISPLAY

0045 21   0738         LXI    H,DISP3CH
0048 CC   0100         CALL   DISPLAY
```

Figure 18. Main Program to Call UDCLOAD and DISPLAY Subroutines