Agilent Technologies
Innovating the HP Way

Interfacing the MC68HC11 to the HCTL-2020

Application Brief M-023

Introduction

This application brief describes two interfaces for the HCTL-2020 to the MC68HC11. One is a port interface and the other is a bus interface.

Port Interface

The connections are shown in Figure 1, the schematic titled "Port Interface". Port C is used to read the data in and 3 pins on port B are used for the control signals to the HCTL-2020. The E clock from the 68HC11E9 is used to clock the HCTL-2020. In this interface it is assumed that the 68HC11E9 is in the single chip mode.

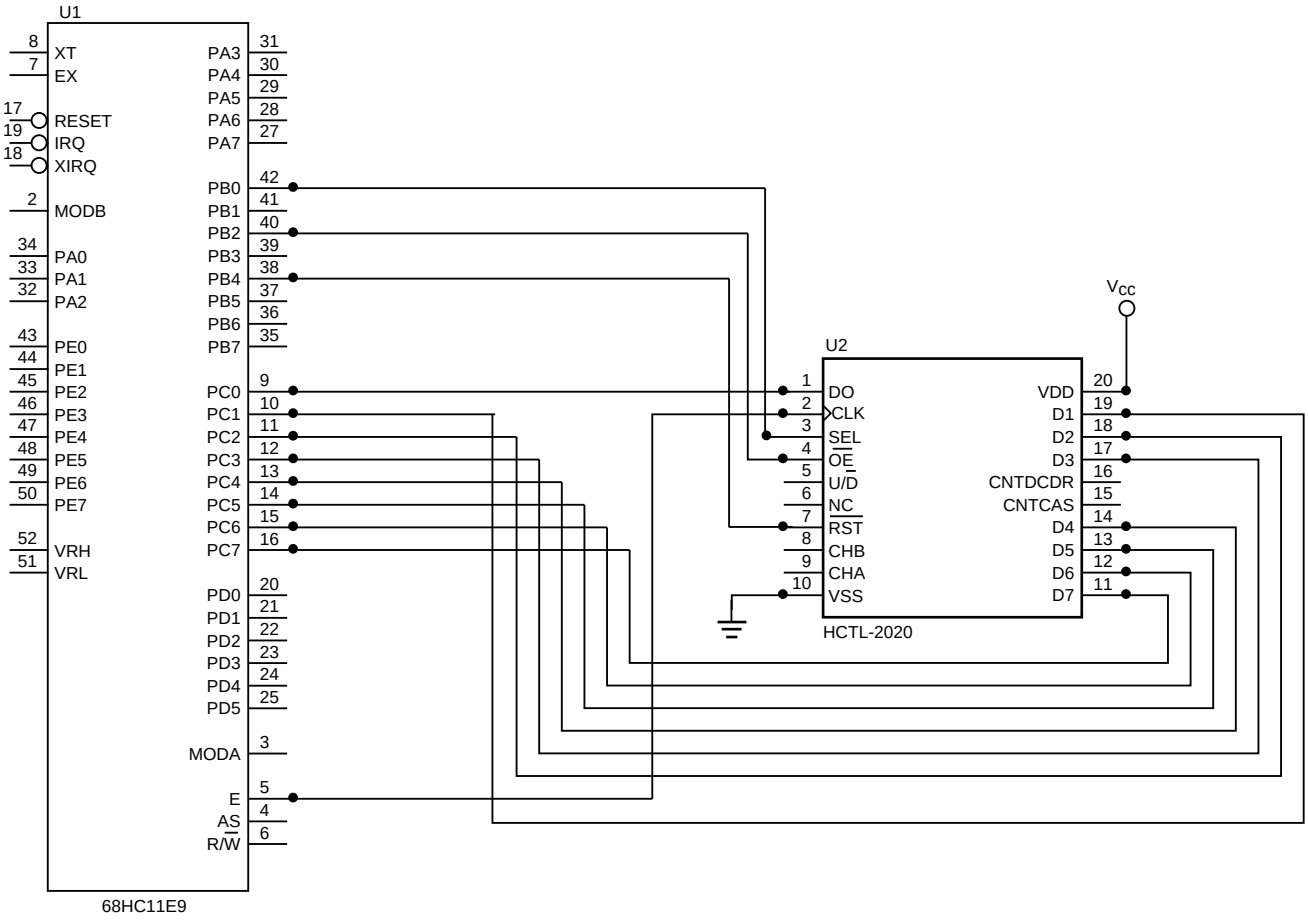
The subroutines to read from the HCTL-2020 and to reset the HCTL-2020 follow.

```
;*************************************************************************
;THIS SUBROUTINE IS USED TO READ DATA FROM THE HCTL-2020
;FOR THE PORT INTERFACE.
;THE SUBROUTINE RETURNS THE 16 BIT DATA FROM THE HCTL-
;2020 IN REGISTER IX.
;* DENOTES ACTIVE LOW SIGNALS.
;*************************************************************************

RD2020:  PSHA        ;SAVE REG A ON STACK.
         PSHB
         LDAA#00
         STAA$1007   ;PUT PORT C IN INPUT MODE.
         LDAA#0FA
         STAA$1004   ;SEL LO AND OE* LO.
         LDAA$1003   ;HIGH BYTE OF DATA IN REG. A.
         LDAB#0FB
         STAB$1004   ;SEL HI AND OE* LO.
         LDAB$1003   ;LO BYTE IN REG. B.
         XGDX        ;REGISTER IX HAS THE 16 BIT VALUE FROM
                     ;THE HCTL-2020
         LDAA#0FF
         STAA$1004   ;SEL HI AND OE* HI.
         PULB        ;RESTORE REG B FROM STACK.
         PULA        ;RESTORE REG A FROM STACK.
         RTS

;*************************************************************************
;THIS SUBROUTINE IS USED TO RESET THE HCTL-2020 IN THE
;PORT INTERFACE.
;*************************************************************************

RST2020: PSHA
         LDAA#0EF
         STAA$1004   ;RST*LO.
         LDAA#0FF
         STAA$1004   ;RST*HI.
         PULA
         RTS
```



NOTE: 68HC11E9 IS IN THE SINGLE CHIP MODE.
REFER TO THE 68HC11E9 REFERENCE MANUAL FOR DETAILS.

Figure 1. Port Interface Schematic.

Bus Interface

In applications where the expanded-mode is already being used, it is convenient to use the bus interface to the HCTL-2020. Figure 2, “Bus Interface Control Signals”, is the schematic diagram to generate the control signals in the expanded mode.

The subroutines to read and reset follow.

```
;*******************************************************************************
;THIS SUBROUTINE READS A VALUE FROM THE HCTL-2020. THE HIGH
;BYTE OF DATA IS RETURNED IN REG IY IN THE CORRECT ORDER OF
;HIGH AND LOW BYTES.
;THE TWO BYTES ARE MAPPED AT THE MEMORY LOCATIONS AT 0CFFOh
;AND 0CFF1h RESPECTIVELY.
;*******************************************************************************


H2020 EQU $0C000

RD2020:  LDY H2020
         RTS


;*******************************************************************************
;THIS SUBROUTINE IS USED TO RESET THE HCTL-2020. THE RESET
;SIGNAL IS MAPPED TO MEMORY LOCATION 0CFF2h.
;*******************************************************************************

REST2020 EQU $0CFF2

RST2020:  PSHA
          LDAA REST2020       ;READ LOCATION $CFF2 TO CAUSE RESET
          PULA
          RTS
```

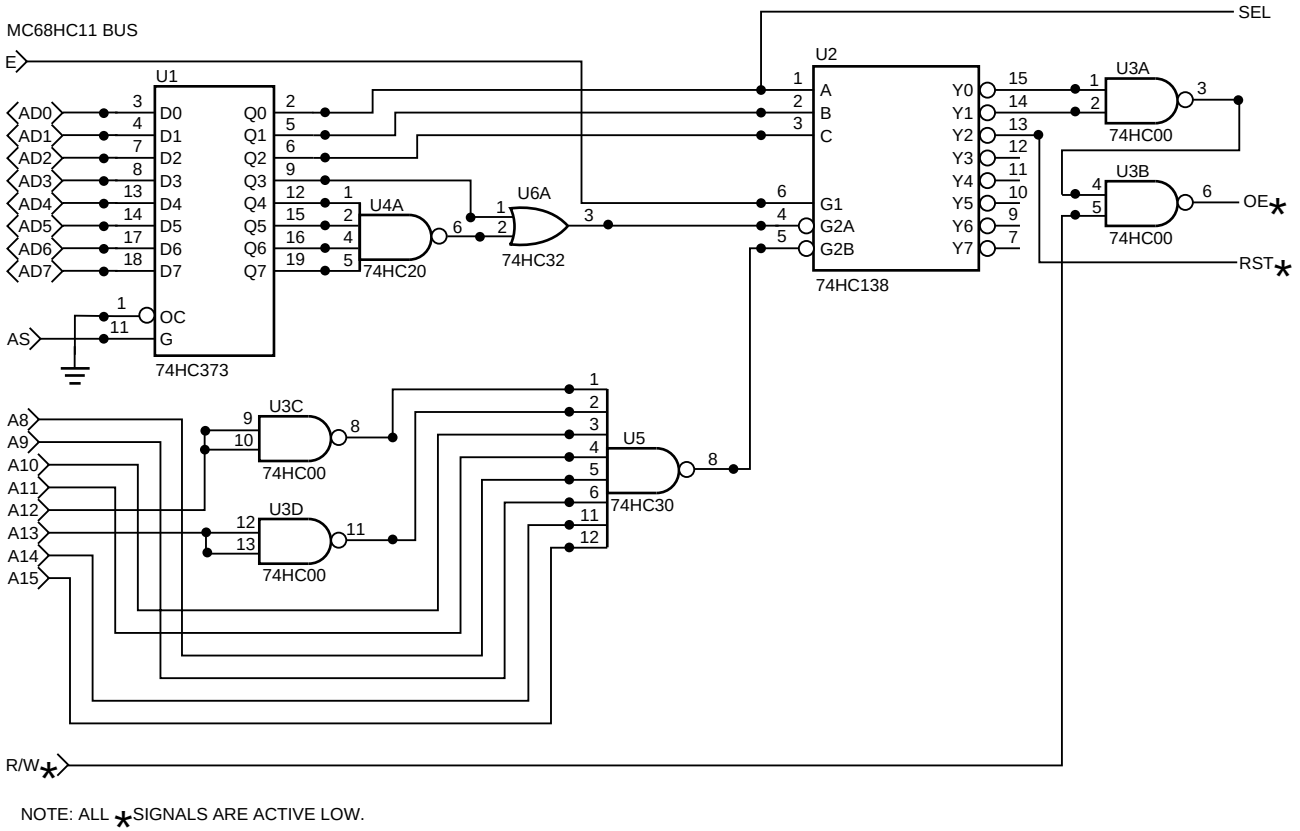


Figure 2. Bus Interface Control Signals.

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