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Interfacing the HCTL-1100 to the MC68HC11

Application Brief M-021

Introduction

This application brief describes two interfaces to the HCTL-1100 with the MC68HC11E9. They are Port Interfacing and Bus Interfacing, respectively. Circuit diagrams for both cases are presented and code to read and write to the HCTL-1100 is supplied. A table showing the read and write cycle timing for both cases is presented for comparison purposes.

For the purpose of the port interfacing the 68HC11 is used in the single-chip mode. Port C is connected to the data/address pins of the HCTL-1100 and four pins on port B are used to control the reading and writing of data from and to the HCTL-1100. The E clock of the 68HC11 is connected to the clock input of the HCTL-1100. The frequency of the E clock is 2 MHz (1/4 the crystal frequency of the 68HC11). This is the highest clock frequency at which the HCTL-1100 can be run.

Port Interfacing

Connections:

E clock of the 68HC11 is connected to HCTL-1100 EXTCLK.

Port C pins PC0-PC5 are connected to the AD0-AD5 respectively.

PC6 to D6.
PC7 to D7.
PB0 to OE.
PB2 to CS.
PB4 to ALE.

PB6 to R/W, as shown in the schematic diagram in Figure 1, “68HC11 to HCTL-1100 Port Interface”.

The table shown below compares the time taken by the read and write routines in the port and bus interfaces.

Table 1. Execution Times

	Read Operation	Write Operation
Port Interface	30.5 µs	26 µs
Bus Interface	14.5 µs	12.5 µs

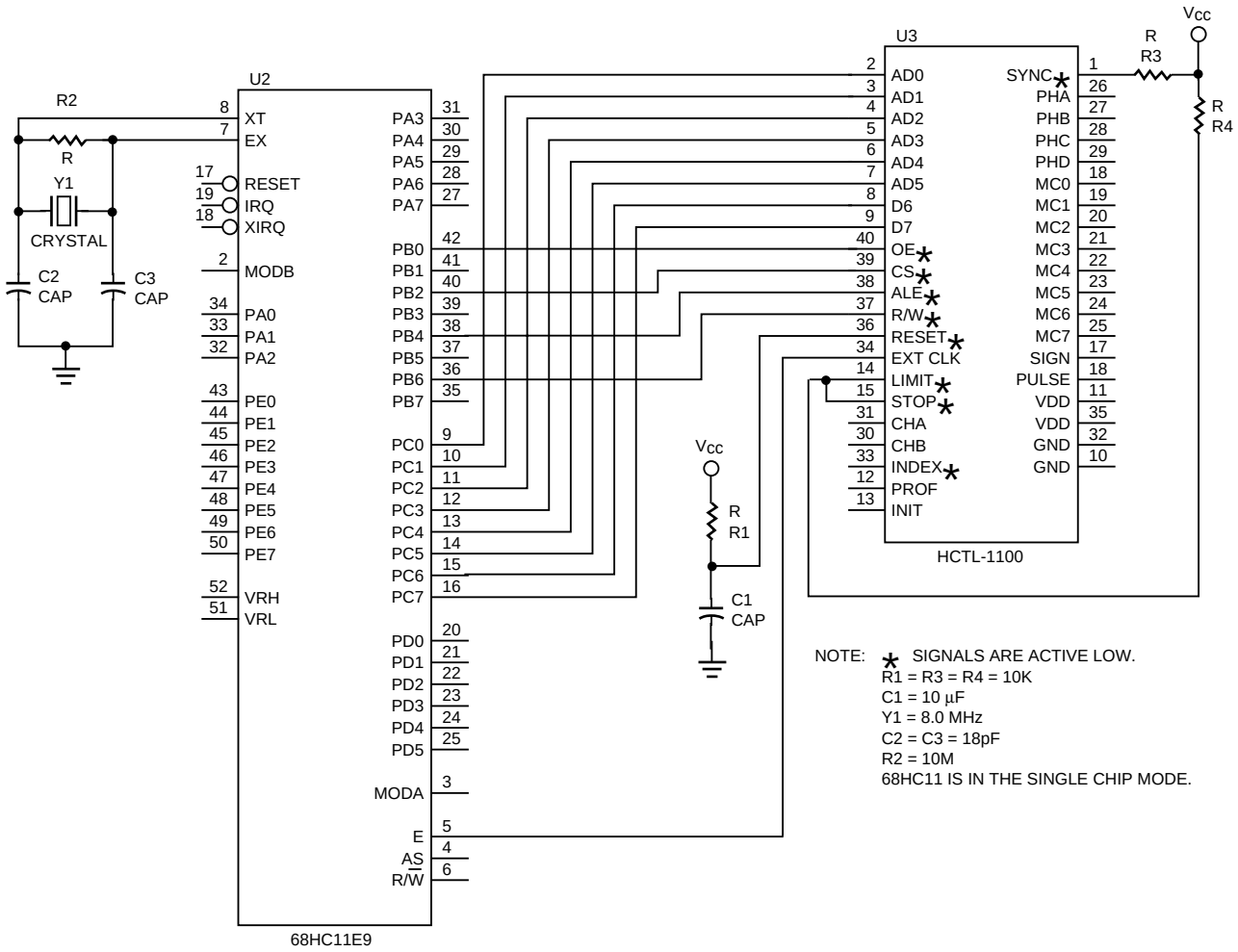

Figure 1. 68HC11 to HCTL-1100 Port Interface.

The following two subroutines to read and write to the HCTL-1100 assume that the non-overlapped mode of interfacing, as explained in the HCTL-1100 data sheet, is being used.

```
;*******************************************************************************
;THE FOLLOWING SUBROUTINE IS USED TO WRITE DATA TO THE HCTL-1100.
;THE SUBROUTINE IS CALLED WITH THE ADDRESS OF THE LOCATION TO BE
;WRITTEN TO IN REGISTER B. THE DATA TO BE WRITTEN IS IN A MEMORY
;LOCATION CALLED WRITEDTA.
;ADDRESS $1007 IS DATA DIRECTION CONTROL REGISTER FOR PORT C.
;ADDRESS $1003 IS PORT C.
;ADDRESS $1004 IS PORT B.
;*******************************************************************************

WR1100:  PSHA            ;SAVE THE ACCUMULATOR IN THE STACK.:
         LDAA#0FF
         STAA$1007       ;SET PORT C DIRECTION TO OUTPUT.
         STAB$1003       ;ADDRESS OUT.
         LDAA#0EF
         STAA$1004       ;ALE LOW
```

(Continues)

```
        LDAA#0BB
        STAA$1004       ;ALE HI, CS LO, R/W LOW
        LDAA WRITEDTA   ;DATA TO BE WRITTEN LOADED IN REGISTER A.
        STAA$1003       ;OUTPUT DATA.
        LDAA#0BF
        STAA$1004       ;CS HI.
        LDAA#0FF        ;
        STAA$1004       ;R/W HI.
        PULA            ;RETRIEVE THE VALUE OF ACCUMULATOR FROM
                        ;STACK.
        RTS


;*******************************************************************************
;THE FOLLOWING SUBROUTINE IS USED TO READ DATA FROM THE HCTL-1100.
;THE SUBROUTINE IS CALLED WITH THE ADDRESS OF THE LOCATION TO BE
;READ IN REGISTER B.
;THE SUBROUTINE RETURNS THE DATA BYTE READ IN REGISTER B.
;*******************************************************************************

RD1100: PSHA            ;SAVE THE ACCUMULATOR ON STACK.
        LDAA#0FF
        STAA$1007       ;PORT C IS SET TO OUTPUT MODE.
        STAB$1003       ;ADDRESS OUT.
        LDAA#0EF
        STAA$1004       ;ALE LO.
        LDAA#0FB
        STAA$1004       ;ALE HI, CS LO.
        LDAA#0FF
        STAA$1004       ;CS HI.
        LDAA#0FE
        STAA$1004       ;OE LO.
        LDAA#00
        STAA$1007       ;PORT C IS SET TO INPUT TO READ THE DATA.
        LDAB$1003       ;READ THE DATA INTO REGISTER B.
        LDAA#0FF
        STAA$1004       ;OE HI.
        PULA            ;RETRIEVE THE VALUE OF THE ACCUMULATOR A
                        ;FROM THE STACK
        RTS
```

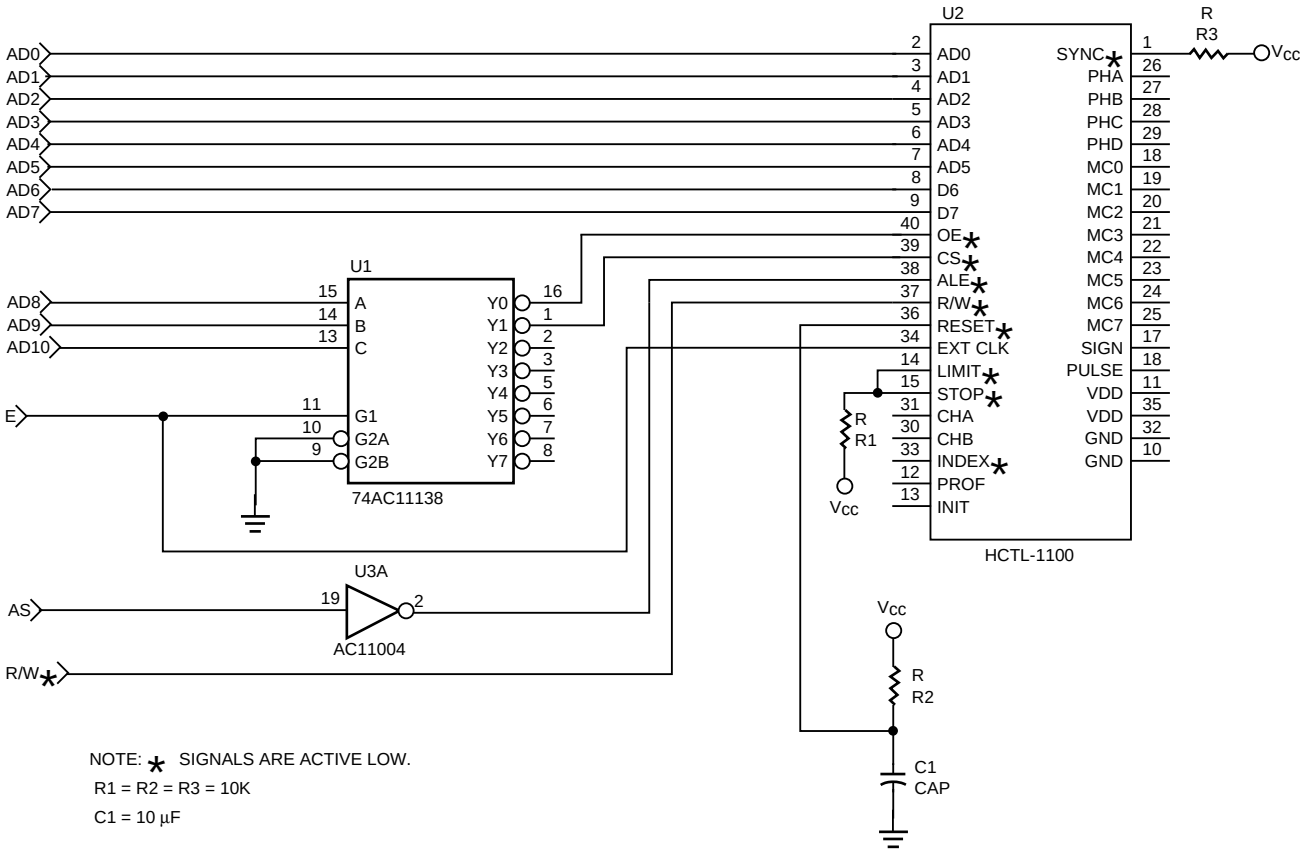

Figure 2. 68HC11 to HCTL-1100 Bus Interface.

Bus Interfacing

Connections:

E clock of the 68HC11 is connected to the HCTL-1100 EXT CLK.

AS of the 68HC11 is inverted and connected to the ALE signal of the HCTL-1100.

R/W of the 68HC11 is connected to the R/W of the HCTL-1100.

The rest of the connections are shown in the schematic diagram in Figure 2, “68HC11 to HCTL-1100 Bus Interface”.

Note that all signals on this schematic with a “*” sign are active low signals.

For the bus interface, a 3-to-8 decoder 74AC11138 and an inverter 74AC11004 are needed. With these two chips, four HCTL-1100 ICs can be interfaced to the 68HC11 bus. The “68HC11 to HCTL-1100 Bus Interface” schematic shows how connections to one of the four HCTL-1100s can be made. The CS and OE signals of the other three HCTL-1100s can be connected to the outputs of the 74AC11138 in a similar manner to the connections made to the HCTL-1100 shown in the diagram.

The following two subroutines are used to write and read while using the 68HC11 bus to interface to the HCTL-1100.

Please note that all four routines assume that the clock frequency into the HCTL-1100 is equal to 2 MHz. If the HCTL-1100 clock frequency is less than 2 MHz, and the processor clock is at 2 MHz, NOPs may be inserted where it is required to produce more delay in the read routine as shown, to satisfy timing requirements given in the data sheet.

```
;*******************************************************************************
;THIS SUBROUTINE IS USED TO WRITE DATA TO THE HCTL-1100 FOR THE
;BUS INTERFACE.
;THE DATA TO BE WRITTEN IS IN MEMORY LOCATION CALLED WRITEDTA
;REGISTER B CONTAINS THE ADDRESS OF THE LOCATION TO BE WRITTEN.
;*******************************************************************************

              OE0   EQU   $0F000   ;ADDRESS HI BYTE FOR OE* SIGNAL.
              CS0   EQU   $0F100   ;ADDRESS HI BYTE FOR CS* SIGNAL.

WRITE1100:    PSHA                 ;SAVE THE ACCUMULATOR
              LDX#CS0              ;HI BYTE ADDRESS IN INDEX REGISTER.
              ABX                  ;ADD THE ADDRESS OF LOCATION TO BE
                                   ;WRITTEN TO FORM COMPLETE ADDRESS.

              LDAA WRITEDTA        ;LOAD THE DATA TO WRITE IN THE
                                   ;ACCUMULATOR.

              STAA 0,X             ;WRITE THE VALUE TO THE HCTL-1100
              PULA
              RTS

;*******************************************************************************
;THIS SUBROUTINE IS USED TO READ DATA FROM THE HCTL-1100 FOR THE
;BUS INTERFACE.
;THE ADDRESS OF THE LOCATION TO BE READ IS IN REGISTER B.
;THE DATA READ IS RETURNED IN REGISTER B.
;*******************************************************************************

RD1100:       PSHA
              LDX#CS0              ;HI BYTE OF ADDRESS WHICH PULSES CS*
                                   ;IN INDEX REGISTER
              ABX                  ;ADD REGISTER B TO FORM COMPLETE
                                   ;ADDRESS.
              LDAA 0,X             ;LATCH THE ADDRESS IN HCTL-1100, BY
                                   ;PERFORMING A DUMMY READ.
              ;NOP
              ;NOP                 ;IF NEEDED.(SEE EXPLANATION ABOVE.)
                                   ;NOT NEEDED IF HCTL-1100 HAS 2 MHz
                                   ;CLOCK.

              LDX#OE0              ;LOAD THE HIGH BYTE OF THE ADDRESS
                                   ;WHICH PULSES OE* IN INDEX REGISTER.

              LDAB 0,X             ;READ THE HCTL-1100. DATA IN REGISTER B.
              PULA
              RTS
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