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# A Simple Interface for the HCTL-2020 with a 16-bit DAC without using a processor

## Application Brief M-020

### Introduction

In certain applications it becomes necessary to interface the HCTL-2020 to a DAC (Digital Analog Converter) without having to use a processor or micro controller. A typical block diagram is shown in Figure 1.

A simple circuit with easily available components can be used. The *Analog Devices* AD 569 16-bit DAC is shown. It has an 8-bit interface and signals to control the loading of the high and low bytes from the HCTL-2020 called HBE (High Byte Enable) and LBE (Low Byte Enable) respectively. These signals are active LO signals. The LDAC signal on the AD 569 can be connected to ground or tied to LBE. The CS signal is tied to ground. Please refer to the data sheets for the DAC AD 569 for detailed timing diagrams. The different operations needed to achieve the interface can be described as shown in Table 1.

**Table 1.**

| SEL | $\overline{OE}$ | $\overline{HEB}$ | $\overline{LBE}$ | Remarks |
|---|---|---|---|---|
| LO | LO | LO | HI | ;enable the HI byte from HCTL-2020,<br>;load the byte into the DAC with the<br>;HBE signal. |
| LO | LO | HI | HI | ;complete the loading process. |
| HI | LO | HI | LO | ;enable the LO byte from the HCTL-<br>;2020, load the byte into the DAC<br>;with the LBE signal. |
| HI | LO | HI | HI | ;complete the loading process. |
| HI | HI | HI | HI | ;pull OE high to complete inhibit<br>;reset of HCTL-2020. |
| HI | HI | HI | HI | ; |
| HI | HI | HI | HI | ; |
| HI | HI | HI | HI | ;The above three sets of states have<br>;been added to get a total of 8 states. |

The last three states in Table 1 simplify the design. They can be arbitrarily selected. For example, they can be used to reset the inhibit in the HCTL-2020 by dummy read. In order to simplify the design they have been chosen to be HI here. Note that LO on all cannot be used as it corresponds to enabling the HCTL-2020 and the AD 569. After this last state the circuit is made to start from the beginning and therefore repeat the read to the HCTL-2020, write to the DAC cycle.

Note: If you are using a 16-bit DAC with no 8-bit interface, but only a 16-bit interface, consider using the signals HBE and LBE to enable external latches connected to the HI and LO bytes of the DAC respectively as shown in Figure 1.

The design consists of dividing the main clock by 2, 4 and 8 using a 74LS193 counter, and combining the 8-states to give the sequence of steps described above for each signal. The diagrams shown in “Sequencer and Control Signals Timing Diagram” and

"Truth Table" are descriptive of the process. The SEL signal can be realized with an OR gate. In a similar manner the other signals can be constructed also. A logic gate diagram of the sequencer and control signals is shown in Figure 2.

The maximum rate at which the DAC is updated with a new count is equal to the main clock rate into the HCTL-2020 divided by 8.

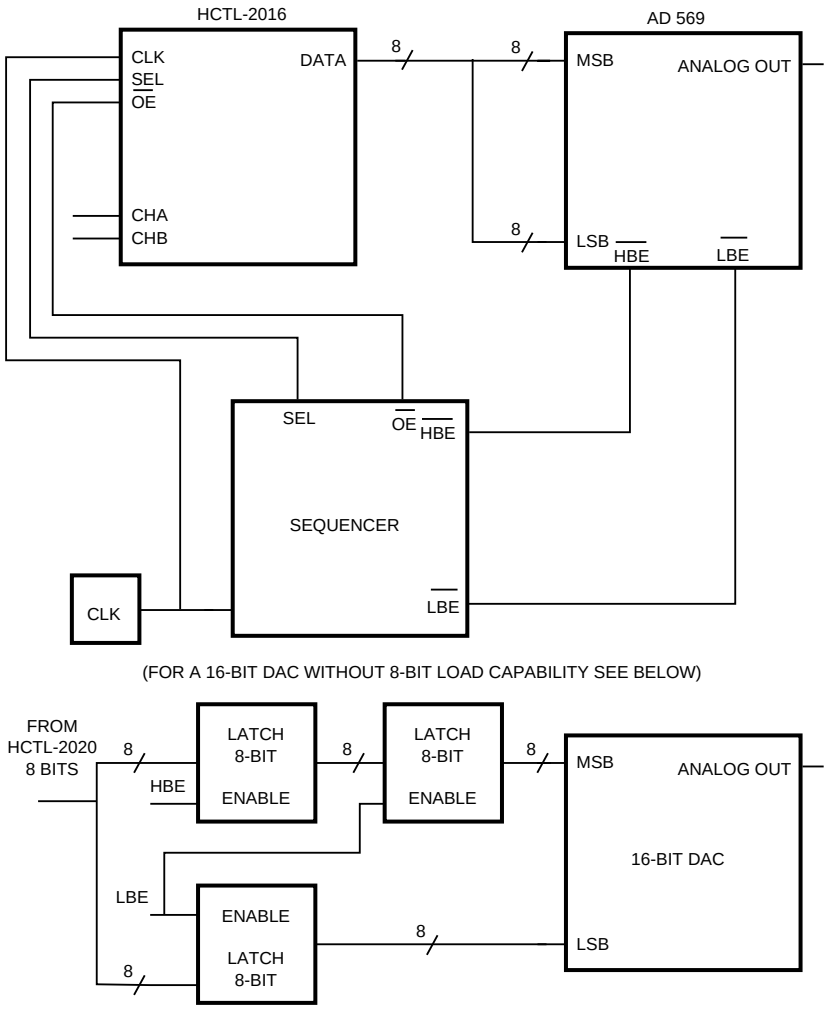
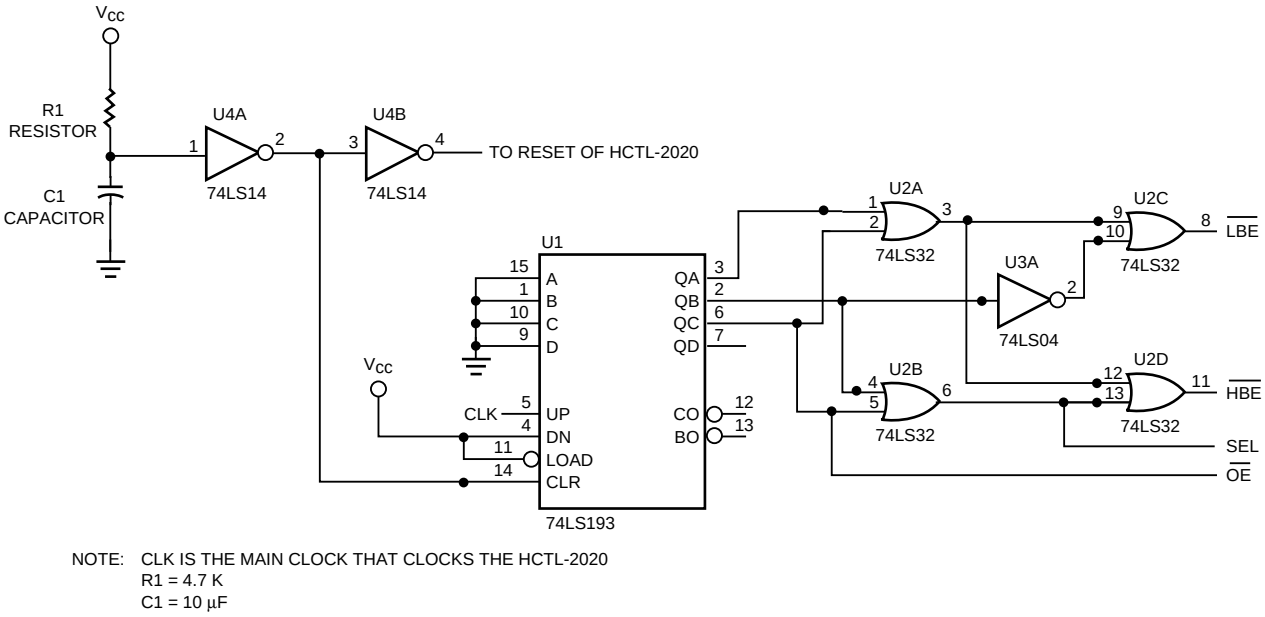



**Figure 1. Interfacing the HCTL-2020 with the 16-bit DAC AD 569.**

## Truth Table

| M3 | M2 | M1 | SEL | $\overline{OE}$ | $\overline{HBE}$ | $\overline{LBE}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: M1 = CLK/2
M2 = CLK/4
M3 = CLK/8




NOTE: CLK IS THE MAIN CLOCK THAT CLOCKS THE HCTL-2020
R1 = 4.7 K
C1 = 10 μF

**Figure 2. Sequencer and Control Signals Logic Diagram.**

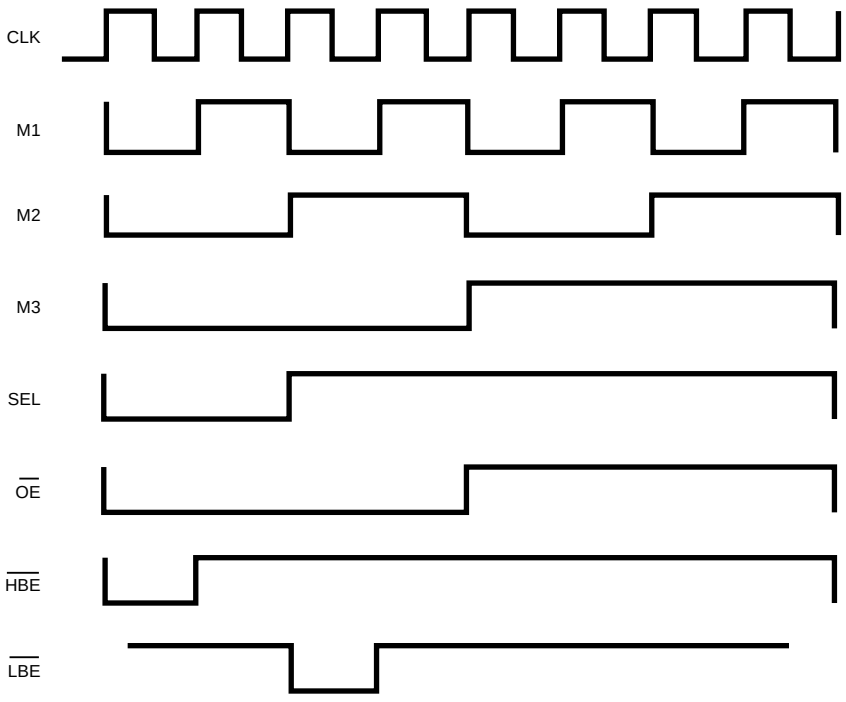



**Figure 3. Sequencer and Control Signals Timing Diagram.**

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