Agilent Technologies
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# Answers to Commonly Asked Questions About the HCTL-2020

## Application Brief M-019

### Question 1.

**What is the maximum frequency on any one channel (A or B) of pulses that will be counted by the HCTL-2020?**

Answer: 2.3 MHz.
The maximum frequency of the clock that can be used is 14 MHz. Each input qualified by the chip input filter is considered to be a valid level if it remains for at least three consecutive rising edges (3/14 microseconds). Therefore, for two valid levels (one cycle of the input) the minimum time should be 6/14 microseconds. The maximum frequency is 14/6 MHz. This maximum frequency will be reduced slightly in order to take into account the finite rise times, assymetry of the waveforms, and noise.

### Question 2.

**Is it possible to hold the SEL line LO and read the HI byte (a flow-through of the HI byte) like it is possible to hold the SEL line HI and read the LO byte (a flow-through of the LO byte)?**

Answer: No.
With a negative clock edge the internal latch is inhibited and stops being updated. The HI byte value is not updated for subsequent reads.

### Question 3.

**If SEL and OE are LO but there is no negative clock edge during this time, does it mean that the inhibit will not be set?**

Answer: No.
Internal to the chip SEL and OE being LO at the same time leads to an inhibit condition being satisfied. With the next negative clock edge the internal latch is inhibited from counting. In order to reset the inhibit two conditions should be satisfied in sequence:

1) a negative clock edge should see SEL being HI and OE being LO.

2) a negative clock edge should see the OE at HI. (SEL is a don't care for this.)

Note that a total of three clock edges – one to set the inhibit, one to start the reset, and one to complete the reset of the inhibit, is needed for the whole process.

### Question 4.

**Can the index pulse from a three channel encoder be used to reset the latch in the HCTL-2020?**

Answer: Yes.
Agilent three channel encoders give a HI level index pulse every revolution of the code wheel and this index pulse occurs when both channel A and B are LO for a quarter period of a cycle. If this index pulse is inverted and connected to the reset (Pin 7 on HCTL-2020) it will reset the internal latch to zero as long as this signal is LO for 28 ns. Note that a reset also resets the inhibit.

### Question 5.

**Can the chip be reset at the end of every read?**

Answer: Yes.
Since the chip was not designed with this purpose in mind, some timing constraints for doing this follow. It is assumed that the chip is being read at a negative going clock edge as explained in the data sheets. The chip can be reset if a delay can be introduced after the negative going clock edge at which the chip is read such that the data that is being read is stable in the internal latch (in

other words, it is not being reset to zero by the time it is read) and then a LO signal (duration = 28 ns and occuring before the next rising clock edge after the read) is input to the reset pin. It is necessary that the reset signal occur before the next rising clock edge after the read; otherwise a new count that could be coming in with the rising edge will be lost.

## Question 6.

**What is the quadrature relationship needed between signals on channel A and channel B?**

Answer: At least one positive clock edge between any two valid quadrature states, which will be ensured if there is at least one clock period between two successive quadrature states. A good design will take into account the finite rise times of signals.

## Question 7.

**Is the up/down signal a level? HI when counting up and LO when counting down?**

Answer: No.
The signal is at the correct level one positive clock edge before a count and stays at the correct level until the next rising edge after the count. Therefore, if there are quadrature counts every four positive edges (which is the fastest possible rate), then the signal stays at the correct level at all times. At all other times the level on the signal is not defined. Therefore, to use the signal, combine it with the $CNT_{DCDR}$ signal.



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