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Interfacing the HCTL-20XX to the Intel 8051

Application Brief M-017

Introduction

The HCTL-2000, 2016, and 2020 are CMOS ICs that provide a noise filter, quadrature decoder, counter, and bus interface on a single chip. This family of ICs is designed to improve system performance by removing the burden of quadrature decoding from the processor. The HCTL-2000 has a 12-bit counter and the HCTL-2016 and HCTL-2020 have 16-bit counters.

This application brief discusses what is required to interface the HCTL-20XX family to an Intel 8051 microcontroller bus. The hardware interface is shown in Figure 2. The address decoder in this circuit consists of a single 8-input NAND gate which is used to decode the base address of 0FEXXH. This address is purely arbitrary and the user could substitute their own address decoder circuitry to select any arbitrary address in the 8051's external address space. The SEL line can also be connected to any arbitrary address line.

The decoded address signal is ANDed together with the processor RD signal to form the HCTL-20XX OE signal. When this signal is active the HCTL-20XX places the selected count byte on the data bus. The timing for these signals is shown in Figure 1.

The HCTL-20XX has internal inhibit logic circuitry and latches to guarantee that the 16 bit count is held stable while both 8-bit halves of this count are read by the processor. For proper operation of this circuitry the processor should read the high byte first (SEL=0) and then the low byte (sel=1). This sequence can be seen in the code listings provided with this application brief.

The interfaces for the HCTL-2000, 2016, and 2020 are identical. The HCTL-2020 also provides additional signal for cascading external counters. This is helpful for designs which require more than a 16-bit counter. For more information on these ICs please see the HCTL-20XX data sheet.

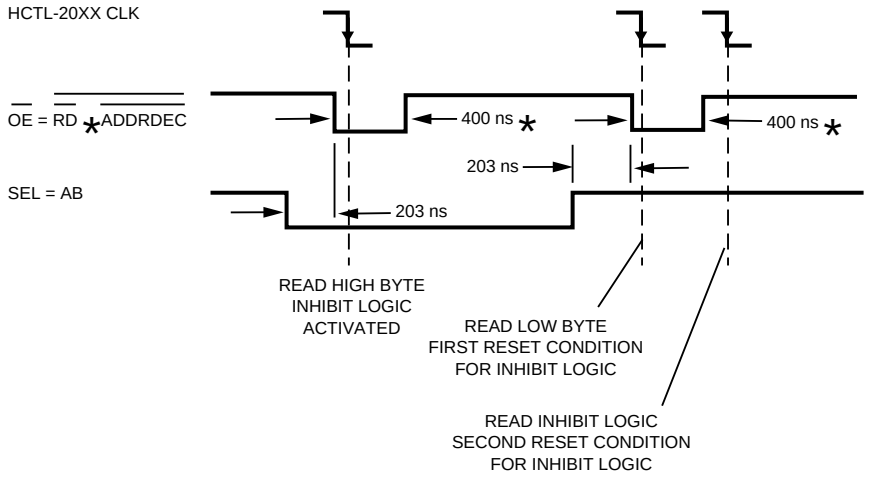

Figure 1. HCTL-20XX/8051 Read Cycle Timing

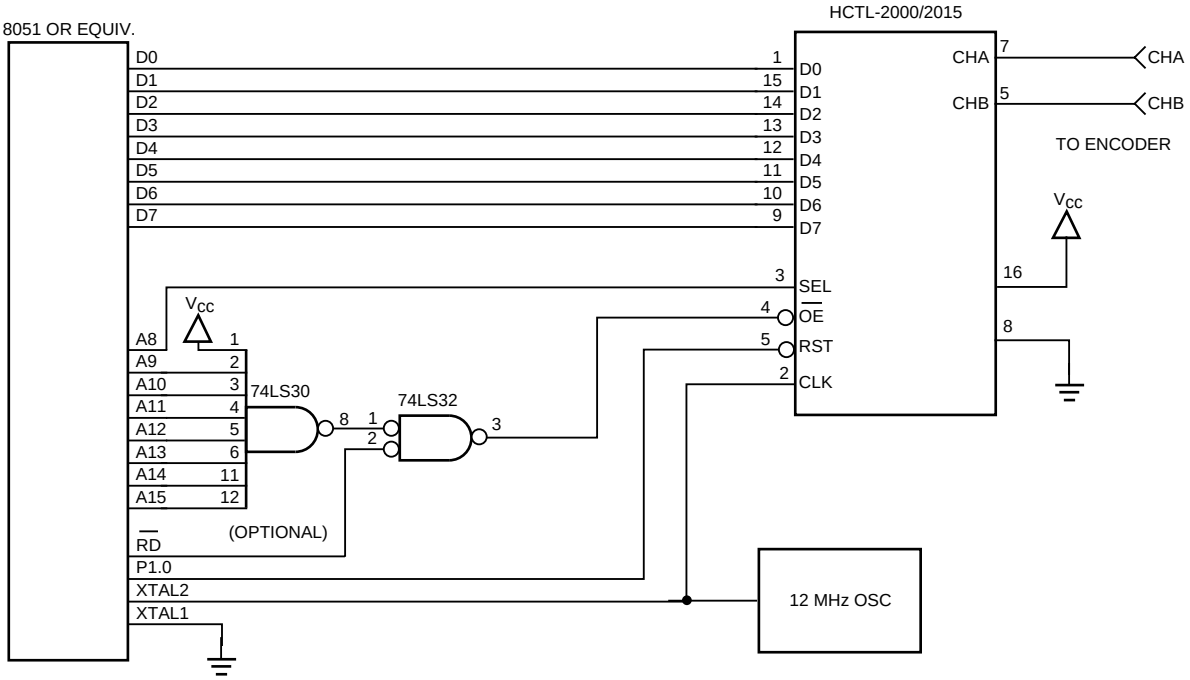

Figure 2. 8051/HCTL-2000 Bus Interface

```
;*****************************************************************************
;HCTL-20XX INTERFACE ROUTINES
;THIS SOFTWARE ASSUMES THE FOLLOWING:
;
;1)  THE HCTL-20XX BASE ADDRESS IS 0FE00H
;2)  THE SEL LINE IS CONNECTED TO A8
:3)  THE RESET LINE IS CONNECTED TO P1.0
;*****************************************************************************


;*****************************************************************************
;HCTL-2000 EQUATES
;*****************************************************************************

; INTERNAL MEMORY ALLOCATION
COUNTH   EQU     030H            ; POSITION COUNT - HIGH BYTE
COUNTL   EQU     031H            ; POSITION COUNT - LOW BYTE

; HCTL-2000 I/O ADDRESSES
H2000H   EQU     0FF00H          ; HCTL-2000 PORT ADDRESS - HIGH BYTE
H2000L   EQU     0FE00H          ; HCTL-2000 PORT ADDRESS - LOW BYTE



;*****************************************************************************
;SUBROUTINE RD2000
;THIS SUBROUTINE READS THE 16 BIT COUNT VALUE FROM THE
;HCTL-2000 AND STORES IT IN INTERNAL MEMORY LOCATIONS
;COUNTH AND COUNTL.
;*****************************************************************************

RD2000:  MOV     DPTR,#H2000H  ; SELECT HIGH BYTE OF HCTL-2000
         MOVX    A,@DPTR
         MOV     COUNTH,A      ; STORE IN INTERNAL RAM
         MOV     DPTR,#H2000L  ; SELECT LOW BYTE OF HCTL-2000
         MOVX    A,@DPTR
         MOV     COUNTL,A      ; STORE IN INTERNAL RAM
         RET



;*****************************************************************************
;SUBROUTINE RS2000
;THIS SUBROUTINE RESETS THE HCTL-2000
;THIS SUBROUTINE ASSUMES THAT THE HCTL-2000 RESET LINE IS ;CON-
NECTED TO P1.0 ON THE 8051
;*****************************************************************************

RS2000:  CLR     P1.0            ; BRING HCTL-2000 RESET LINE LOW
         SETB    P1.0            ; BRING HCTL-2000 RESET LINE HIGH
         RET
```

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