DDR4 TdiVW/VdiVW Bit Error Rate Measurements or Understanding Bit Error Rate Measurements in DDR

Application Note

Historically, DDR (double data rate) has defined its timing specifications with a belief of a zero bit error rate (BER). While a zero bit error rate is statistically not possible, timing budgets had enough margin to justify the method of specification and measurement. With each generation of DDR Synchronous Dynamic Random Access Memory (SDRAM), speeds increase, package sizes decrease, and power consumption decreases. (See Table 1). Added challenges come with these improvements of decreased design margins, signal integrity, and interoperability. Latest DDR technology offers data rates of 3.2Gb/s or higher. Each picosecond now matters and can be the difference in passing and failing bits. At these high data rates, BER measurements are important in order to understand the true reliability of a system. Noise and jitter affect the signal integrity and its overall reliability. Measuring and understanding the components of noise and jitter can enable designers to minimize them on the overall system design to ensure valid and accurate data transfer. In this paper, we are going to take a look at the measurements of the timing data input valid window (TdiVW) and the voltage data input valid window (VidVW).

Table 1. DDR technologies and key JEDEC specifications

DDR standard	DDR	LPDDR or mobile-DDR	DDR2	LPDDR2 or mobile-DDR2	DDR3	LPDDR3 or mobile-DDR3	DDR4
Specification	JESD79E	JESD209	JESD79-2E, JESD208	JESD209-2B	JESD79-3C	JESD209-3	JESD79-4
Operating voltage	1.5 - 3.3 V	1.8 V	1.8 V	1.6 B	1.5 V	1.2 V	1.2 V
Clock frequency	100 - 200 MHz	100 - 200 MHz	200 - 400 MHz	100 - 533 MHz	400 - 800 MHz	667 - 800 MHz	800 - 1600 MHz
Data transfer rate	200 - 400 MT/s	200 - 400 MT/s	400 - 800 MT/s	200 - 1066 MT/s	800 - 1600 MT/s	1333 - 1600 MT/s	1600 - 3200 MT/s
Package type	This Small Outline Package (TSOP)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)	Fin Ball-Grid Array (FBGA)/ POP	Fine Ball-Grid Array (FBGA)	POP	Fine Ball-Grid Array (FBGA)
Package size	x4, x8, x16, x32	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16	x16, x32	x4, x8, x16
Backward compatibility	No	Yes, with DDR	No	Yes, with DDR2	No	No	No

Impact of Noise and Jitter on Data Transfer

Sources of jitter in a system include inter-symbol interference (ISI), cross talk, and duty cycle distortion (DCD) and can limit the performance and the interface between the memory controller and the DRAM.

Jitter is defined as the deviation of a signal transition from its ideal time. As data rates increase, timing budgets decrease and each pico second of margin gained becomes more important. A small amount of jitter can easily close the data valid window of the read or write data at high speed data rates. This will ultimately increase bit error rate and data sampling error.

When operating at a high date rate, the data valid window is very small. The noise in the system or crosstalk from adjacent electrical signals, or even electro-magnetic interference could easily distort the signal integrity which could result in data sampling error. Real-time eye diagram provide eye height and eye width measurements for signal integrity checks and estimates the data valid window. However, simply measuring a data eye with real time eye diagram measurement does not give full insight into the data valid window and expectations of a bit failure rate. Figure 1 shows a write data eye with over 100,000 unit intervals (UI) measured. This initial measurement of over 100,000 UI would result in a measured TdiVW of 353.75ps (or a margin of 56.25ps to the defined mask) and a VdiVW of 377mv (or a margin of 71.1mv). Figure 2 shows how the (deterministic jitter (DJ)) and (random jitter (RJ)) lines show the impact of jitter over a long period of time and the actual data valid input window after 1 trillion UI (a 1e-12 bit error rate or BER). Deterministic jitter is generally bound and predictable and can be correlated to the data stream; such as inter symbol interference and duty cycle distortion. Random jitter is generally Gaussian and is unbounded. As with any Gaussian distribution, as a population increases, so does the peak-to-peak value of the distribution. Therefore, total jitter is DJ plus a BER multiplier of RJ. Note that the data valid input window is made on write data. You can see how important it is to make BER measurement calculations to form a statistical measurement of total jitter in order to understand the design's data valid window result and to properly understand at what rate you can expect an error within the design. Additionally, understanding the components and sources of jitter can enable designers to reduce jitter in their designs and ensure better data performance.

Figure1. Direct Measurement with 100,000 UI

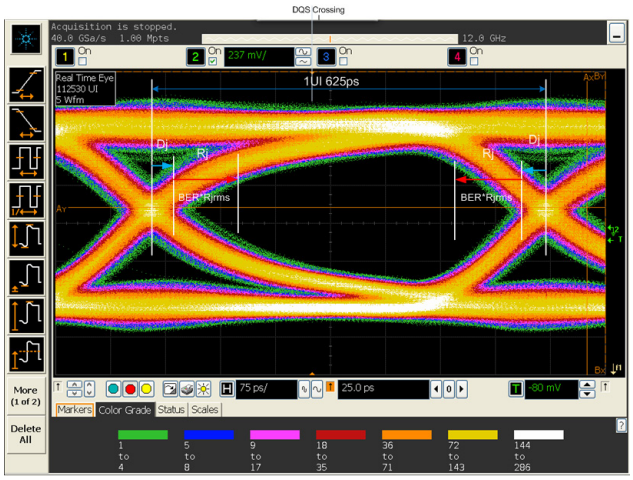

Figure2. Dj and Rj impact on the data eye

Making a Data Jitter Measurement

The data valid input window is the window of valid write data to the respective clock edge. The time interval error (TIE) is measured for each data edge in relation to the clock edge. Two TIE trends can be measured; one for data transitions before clock and another for data transitions after clock to calculate TdiVW. Once a TIE trend of data is established, jitter decomposition of deterministic jitter and random jitter can be determined. A total jitter for data on each side of DQS can be calculated, and a TdiVW is determined for a desired bit error rate.

Figure 3 shows the same eye diagram from Figure 1 now with contour points at a BER of 1e-12 (or 1 trillion data transitions). Directly, measuring 1 trillion data transitions-, would be extremely time consuming. By extrapolating different BERs, we can begin to understand the failure rate to the mask that is expected. At 1e-12, the TdiVW measurement is 173ps (with a margin to the defined mask of only 5ps). The VdiVW measurement is 259mv (with a margin of 27mV to the defined mask). This is a significant difference to the initial measurement for TdiVW and VdiVW. At a BER of 1E-12, there is little margin to the mask, but we can say that we can expect better than a 1e-12 failure rate (or 1 in 1 trillion). Figure 4 shows the contour of 1e-15 which fails the mask. We know that we can expect bit failures to this mask within 1 quadrillion data transitions.

While there is no specific data valid window specification for read data, it is just as important to understand the read data being presented to the controller from the memory device. Measurements can be made in the same manner for read data so that memory controller designers can understand the impact of jitter and noise on the data being sent from the memory to the memory controller and create design expectations to develop a robust memory controller.

Figure 3. Data Eye with 1E-12 BER

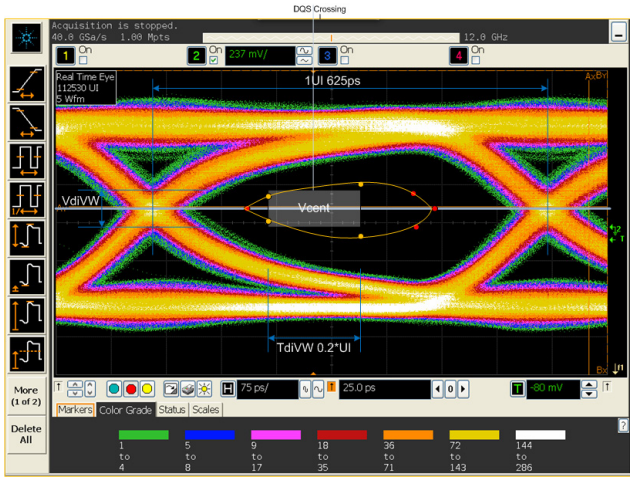

Figure 4. Data Eye with 1E-15 BER

Summary

As memory technology reaches higher data rates, the signal amplitude and data valid window becomes very small, resulting in increased data sampling error. It is clear that simply making a measurement of an undefined quantity, may falsely indicate great margin. Measuring jitter and noise to compute statistical measurements of data valid windows helps you to quantify the bit error rate of your system. Understanding and making these measurements is important in developing high quality designs.

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