Agilent 81150A and 81160A Arbitrary Bit-Shape Pattern Generator

Application Note

- Ideal and distorted pattern
- Stress test with PRBS up to 2^{31}
- Two, three or four level signals allowing support for serial protocols that require electrical idle signaling
- Definition of customized bit shapes
- Up to 16 Mbit for complex patterns
- Arbitrary bit shaping to emulate real world signals including over- and undershoot, ringing or distorted level transitions

Agilent Technologies

Get ready for the new challenges

No matter which segment of the electronic market you are looking at, the demand for higher speed and higher bandwidth data transmission continues. The necessity to achieve this at low cost and the continued trend to miniaturization drive the device design to its limits: a growing number of channels at Gigabit speeds on one printed circuit board also means a growing influence of disturbing side effects which threaten signal integrity. Jitter, noise, reflections and cross-talk can distort a high speed signal in a way that spikes are misinterpreted as a clock signal and the true clock is obscured.

Therefore it becomes crucial to know the behavior of your device under stress in order to be able to guarantee the reliability of your system. Designers need to strain the components with well-defined and reproducible real-world signals to test and optimize their robustness.

Usually, these distorted signals are created with a two-channel pulse generator. On the first channel, the ideal signal is set up by defining pulse width, delay, rising and falling edges and amplitude.The second channel is used for the distortion, such as overshoot or undershoot, that will be added to the clean signal. In Figure 1 this is a positive or negative spike.
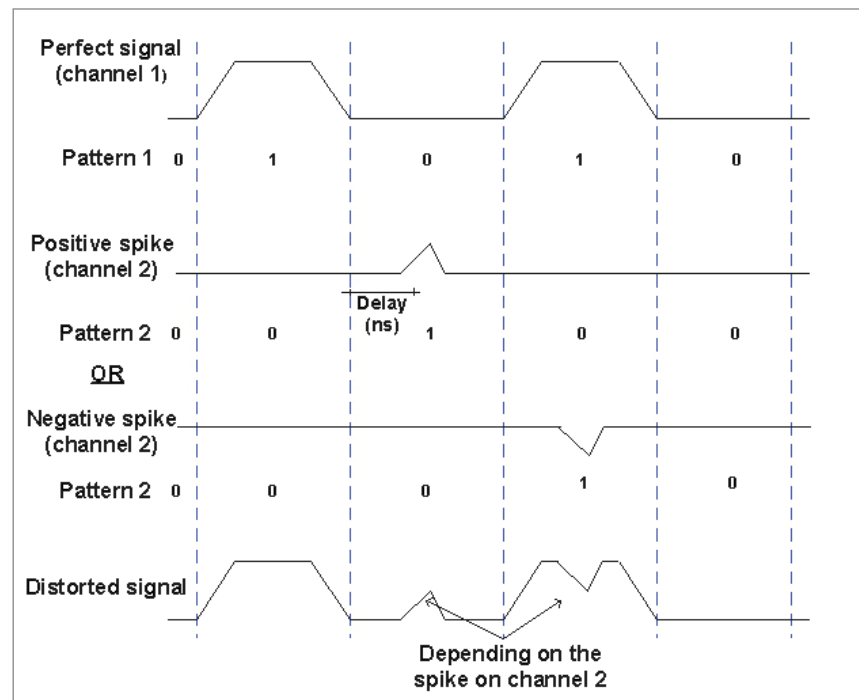

Figure 1. Distorted signal created with a two-channel pulse generator

For a real-world signal with common mode noise, an additional function generator is needed that adds AM (amplitude modulation) to the data sequence. A power divider is included into both signal lines to add the modulation signal. The setup as seen in Figure 2 starts to become complex, even more so because you have to take care that the electrical length of both data lines, between generator output and receiver output, are the same.
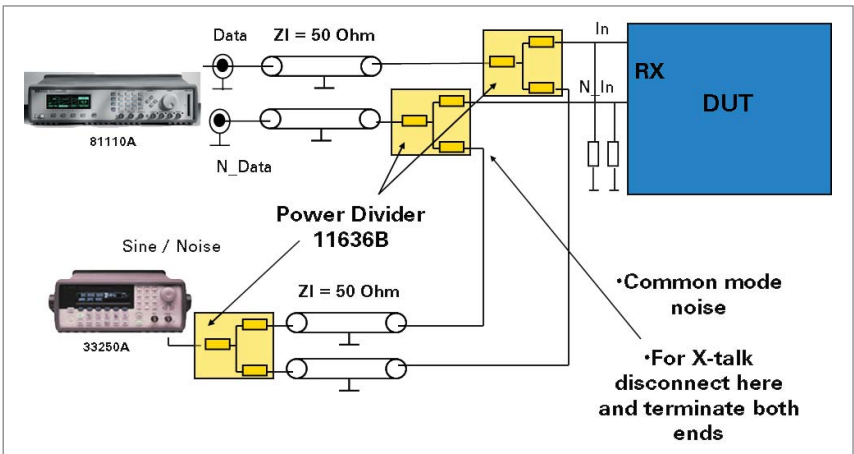
Figure 2. Traditional setup for real-world signal tests

It may be easier to create a distorted signal using an arbitrary waveform generator but as a question of cost this may often not be an alternative.

The 81150A and 81160A Pulse Function Arbitrary Noise Generators offer a solution to this dilemma; in a moderate price segment, they are able to create arbitrary signals with length up to 8 kbits (for the 81150A) and up to 4 kbits for the 81160A.

With the optional arbitrary bit-shape pattern generator it is now possible to create distorted digital data streams even longer, by a factor of thousand. Hence, the 81150A and 81160A pattern generators are a convenient alternative to complex stress test setups or costly high-end arbitrary waveform generators.

Maximizing the waveform length with the unique arbitrary bit-shape pattern generator

Using a completely different concept for waveform creation, the optional arbitrary bit-shape pattern generator renders possible distorted signals of up to 16 Mbit length.

For the 81150A and 81160A arbitrary signals, every single point of the signal needs to be specified. The pattern generator however, only needs the definition of a bit sequence together with the definition of all possible bit value transitions. Built that way, the signal takes up less storage place, which in turn allows longer arbitrary waveforms – 16 Mbit for the 81150A, 4 Mbit for the one-channel 81160A and 2 Mbit per channel for the two-channel 81160A.
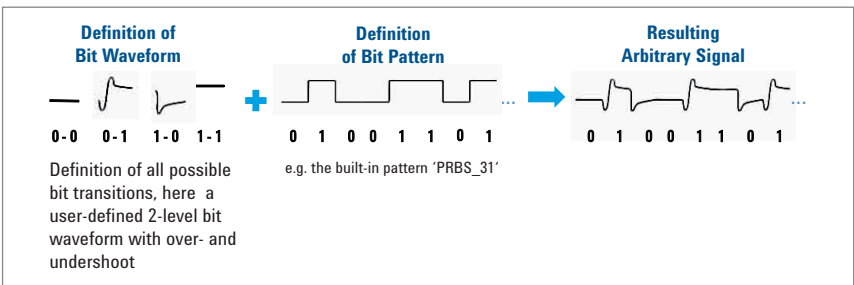

Figure 3. Waveform creation concept of the 81150A and 81160A pattern generators

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Pattern source

The bit pattern can be generated internally either from an algorithm or from memory. Alternatively, it is possible to provide an externally generated data stream at the MOD-IN input for re-shaping by the 81150A and 81160A.
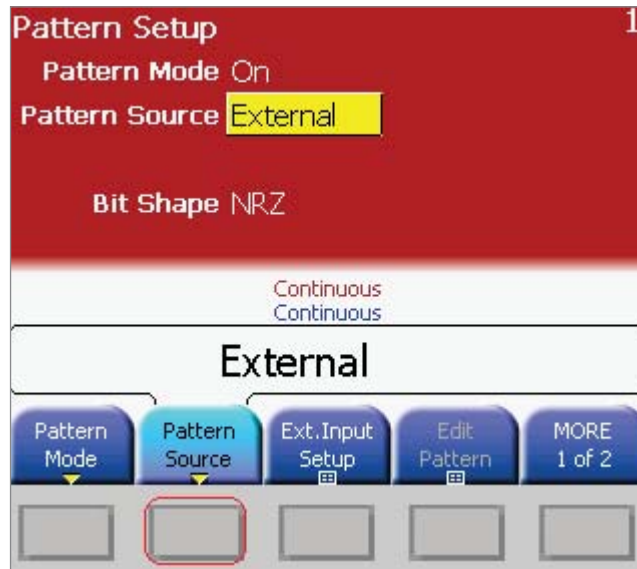
External pattern source

Figure 4. External pattern source

External bit patterns are provided at the MOD-IN connector at the rear-panel. In external or 'pass-through' pattern mode, the 81150A and the 81160A can be used to retime, reshape and output a data stream according to the configured data rate, output levels, number of levels and formatting settings, like any internally generated pattern.
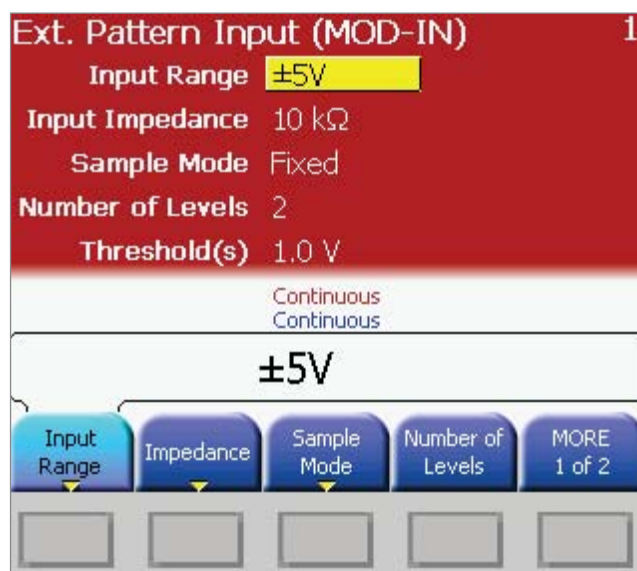

Figure 5. External input setup

The **Input Voltage Range** defines the full scale of the pattern signal. It can be selected between ± 2.5 V and ± 5 V for the 81150A. It is ± 2.5 V fixed for the 81160A.

The **Impedance** of the Modulation-In connector can be selected between 50 Ω and 10 kΩ.

The **Sample Mode** defines how the 81150A or the 81160A samples the externally provided data stream. In **Fixed Sampling Mode**, there is a fixed relation between the sampling time and the rising edge of the TRIGGER-OUT signal. In **Automatic Sampling Mode**, the instrument searches for an initial transition and then samples at the configured data rate. Transition search restarts after a certain time of inactivity at the input.

The **Number of Levels** that have to be detected in the provided external pattern signal can be set to 2 or 3.

The **Lower Threshold Voltage** defines the voltage level below which a sample is considered as logical '0'. If the voltage at MOD-IN is equal to or less than the lower threshold voltage, the externally provided bit is considered to be '0'. In case of 2-level signals, a voltage level above the lower threshold is considered to be logical '1'.
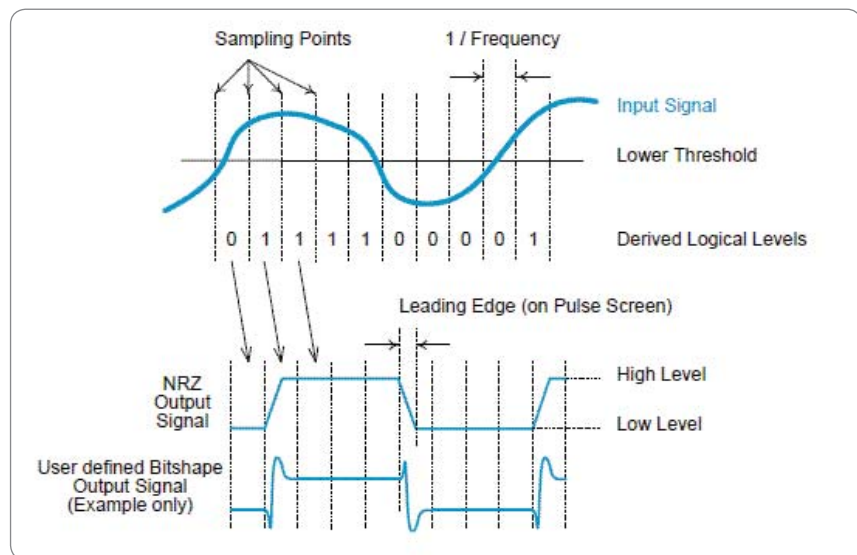

Figure 6. Lower threshold

The **Upper Threshold Voltage** can be defined only for 3-level signals. It specifies the voltage level at which a sample is considered to be logical '1'. If the voltage at MOD-IN is above the upper threshold voltage, the externally provided bit is considered to be '1'. If the voltage is above the lower threshold but less than or equal to the upper threshold, the bit is considered to be an idle symbol (and will result in the programmed offset voltage at the output).
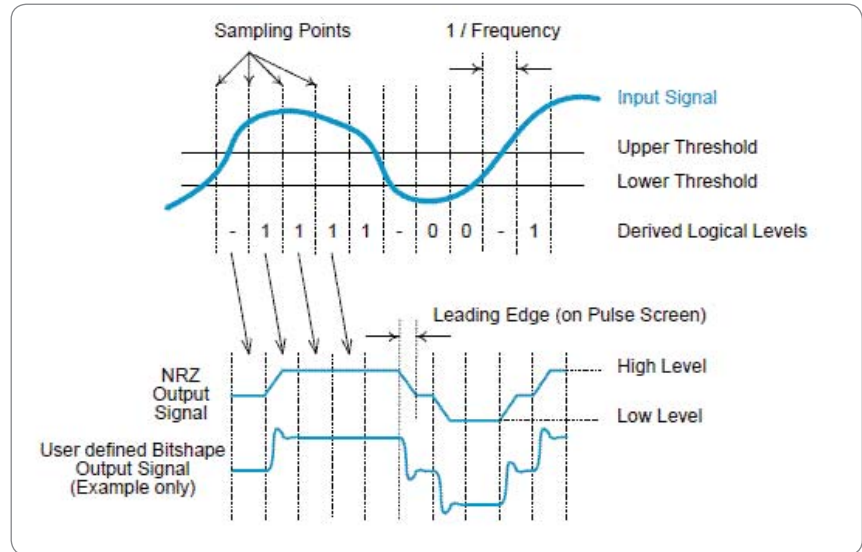

Figure 7. Upper threshold

Internal pattern source

The 81150A and 81160A Pattern Generators provide 6 different built-in bit patterns and can store up to 4 user-defined patterns. The volatile memory can also be used for storage of one additional user-defined pattern.

Built-in patterns

The built-in patterns are 2-level pseudorandom binary sequences that cannot be altered.

Built-in patterns
PRBS-7
PRBS-9
PRBS-11
PRBS-15
PRBS-23
PRBS-31

User-defined patterns

Figure 8. Create new pattern screen

User-defined patterns are created using the following parameter settings:

The **Number of Bits** specifies the initial number of bits, which can later be modified.

The **Number of Levels** can be set to 2, 3 or 4.

Default Value defines the default bit value that is used to fill the pattern during creation. Depending on the number of levels, the possible values are 0 and 1 for 2-level patterns, 0, 1 and idle for 3-level patterns and 0,1,2,3 for 4-level patterns.

If the **Auto Update** is turned on, changes of the pattern will be applied to the output immediately. This slows the editor. When it is turned off, the editor is faster because pattern changes are only applied to the output after the editing is finished.

Pattern Editor

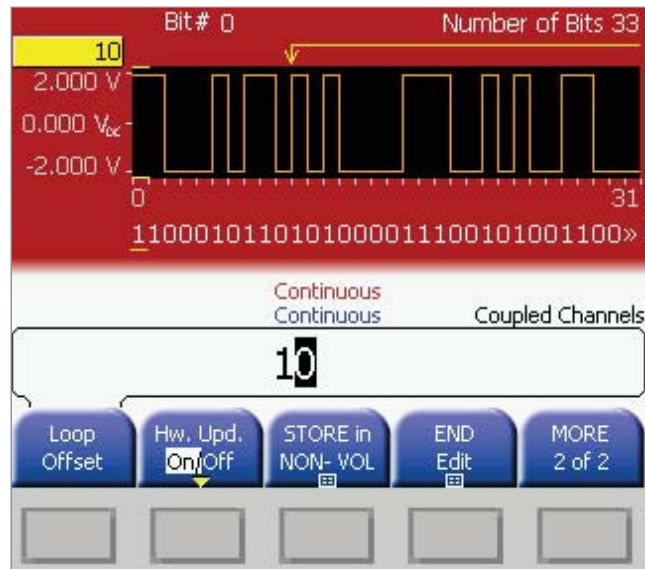The pattern defined this way or also any other stored pattern can be viewed in the Pattern Editor.

Figure 9. Pattern Editor

There, bits can be inserted and deleted, the pattern can be edited, and then stored to one of the 4 non-volatile memory locations for patterns or to an external USB memory device.

A bit position for a loop offset can also be specified. That way, it is possible to define an initialization or preamble pattern in front of the test pattern that will be looped during pattern generation.

Hw Upd On/Off decides whether changes in the pattern shall be programmed to the hardware immediately, or if the hardware update shall be suppressed until the editing of the pattern is finished. Edting will be faster, when hardware update is turned off.

Bit-shape parameter

If the bit-shape parameter on the pattern setup screen is set to 'Arbitrary', it is possible to select a predefined or user-defined waveform that specifies the shape of a bit. If the bit shape parameter is set to 'NRZ', rectangular bits will be created by the pattern generator.
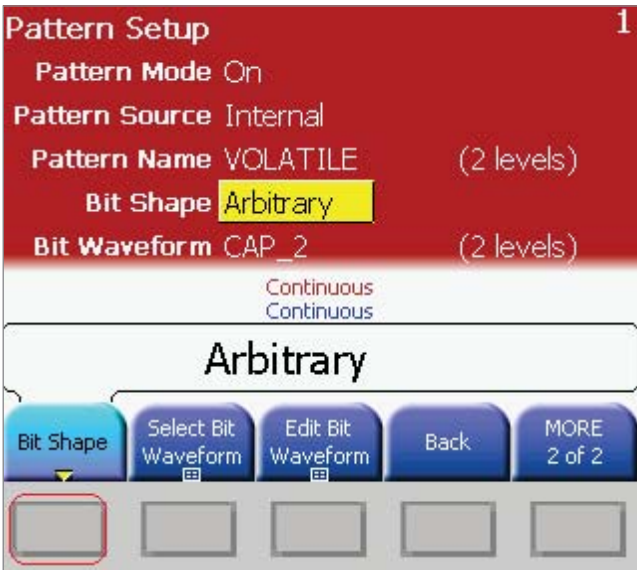
Figure 10. Bitshape arbitrary

Arbitrary bit waveforms

You can choose from 4 user-defineable and 6 built-in shapes that cannot be changed. One bit waveform can be saved to the volatile memory.
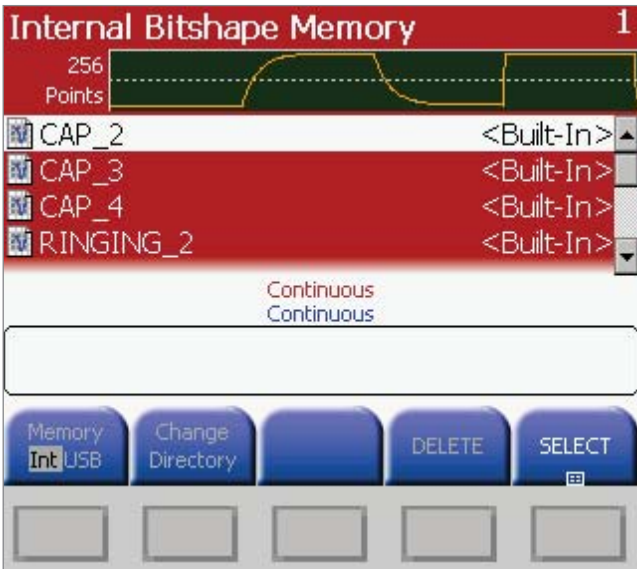

Figure 11. Bit shape memory

Built-in bit waveforms	No. of levels
CAP_2	2
CAP_3	3
CAP_4	4
RINGING_2	2
RZ_2	2
RZ_3	3

Create a new arbitrary bit waveform

You can create an arbitrary waveform with up to 64 points per bit. Depending on the number of levels of the pattern used, there are 4, 9 or 16 different bit shapes to be defined in one bitshape waveform.

The **Initial # of Points** defines the initial number of waveform points, which can later be changed. By default, **Interpolation** is turned on, which results in a straight-line connection between two points. If it is disabled, a constant voltage level is kept between points, which creates a 'step-like' waveform. With **Auto-Update** turned on, changes of the waveform will be applied immediately to the output. In this case, the editor is slower. If it is disabled, changes will be applied to the output after editing is finished.

Waveform Editor

The arbitrary waveform defined by the above parameters and all stored user-defined waveforms can be edited point by point in the Waveform Editor.

The Waveform Editor separates the waveform into different sections with vertical dashed lines. Each of the sections corresponds to one of the possible bit value transitions that are to be defined. In the upper left corner is displayed which bit value transition is currently being edited. Depending on whether a 2-, 3- or 4-level signal is being defined, there are 4, 9 or 16 possible bit value transitions.
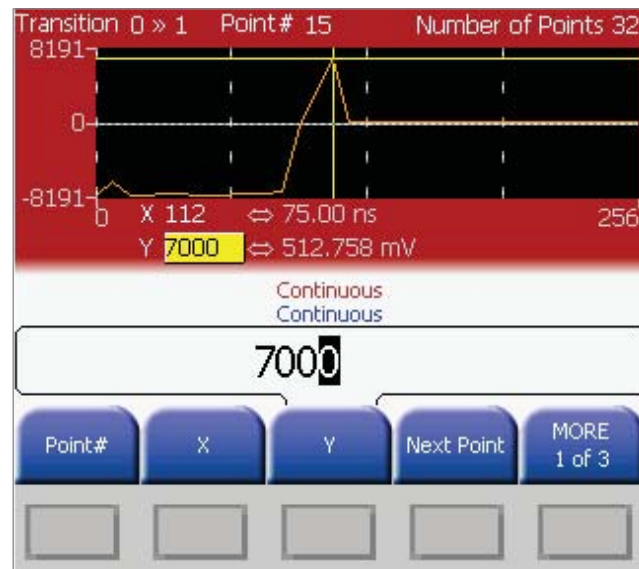

Figure 12. Waveform Editor

Initially, the points of a new waveform are all set to zero and can be adjusted using the editor. Points can be inserted and deleted. The waveform can be stored to one of the 4 non-volatile memory locations for waveforms or to an external USB memory device.

Hw Upd On/Off decides whether changes of the waveform shall immediately be programmed to the hardware or if the hardware update shall be suppressed until the editing of the waveform is finished.

In trigger mode, it is possible to select whether a trigger event will cause the generation of a complete pattern or just a single bit. The behavior in gated mode is similar, as it allows to either generate complete pattern cycles or 'blocks' as long as the gate signal is active. A started block is completed when the gate signal goes inactive. The other possibility is to gate on a per-bit basis, with the bit being completed when the gate signal goes inactive.
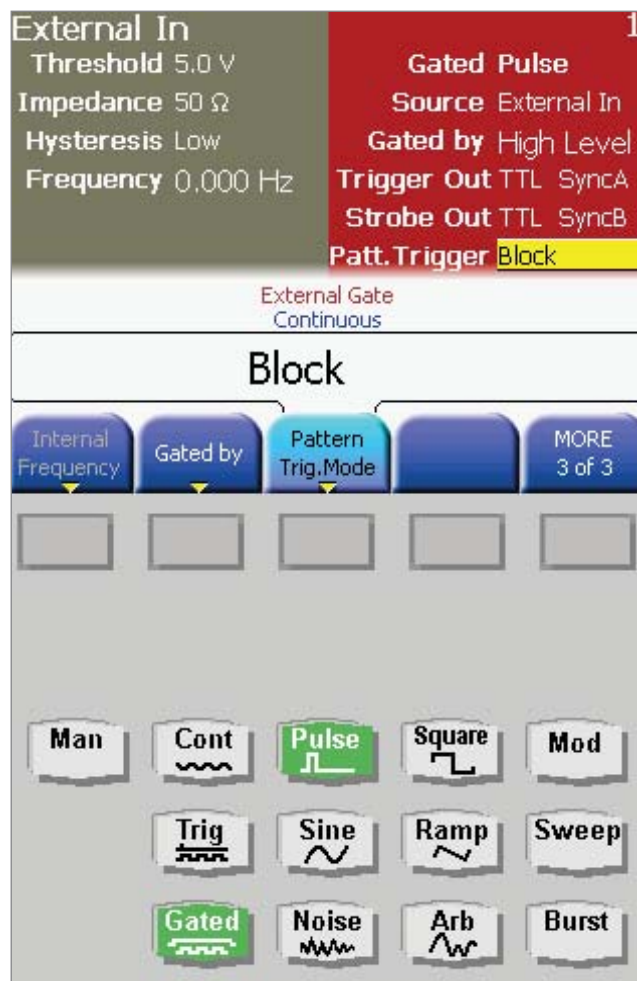

Figure 13. Pattern gated in blocks

	81150A Option PAT	81160A Option 330	81160A Option 660
Data rate	1 µbit/s to 120 Mbit/s (with internal pattern source)	1 µbit/s to 330 Mbit/s	1 µbit/s to 660 Mbit/s
Pattern memory	16 Mbit with 1 bit resolution	4 Mbit for 1-channel instrument 2 Mbit per channel for 2-channel instrument	
Pattern memory resolution	1 bit		1 bit for data rate 1 µbit/s to 330 Mbit/s 2 bits for data rate 330 Mbit/s to 660 Mbit/s
Number of levels	2, 3, or 4 (user selectable)		
Sequencing	Preamble followed by one looped data block—loop count: 1 - 10,000,000 the whole sequence can loop indefinitely or triggered		
Trigger modes	Continuous, gated, one bit per trigger event, one sequence per trigger event		
Pattern sources	Internal: PRBS -7, 9, 11, 15, 23, and 31 User-defined External: Pass through pattern mode. Pattern is applied and sampled at Modulation In. Indefinite pattern length. Up to 10 Mbit/s. Selectable automatic sampling for asynchronous operation or fixes sampling for synchronous operation		
External sampling	Automatic and fix		
Pattern modulation	AM, FM, PM		
Arbitrary bit shapes	User defined and predefined bit transitions with up to 64 arbitrary waveform points per bit transitions		

Ordering Information for Agilent 81150A

Ordering together with the 81150A
81150A-PAT   Pattern generator license for 81150A

Ordering for an existing 81150A
81150AU-PAT   Pattern generator license for 81150A upgrade

Ordering Information for Agilent 81160A

Ordering together with the 81160A
81160A-330   License for 330Mbit/s pattern generation
81160A-660   License for 660Mbit/s pattern generation

Ordering for an existing 81160A
81160AU-326   License for upgrade from 330Mbit/s to 660 Mbit/s pattern generation
81160AU-330   License for 330Mbit/s pattern generation
81160AU-660   License for 660Mbit/s pattern generation

Literature title	Publication number
81150A and 81160A Pulse Function Arbitrary Noise Generator Data Sheet	5989-6433EN
Pulse Pattern and Data Generators Brochure	5980-0489E
81150A and 81160A Pulse Function Arbitrary Noise Generator Demo Guide	5989-7718EN
81150A Pulse Function Arbitrary Noise Generator Flyer	5989-7720EN
81150A and 81160A Pulse Function Arbitrary Noise Generator Application Booklet	5989-7860EN
81150A Quick Fact Sheet	5990-4565EN
81160A Quick Fact Sheet	5990-6984EN

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