Agilent *Medalist* i1000D Boundary Scan Debug

White Paper

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With Boundary scan test technology being more commonly used in the electronics test industry today; there is a growing concern among test engineers and technicians about how to effectively handle the debugging of a boundary scan test. Most experienced engineers are proficient with boundary scan on the Agilent *Medalist* i3070 in-circuit test platform. Many though, are still very new to the *Medalist* i1000D ICT system.

Having debugged a number of boundary scan tests on the i1000D, I'd like to take this opportunity to share my experiences and learnings through this paper.

A good boundary scan test setup includes:

1. An i1000D test fixture with good digital signal quality

2. Stable working voltages on the device under test (DUT) that is related to the boundary scan device

3. Accurate boundary scan description language (BSDL) file

4. Correct logic levels for the digital drivers/receivers

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Signal quality of test fixtures

Having an i1000D test fixture with good signal integrity is of the utmost importance. Over the years, many ICT users have raised questions regarding boundary scan debug. One commonly asked question is, "How can I debug my boundary scan tests?" and my usual answer will be a counter question, "Is the signal quality of your test fixture good enough?"

In most cases, the user will reply, "Of course, the digital signal quality on my fixture is superb!" Or, "There's no problem with my test fixtures. All the digital resources on my fixture have ground plane isolation."

However, how can one verify the signal quality of the fixture? The only way is to probe the digital nodes on the fixture with an oscilloscope. Figure 1 shows a screenshot showing the TCK and TDO signals of a boundary scan test device during debug.

Therefore, it is recommended for users to check the signal quality of the fixture during debug using an oscilloscope.
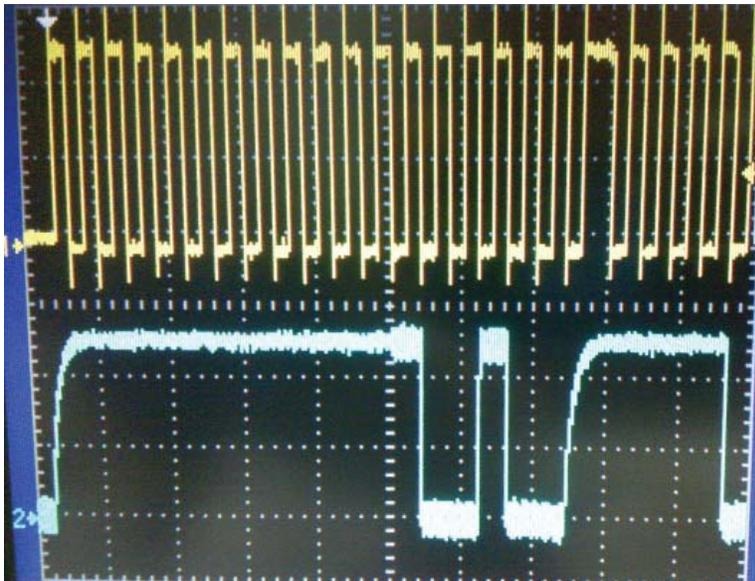
Figure 1. TCK and TDO signals of a boundary scan test device during debug

Stable working voltages

Why do we need a stable working voltage that is related to the boundary scan device under test? Most users will have the answer to this question. Without a stable working voltage, it is only logical that the device under test will not be in a stable condition and thus, any tests done will have unstable results.

Boundary scan devices may operate with several different input voltages. Voltages like +3.3 V, +2.5 V and +1.0 V are common for large devices like micro controllers and ASICs. Users working with these devices will need to ensure that all of the input voltages are available and stable throughout the entire boundary scan test sequence. Fluctuations in any of these input voltages will simply cause the device to go into an unknown state and stop responding to the boundary scan stimulus. Nowadays, many board designers employ pulse width modulation (PWM) as a method to control the power circuitry on their boards.

Firstly, the theory of PWM power circuitry. The PWM circuit converts an input reference voltage level to a pulse train of a specific pulse width. The pulse train is subsequently used to control the ON/OFF status of the power rails through some power transistors or MOSFETs, thus achieving a method of controlling the amount of power delivered by the power rail. A typical design starts with a triangular wave being fed into comparators. The comparators compare the triangular waves to a reference voltage and then switch their output accordingly, achieving a square wave with duty cycle controlled by the reference voltage. The higher the reference voltage, the longer the HIGH pulses on the square wave.

Reference voltage

Short "ON" pulse
Low power

Reference voltage

Long "ON" pulse
High power
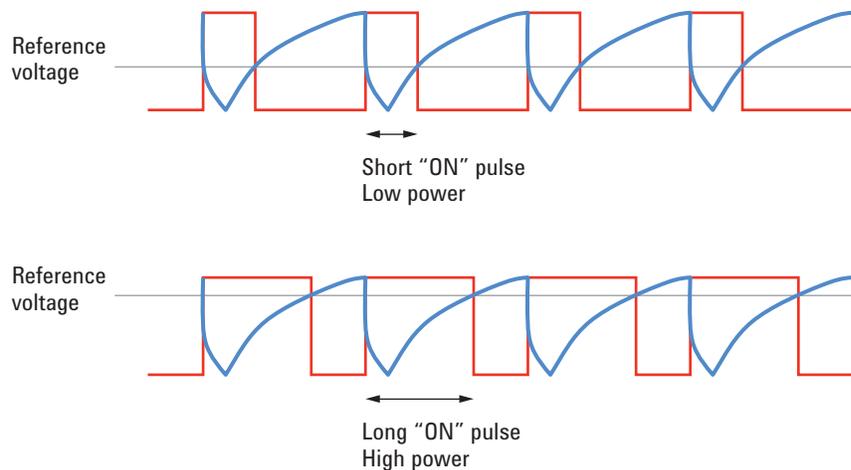
Figure 2. Illustration of comparative reference voltages, with higher reference voltages appearing as longer pulses on the square waveform

The square wave is now used to control the ON/OFF state of the power transistors or FETs. Therefore the higher the reference voltage, the longer the HIGH pulses and the longer the ON state. Controlling electrical power by means of quickly switching it on and off, and varying the "on" time, is known as Pulse Width Modulation.

Stable working voltages

Combined with other sense and feedback circuitry, the PWM circuitry is a delicate and complex design. Any offset or interference to any part of the circuit may result in unstable output of the power supply, or even cause the power supply to be totally turned off. This poses a huge challenge to the In-Circuit Testing (ICT) world. Figure 3 shows an example of a PWM circuit design.
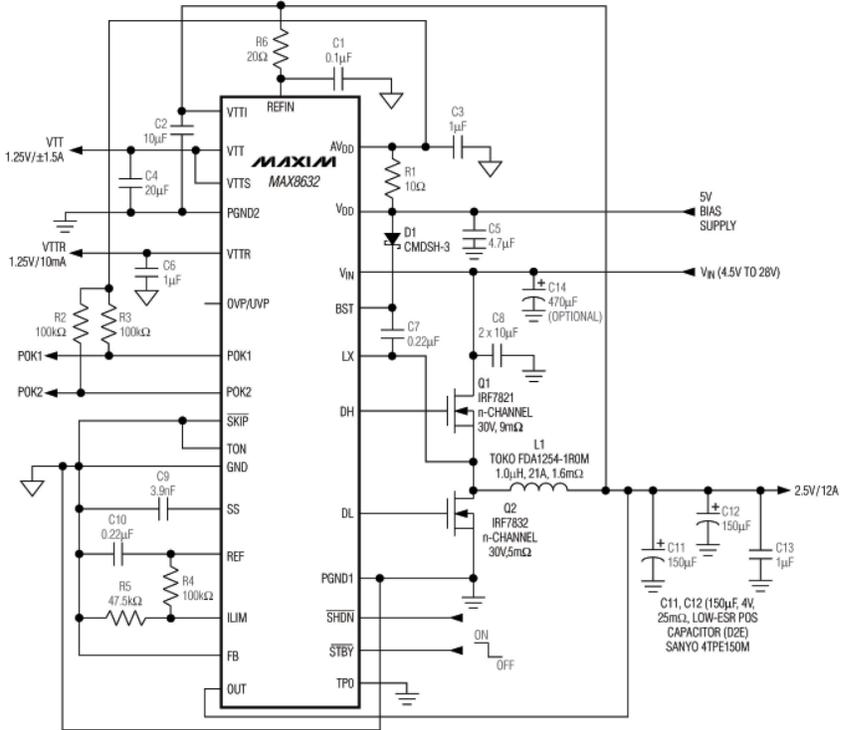
Figure 3. An example of a pulse width modulation circuit design

On an ICT fixture, each probe on the fixture has a certain amount of loading effect to the signal on the board. These additional loads from the test probes may just cause the PWM to become unstable and thus affect the output. Therefore, it is recommended that all test probes around the PWM circuitry be removed, leaving only the Input and Output section. This isolates all the sense and feedback signals of the PWM from the unwanted loads of the test probes and will help to ensure stability of the PWM operation.

You may wonder if these steps are sufficient to ensure stability. In most cases, isolating the PWM circuitry will directly result in much more stable working voltages. However, there are certain times where the power supplies may be interrupted during the boundary scan test itself. If that happens, then detailed analysis of the boundary scan test signals and outputs will need to be conducted to see if there are any nodes involved in the boundary scan test which are linked to the PWM circuit. If so, further isolation will need to be done. Therefore, it is recommended to insert some voltage measurement steps before and after the boundary scan test steps so as to help the user determine if the voltages are correct during the test. These additional steps can be easily removed after debug.

Accuracy of BSDL file

The *Medalist* i1000D software can read a BSDL file without any need to edit its format. The software also checks and validates the contents of the BSDL file for syntactical errors and topological mismatch with the device when it is being assigned.

However, the i1000D software cannot determine if the file is the correct BSDL file for the targeted device on the board. This will be the responsibility of the user. The user needs to work with R&D engineers or with the IC manufacturer to ensure the validity of the selected BSDL. Only with the right BSDL can you obtain the right results for the boundary scan tests.

Logic levels of digital drivers/receivers

Regardless of the complexity of the digital test, selecting the correct logic family which matches the targeted device is crucial.

How can the user know what logic family to use for his or her boundary scan device?

In most cases, the user can find the logic level information directly from the schematics. As shown in Figure 4, it can be easily seen that the boundary scan Test Access Port signals (TAP) use the 3.3 V logic. This is suggested by the pull-up resistors (R171) on the TMS pin. Therefore, user programs the logic family for the TAP pins to be:

Drive 'High'   = 3 to 3.3 V
Drive 'Low'   = 0 V
Receive 'High' = 2 to 3 V
Receive 'Low' = 0.2 to 0.5 V
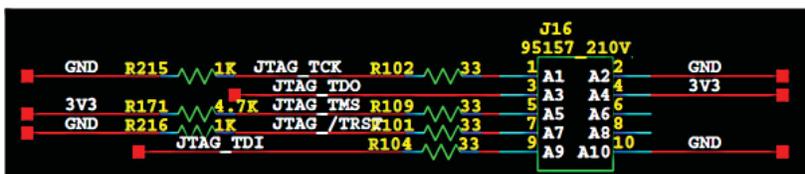
Figure 4: 3.3 V logic level for TAP signals

Logic levels of digital drivers/receivers

Similarly in the next example, the TAP pins had pull-up resistors to 2.5 V. Therefore, the TAP pins can be expected to operate in the 2.5 V logic level. Set the logic to be:

Drive 'High'   = 2 to 2.5 V
Drive 'Low'   = 0 V
Receive 'High' = 1 to 2 V
Receive 'Low'   = 0.2 to 0.5 V
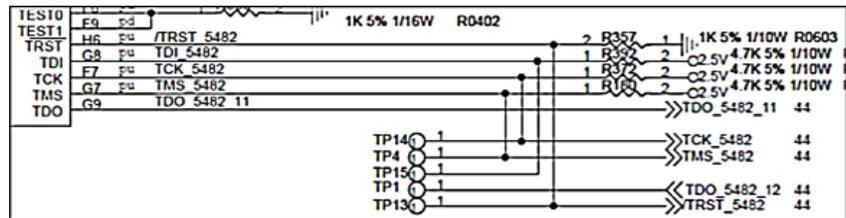
Figure 5. 2.5 V logic level for TAP signals

The next example shows that the TAP pins are not being pulled to any logic level. How will the user determine the logic family then?
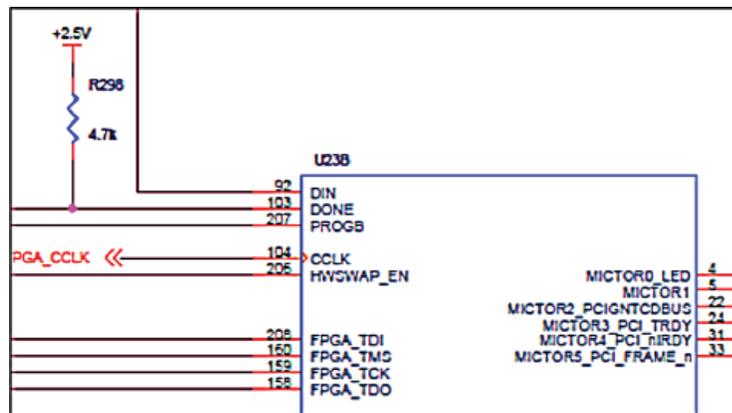
Figure 6. Device logic family defines TAP signal logic levels

Usually, the operating voltage of the boundary scan device will be the logic family of the TAP pins as well. Therefore, in cases where the TAP pins do not contain any pull up information, referencing the logic family to the device operating voltage may help. Of course, there will still be cases where the TAP pin logics are also different from the operating voltages. It will be good to refer to the data sheet in order to get the correct logic information for the device.

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Boundary Scan setup and debugging techniques on the *Medalist* i1000D

Let us use a typical i1000D test program to discuss boundary scan debugging techniques.

Firstly, assign the BSDL file for the boundary scan device to the IC digital status interface under the Digital Library column. Create a node library to define any upstream disabling or conditioning vectors and assign it to the respective devices under the Supplemental Library column as shown in Figure 7 below for U14 and U19.

Figure 7. IC Editor interface for library assignment

Next, double-click the "T" field under the Digital column to launch the boundary scan test (BST) interface, as illustrated in Figure 8.
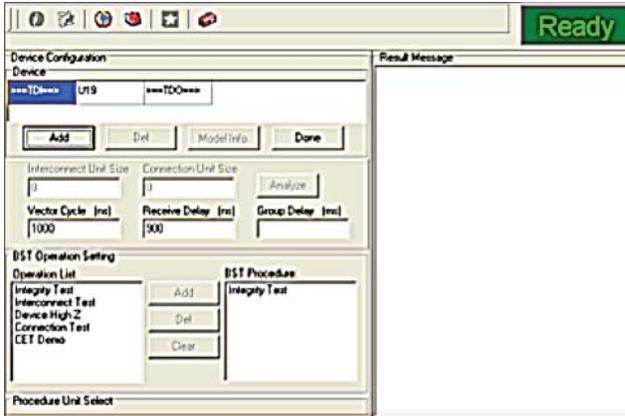
Figure 8. The Boundary Scan Test (BST) user interface

If the boundary scan device is connected as a chain, click **Add** in the BST interface to assign the other device in the boundary scan chain. The Device Assignment selection message will appear as below.
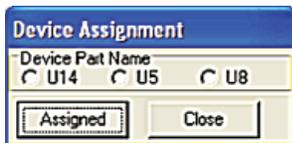
Figure 9. Device assignment selection

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Following the boundary scan chain connection on the board, complete the
assignment of devices on the chain and then click **Done**.

Next, click **Analyze** to have the software verify the chain information as below.
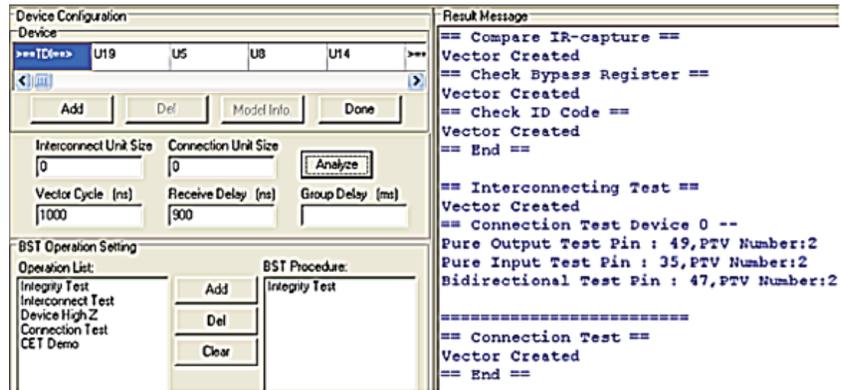
Figure 10. Boundary scan information analysis in BST interface

Leave the BST procedure with only Integrity Test, exit the BST interface and
move into the Test Editor Interface. Next, select the Function group, followed by
the function sub-group. At this juncture, if the boundary scan test step has not
been generated yet from the Test Developer process, you may add in a new line
and set up the test mode (BST) and part name for the first device of the bound-
ary scan chain manually.

Figure 11. Creating test steps in Function group

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Double-click the "StdVal" column of the step and you will be brought back into
the BST interface again; except that this time, you are not allowed to make any
changes to the chain information.

Figure 12. Selecting test types in BST Interface

Select the desired test operation from the Operation list on the left and click
Add to add it into the BST procedure list (see Figure 12). Double-click any of the
selected procedures in the BST Procedure and the details of that test procedure
will be displayed under the Procedure Unit Select section below.

*Figure 13. Selecting desired test operation from the
Operation list*

Units that are marked with "V" under the enable column are the active test
units to be executed. You may simply double-click to remove the "V" to disable
the respective test units.

Boundary Scan setup and debugging techniques on the *Medalist* i1000D

Testing a large number of pins at the same time in a boundary scan test will result in high Ground bounce, which in turn, affects the stability of the test. For that, the i1000D software provides a Unit Size setting for the Interconnect and Connect test units as per Figure 14 below.
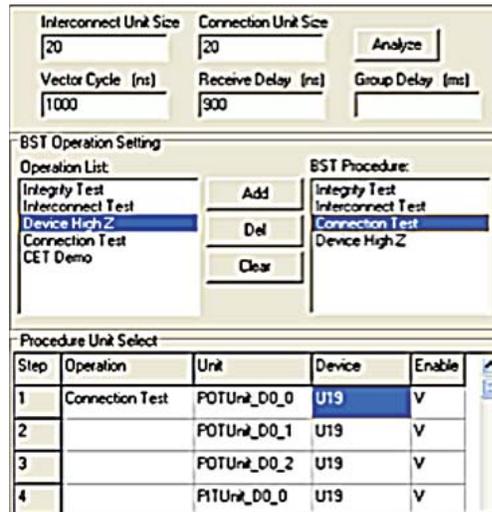
Figure 14. Unit size setting for the Interconnect and Connect test units

With the Connection Unit Size set to 20, clicking the Analyze button will cause the software to analyze the boundary scan test and allocate a maximum of 20 pins to each unit. You will see multiple test units (POT, PIT, BOT or BIT) generated. Double-clicking each of the units will reveal the list of pins tested within that unit on the Result Message window on the right.

In cases where you need to disable the test on a specific pin on the boundary scan device, the i1000D software provides a easy and simple method. Given the Figure 13 example, you may need to disable pin K33 of U19 (u19.K33).

Select **U19** on the Device Configuration section and click **Model Info.**.
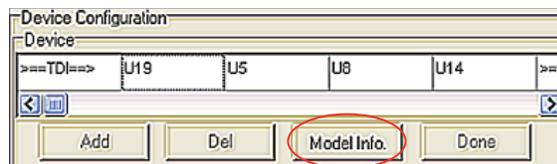
Figure 15. Displaying Model Information of the boundary scan device

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The software launches the Model Information window and the BSDL file is loaded and displayed. Use Ctrl+F and search for pin K33. Once found, simply click the 'Skip' field on the first column of pin K33 to disable it from the test. In this way, the software will no longer include pin K33 for the boundary scan test.

404		403	BC_2	PLB_CS_N_2	output3	x	398	1	z	K32	out	10	0
405		404	BC_7	PLB_CS_N_1	bidir	x	398	1	z	L30	inout	10	0
406	V	405	BC_2	PLB_CS_N_0	output3	x	398	1	z	K33	out	10	5178
407		406	BC_7	PLB_DATA_15	bidir	x	407	1	z	L31	inout	10	454

Figure 16. Disabling boundary scan test for specific pins

Debugging of any boundary scan test should start from the Integrity Test step. This is to ensure that the basic connections of the boundary scan signals (TAP pins) are correct and also that the Device ID of the physical part matches what is stated in the BSDL file.

Double-click **Integrity Test** under the BST procedure section to have the software generate the test patterns internally. Then click the Debug GUI icon as shown in Figure 17 below.
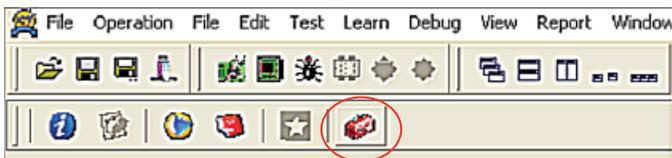
Figure 17. Debug icon on the user interface

On the bottom left of the Debug GUI, the Group Name section will list the different signals used in that test. Simply double-click the signal name or click **Show** to display the selected signal on the graphic display (Figure 18).
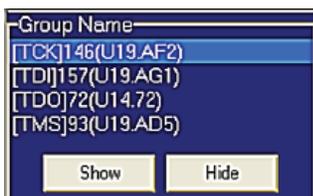
*Figure 18. Group Name lists the
different signals used in the
boundary scan test*

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The Debug GUI for the boundary scan test allows you to adjust the logic levels of each of the signal pins in the select test. To make adjustment to any signal, the selected signal must be displayed on the graphical window first.

When adjusting the logic levels, for example TDO, select the TDO signal on the graphic window and enter the required logic level in the fields provided on the left in the Logic Family section.

Figure 19. Adjusting logic levels on selected signals

After adjustment, click **Save** on the bottom right of the window and the test patterns will be updated immediately. There is no compilation or reload required.

Figure 20. "Pattern Ready" indicates readiness of test patterns

The Message Window will show "Pattern Ready", which indicates that the test patterns are ready (Figure 20). You may now click **Execute** to run the test with the new settings.

In most cases, with an accurate BSDL and correct logic level selection, the Integrity Test can be easily turned on to run without any issue. However, if the Integrity Test continues to fail despite the BSDL and logic level being accurate and correct, then there may be other problems affecting the TAP signals or the power stability of the device and test. In that case, you will need to use an oscilloscope to test the TAP signals to determine the source of the interference. There can be many possible causes of interferences, so these will not be discussed in this document. Once the Integrity Test passes, you may move on to debug the other tests, like the Interconnection Test.

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Interconnection tests are generally easier to debug as they use the boundary scan devices themselves to send test patterns to each other. In that sense, the logic levels are already taken care of during the design of the circuit board, leaving only possible problems, like probe loading. In Figure 21, the boundary scan circuit shows that the TDO pin for each boundary scan device is connected to the next boundary scan device TDI pin with a series resistor. Nodes on both pins of the resistor are probed on the test fixture. During boundary scan testing, the signal quality of the TAP pins is of the utmost importance. They should be clear of any interference and loading. Therefore, in the above example, the test probes on both nodes of the series resistors need to be removed from the test fixture in order to prevent any loading effect to the TDO/TDI signals. Similarly, test probes on the TCK and TMS signals may also be removed to minimize probe loading effect. The only test probes required are those for the TDI, TCK, TMS signals on the first device, and the TDO of the last device on the boundary scan chain.
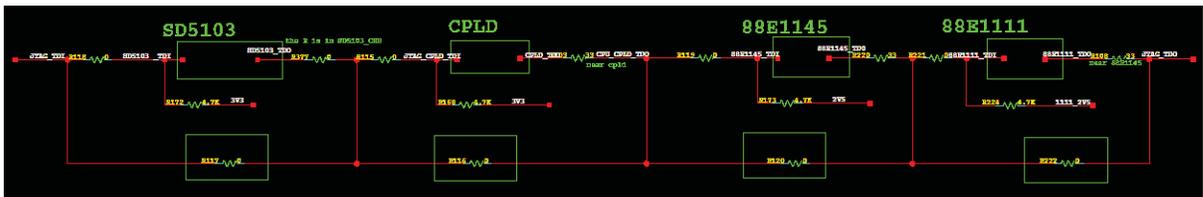
Figure 21. Boundary scan chain circuit

I would like to highlight that Connection Tests can pose more challenges. As the Connection Test utilizes the test resources from the tester, you need to control more parameters in order to ensure that the test patterns are acceptable to the devices. Issues like wrong logic levels, probe loadings, noise interference, etc are potential factors to be dealt with. So in most cases, you will need an oscilloscope for debugging a Connection Test node in order to check the actual signal condition on the board itself. Details of the debug process will not be discussed in this document.

From my experience in working with the i1000D, boundary scan debug is not difficult. With good fixture quality, stable working voltages, accurate BSDL file and correct device logic level settings, one can easily turn on the boundary scan test.

I hope that Agilent i1000D ICT users who are working with boundary scan will find this document useful and informative. If there are any questions or comments to share, please visit our online discussion forum: **www.agilent.com/find/ictforum**

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