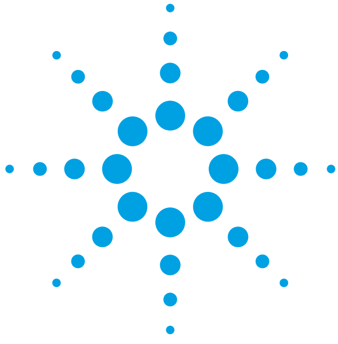


Accurate Calibration of Receiver Stress Test Signals for PCI Express® rev. 3.0 Assuring Interoperability at Data Rates of 8 GT/s

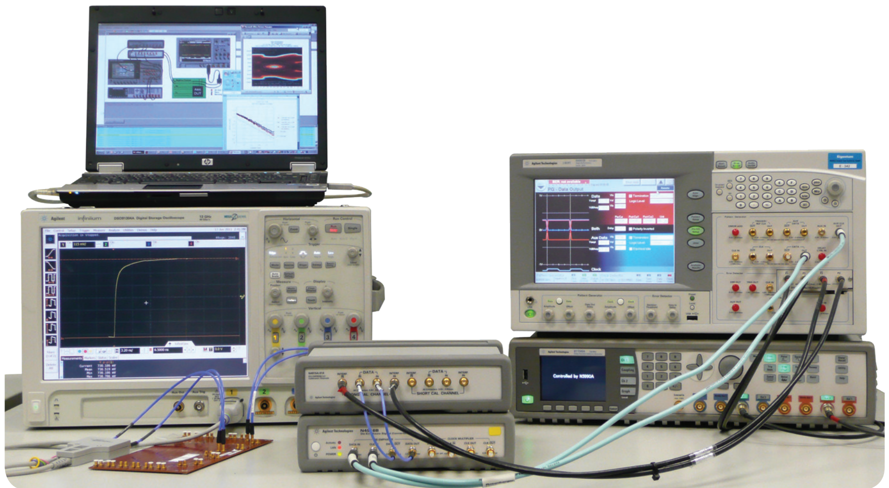
Application Note

Introduction

Chip and system designers face new challenges as data rates move beyond 5 Gb/s. Transmission of such fast signals across printed circuit boards (PCB) deteriorates the signals so much that the eyes at the receiver (RX) inputs may be completely closed. Because the passive infrastructure (such as riser cards of existing servers) is reused when cards are upgraded for the next speed grade, the "channel" properties, i.e., the PCB trace lengths, remain unchanged.

Therefore the capabilities that enable higher data rates must be implemented in the active parts of the transmission system: in the transmitters (TXs) and RXs. As TX de-emphasis, which is already commonly used at lower data rates, only partially compensates channel-induced data dependant jitter (DDJ) such as inter-symbol interference (ISI), RX equalization must be included to enable error free[1] transmission. Therefore RX testing is no longer optional and thus is included in standards such as the base and the card electro-mechanical (CEM) specification of PCI Express® rev. 3.0[1] that support transfer rates of 8 GT/s.

1. *In this context "error free" is equivalent to a detection with a BER lower than a specified value, very often* 10^{-12}



About This Document

This paper describes the calibration of the receiver-stress signal according to the base specification of PCIe 3.0. This differs in the following ways from what was common practice at lower data rates, e.g., for PCI Express rev. 2.0:

- The specifications relate to a point inside the RX, which makes post processing of the measured RX test signal necessary
- Accurate measurement of this test signal is impractical and error prone due to the noise floor of current real time oscilloscopes (RTOs); therefore,
    - Calibration of deliberately injected impairments is separated from the characterization of the test setup, and
    - The RX test signal with the intended eye opening is constructed using simulation software.
- Other aspects of the PCIe3 RX test related to the CEM specification, such as the link training procedure, are not included in this document as the related test procedures are not yet defined (see Figure 1).

Agilent Technologies

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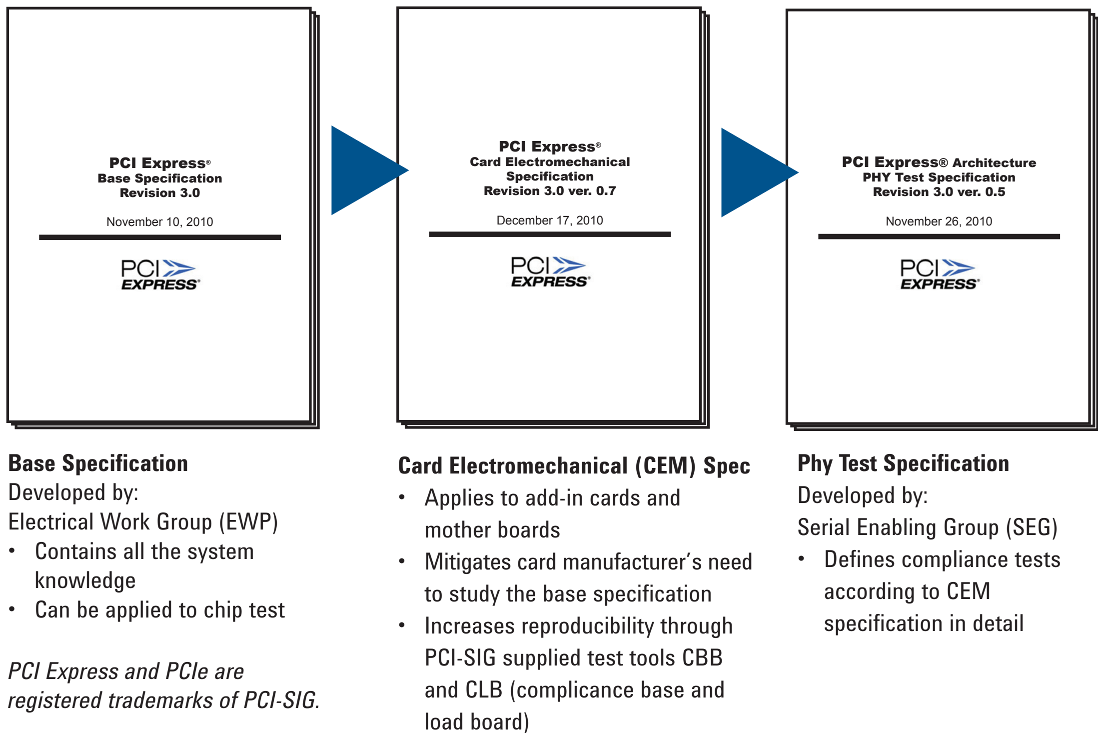
PCIe Working Groups and Resulting Standards and Test Procedures

The PCI standard body has several work groups that contribute to the different standard documents, which together define the functionality of the PCI Express bus system. Those standard documents defining the physical layer (PHY) are depicted in figure 1, which also explains the main deliverables of the work groups.



Base Specification
Developed by:
Electrical Work Group (EWP)
- Contains all the system knowledge
- Can be applied to chip test

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Card Electromechanical (CEM) Spec
- Applies to add-in cards and mother boards
- Mitigates card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (complicance base and load board)

Phy Test Specification
Developed by:
Serial Enabling Group (SEG)
- Defines compliance tests according to CEM specification in detail

Figure 1. Sequential development of the PCIe specifications relevant for the PHY and their scope

2. RX-Test Procedure and Test Setup

2.1. Generic RX test: an overview

The RX test at > 5 GT/s is identical to those at lower data rates (e.g., PCIe 2.x).

The input of the RX under test is stimulated with a "stressed eye" signal. This signal is composed of all possible impairments expected at the RX input when operating in a target system, including timing impairments (jitter) and superimposed voltages (very often called "noise," although for test purposes they are sinusoidal shapes).

Because the RX output usually cannot be probed directly, the output signal is looped back through the device's TX[2] so that the RX's correct detection can be observed with a bit error ratio tester (BERT) (see Figure 2).

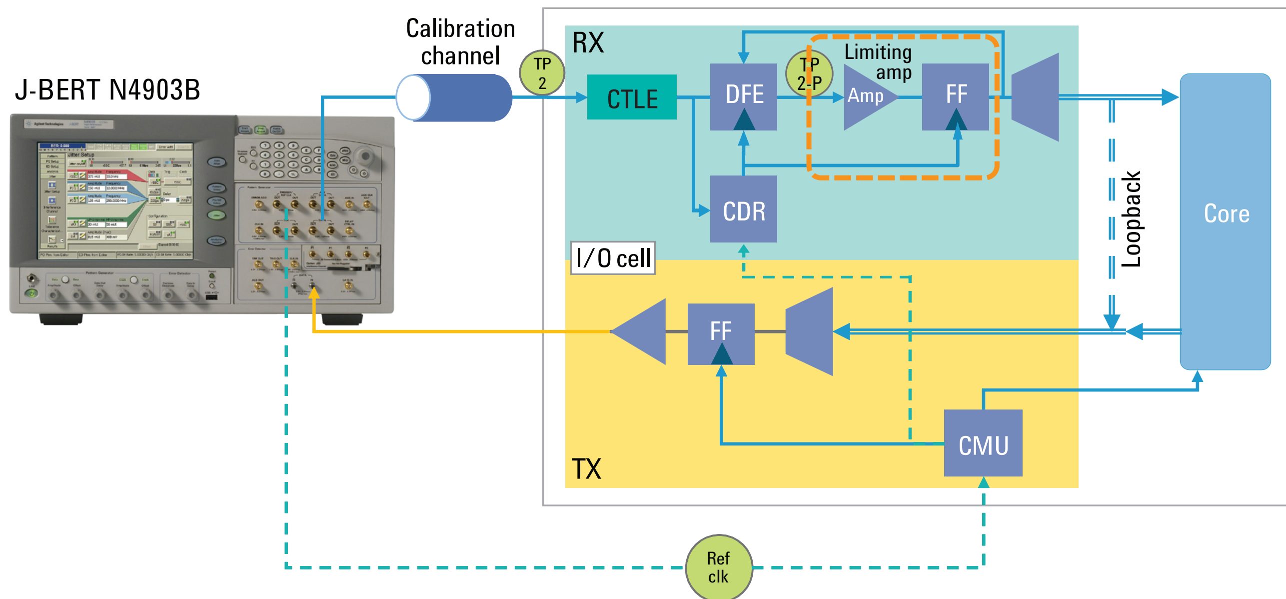


Figure 2. RX block diagram with equalization (CTLE and DFE) and test points (TP2 and TP2-P) according to PCIe 3.0

2. *The TX is assumed to operate error free*

2.2. Definition of the RX stress test signal for PCIe 3.0

Proper calibration of the stressed eye height (EH) and eye width (EW) or its contributing components (such as voltage noises and jitter) is essential to achieve a valid and reproducible test result that eventually guarantees interoperability. For transfer rates up to 5 GT/s, this calibration is usually achieved by measuring the test signal as close as possible to the RX input with a suitable instrument such as a real-time oscilloscope (RTO) and then adjusting the relevant signal parameters of the BERT generator until the desired result is achieved (EH and EW or amount of, for instance, random (RJ) or sinusoidal (SJ) jitter). For higher data rate computer-interconnect applications such as PCIe 3.0, a different calibration method in accordance to that used for defining channel compliance was chosen.

Since a goal for PCIe 3.0 was to re-use the passive infrastructure (i.e., the channels), it was necessary to develop a compliance test method that would result in a "pass" for those channels, which passed PCIe 2.x tests. The longest of these channels deliver closed eyes at their outputs. Therefore, a reference RX was defined that would open up the eyes to a reasonable EH and EW, both sufficient to drive the basic RX of Figure 2 (see orange colored, dashed line). The eye opening was chosen as the figure of merit as it directly translates into well understood RX characteristics such as input sensitivity and minimum tolerable width/ jitter tolerance caused by intrinsic input noise and flip flop (FF) set-up and hold times, respectively. Using the same reference RX model[3] to define the RX compliance test and stress test signal was therefore, self-evident.

Figure 2 shows the reference RX's building blocks:

- A behavioral model for the reference package
- A continuous time linear equalizer (CTLE)
- A clock recovery (CR)
- A 1-tap decision feedback equalizer (DFE)
- A limiting amplifier

By defining the stress signal inside a reference RX, it becomes obvious that calibration cannot be achieved by measurement alone (e.g., at TP2, as it was done for PCIe 2.x). Instead, the calibration must include some sort of signal processing to forward the measurement result to the virtual test point TP2-"P" ("P"= post-processing), where the specifications apply.

New in PCIe 3.0

Post-processing of signal measured at TP2

Under PCIe 2.x, it was possible to calibrate the RX stress signal by measurement only. However, under PCIe 3.0, the knot where the specifications apply cannot be probed (specification refers to TP2-P of Figure 2). Therefore post-processing of the signal[4] measured at TP2 is required.

3. *The PCIe 3.0 base specification does not enforce the implementation of the reference RX – only its performance must be achieved for compliance.*

4 *Note that the signal used for calibration of the test set-up at TP2 is NOT the same signal that is used during the actual RX-test, see Chapter 3.2.2.*

3. Measurement Setup for PCIe 3.0 – RXs

Figure 3 shows a more detailed measurement setup for RX test as it is found in the PCIe base specification rev. 3. Connection of the DUT-ASIC (residing on a custom test board, lower right) with test equipment is achieved through "breakout channels." For the actual transfer rates beyond 5 GT/s, the signal degradation of the breakout channels (DDJ)/(ISI) is significant. Probing for calibration of the stress signal directly at the ASIC pins (i.e., balls) is not possible.

Therefore, the structure of the test board with the so-called replica channels (creating TP2) is defined (upper right). Because the replica channels duplicate the breakout channels, the signal at TP2 at the end of these replica channels is equivalent to the signal at the ASIC's RX-input pins.

In order to emulate different target applications, three test cases with different channel lengths are defined (center of Figure 3 and Figure 4). The depicted "sinusoidal signal sources" (Figure 3, left) simultaneously provide voltage "noise" such as common mode- and differential mode-sinusoidal interference (CM-SI and DM-SI). Dedicated tests with different test signals ("stressed-voltage-eye" and "stressed-jitter-eye") aiming to verify the RX's "sensitivity" and "minimum tolerable width/jitter tolerance" have been defined as well. (Parameter values are listed in Appendix 7.3 and 7.4.)

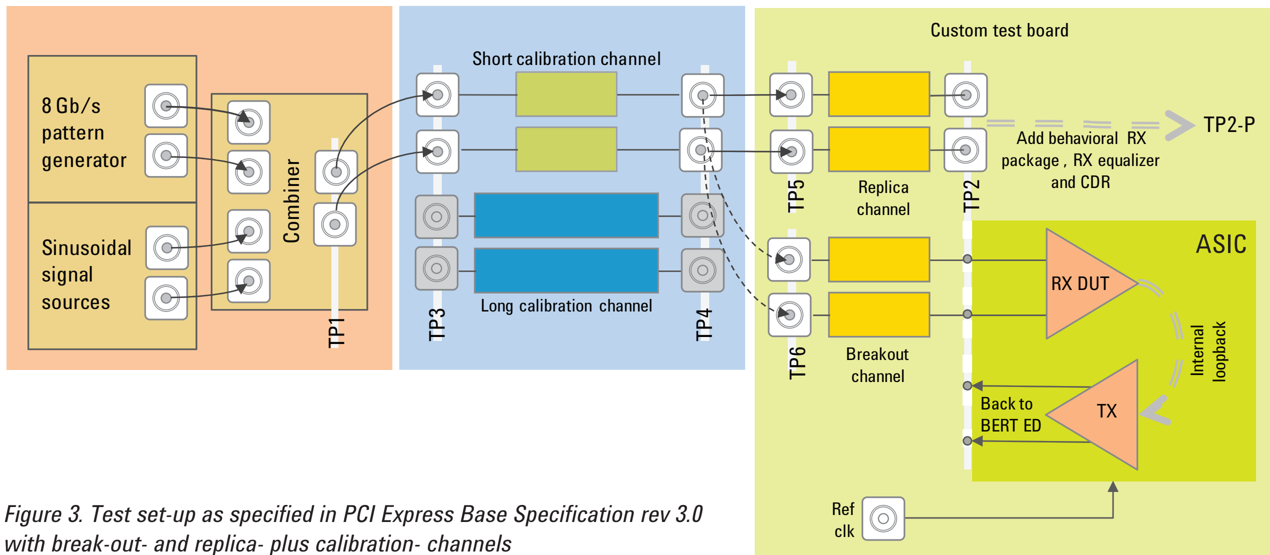


Figure 3. Test set-up as specified in PCI Express Base Specification rev 3.0 with break-out- and replica- plus calibration- channels

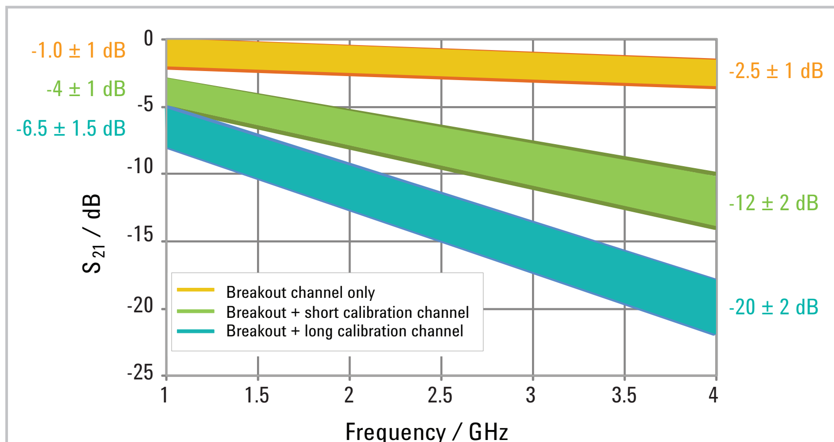


Figure 4. Insertion loss specifications for the three test cases

3.1. PCIe 3.0: Accurate measurement of the stress signal at TP2 is impractical and error prone

Attempting to calibrate the RX stress signal by measuring the specified RX test pattern ("modified compliance pattern," for details see Appendix 7.2) with all impairments turned on at TP2 and then post-processing this signal towards TP2-P such that the resulting eye can be assessed, reveals a measurement dilemma. The resolution setting on the RTO of 100 or 200 mV/div necessary to capture the full maximum swing of 800 mV (achieved for long runs of "1s" and "0s") and the intrinsic noise that comes with this setting, conflicts with the mV vertical accuracy necessary to precisely construct (nearly) closed signal eyes. This is especially true after long channels, as it significantly reduces the eye opening[5] – even more at TP2-P after post-processing.

As a result of this dilemma, the higher the intrinsic noise of the RTO used for calibration, the smaller the eye opening during calibration would appear (not: "be"). The amount of stress deliberately added by test equipment to achieve a certain eye-closure would therefore have to be reduced, eventually making it easier for the RX to pass the test – a dependency that must be avoided!

Figure 5 (left) shows a screen shot of a compliance pattern with an amplitude of approximately 800 mV with DM-SI of 14 mV at 2.1 GHz being superimposed (see Appendix 7.3). Turning off the pattern should show the sinusoidal interference of 14 mV_{PP}, but it doesn't as it is obscured by the intrinsic noise of the RTO (approximately 4.7 mV_{RMS}, theoretically resulting in up to 64 mV_{pp} for BER 10^{-12}).

Removing the intrinsic noise of a scope from a complex test pattern algorithmically is nearly impossible. Therefore, the approach described in Chapter 3.2 has been specified.

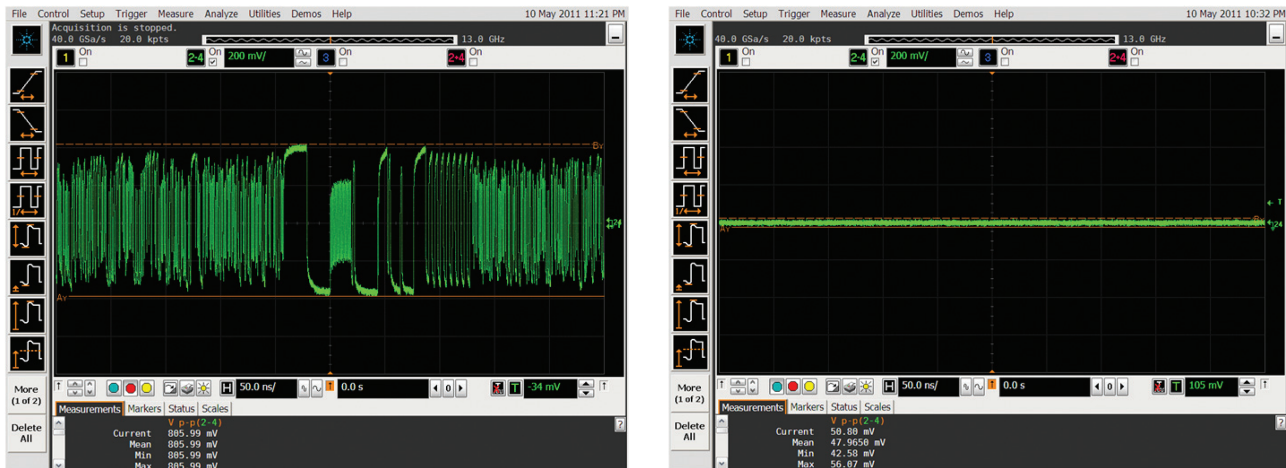


Figure 5. Screen shots of compliance pattern w/ superimposed DM-SI of 14 mV_{PP} (left) and with pattern paused (right)

5. *Intrinsic noise obviously reduces EH; but EW is impacted as well through conversion of voltage noise into "timing noise" (jitter) during signal transitions, closing the eye horizontally.*

3.2. Constructing the stressed eye with a statistical simulator SW (Seasim) and a calibrated jitter generator

First, it is necessary to *measure* all characteristics of the test set-up in use (according to Figure 3: signal generator, cables, splitters/adders, calibration channels, etc...) and *calibrate* in-situ at least those impairments that are influenced by this set-up.

Second, measuring at TP2 requires removing the RTO's intrinsic noise, usually achieved by *averaging*. This technique, however, removes all deliberately injected (non-pattern-correlated) noise and jitter from the signal as well. Therefore, the calibration of the impairments and the characterization of the test setup must be separated.

Additionally, as averaging is only practical for a repetitive pattern of reasonable length a much shorter than the modified compliance pattern must be used for the characterization of the test setup (8,552,960 bits are definitely too long, see Appendix 7.2).

The process for construction and calibration of the test signal for the desired eye-opening is described in Chapters 3.3.1 and 3.3.2.

3.2.1. High level/short form description of the calibration method

The test setup is characterized using a repetitive signal (low frequency clock), which is captured with an RTO using averaging. This captured waveform is fed into a statistical eye analysis simulator SW-program (Seasim) that constructs the RX input eye as seen at TP2-P. Seasim does this in the presence of a variety of adjustable impairments and then optimizes all simulated equalizers of the reference RX for maximum eye opening. The user or an automation SW adjusts the relevant impairments until the desired eye-opening (EH and EW) is reached. These values are then transferred to a test generator featuring jitter generation (e.g., the Agilent J-BERT N4903B) and each impairment is calibrated individually for the test generator, using the best suited method (including test signal and test point).

New in PCIe 3.0

Changes to RX stress signal construction and impairment calibration

Because of intrinsic oscilloscope noise it is impractical using the final PCIe 3.0 test pattern and the impairments cannot be turned on for in-situ calibration of the "stressed eye." The RX stress signal (i.e., the actual data pattern as well as the desired impairments) has to be constructed in software. Furthermore, calibration of signal impairments must be performed during a separate measurement step.

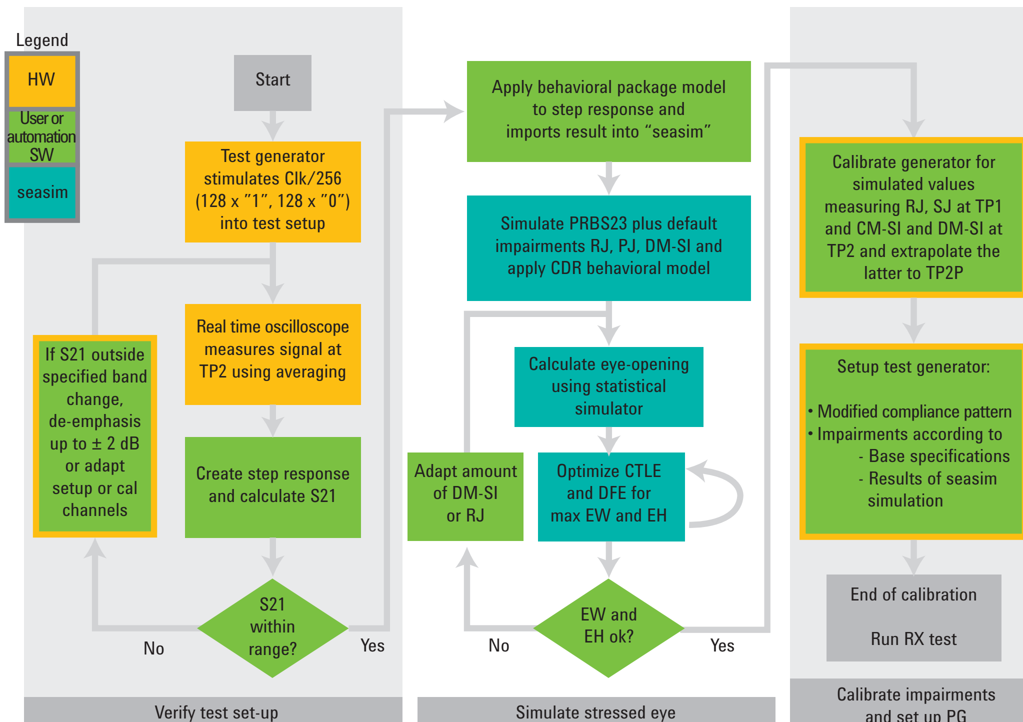


Figure 6. Flow chart of stressed eye signal calibration for RX test according to PCIe 3.0 rev 3

3.2.2. Step-by-step description of calibration method

Capturing the calibration signal and verifying the test setup (Figure 6, far left)

1. The BERT Pattern Generator (PG) provides the specified, repetitive pattern (i.e., a clock/256 = 31.25 MHz (128 x"1," 128 x"0"). This signal is captured with an RTO using averaging to eliminate intrinsic noise.

   The first part of the waveform, representing a positive "step response," is stored in suitable format. Seasim calculates the impulse response (dv/dt) and performs an FFT on this signal delivering insertion loss vs. frequency (magnitude of S21)[6]. With this intermediate result, it is possible to check if the actual set-up fulfills the specification.

A deviation of S21 from the specified tolerance band (see Figure 4) may be compensated with up to ± 2 dB of additional PG de-emphasis; if compensation is desired, then step 1 has to be repeated and the result re-checked.

For visualization purposes, the steps described above (i.e., the measurement of the step response, and the calculation of the impulse response (dv/dt) and the insertion loss (FFT)) are performed on an Agilent DSA 91034A RTO for two different de-emphasis settings (see Figure 7). While the 0 dB de-emphasis setting (step- and impulse- response not shown) led to an insertion loss larger than 20 dB, the -1.5 dB de-emphasis setting yielded an insertion loss of exactly 20 dB.

If the deviation is larger than 2 dB, or if the compensation does not produce S-parameters within the specified limits, the set-up and/or calibration channels have to be adapted accordingly.

With this method, all non-idealities of the components comprising the test set-up (cables, adders or test generator) are actually measured as part of the "step response" and accounted for in subsequent steps[7]. Therefore, although only an LF-Clock signal is used for characterization of the test set-up, this method is equivalent to the direct measurement of the final test signal at TP2, so it is much more accurate than using the S-parameters of the calibration channels alone!

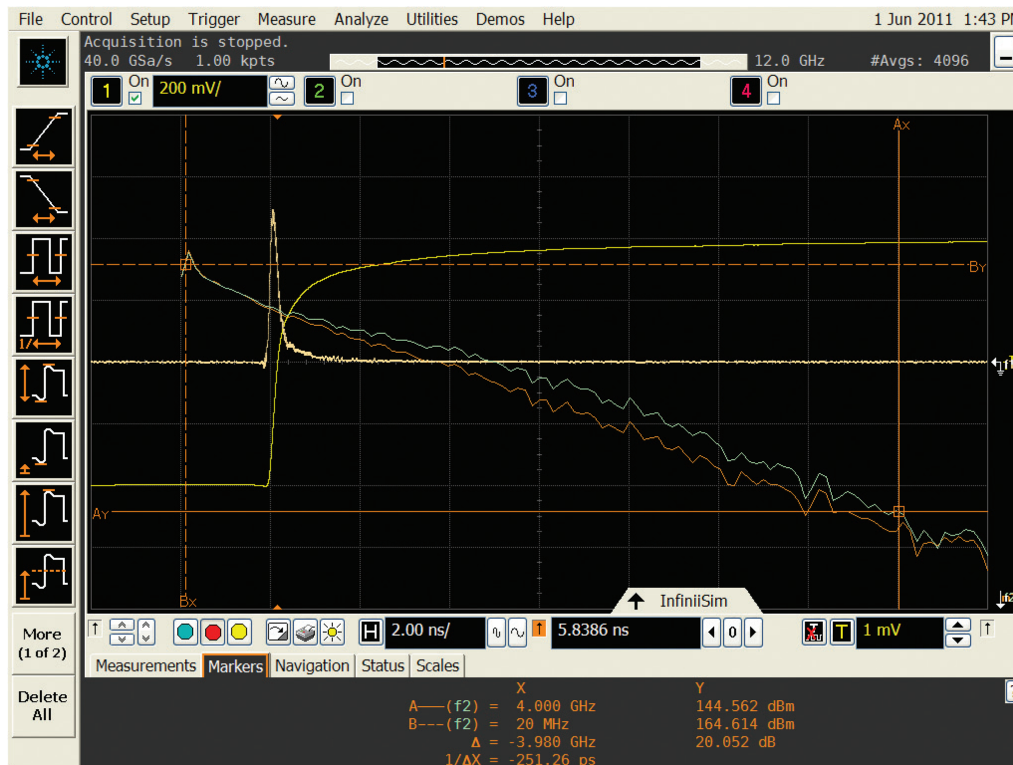


Figure 7. Measured step response and calculated impulse response (dv/dt) and insertion loss (FFT of dv/dt) for two different de-emphasis settings (0 dB and -1.5 dB), leading to exactly 20 dB of insertion loss

6. *Since the raw S21(frq)-curve may show ripples and artifacts of the FFT close to 0 Hz, it is necessary to extrapolate avoiding false readings at 4 GHz.*
7. *As required by the base specification rev 3.0 chapter 4.3.4.3.1 line 9-11.*

Constructing the eye with Seasim statistical simulator SW (Figure 6, middle)

2. The reference package model is applied to the captured waveform using the Infinisim feature of the Agilent series 90k RTOs and the statistical eye analysis SIMulator-SW (Seasim) is used to construct an eye from this step response, simulating the specified test pattern and impairments such as RJ, SJ and DM-SI.

3. The two equalizers are adjusted automatically by the simulator SW (using the reference CDR for the DFE) until the widest/highest eye opening is found.

4. Adjusting the value of that impairment, which is specified as variable for the specific test, delivers the specified eye width/height.

Figure 8 shows two Seasim result screens for the "construction" of the stressed voltage eye with the long calibration channel. On the left, the starting value of 14 mV was chosen, resulting in an eye height (EH) of ~27 mV. So, the DM-SI was increased by 2 mV, reducing the EH to ~25 mV, while at the same time bringing EW into the specified range between 0.30 and 0.35 UI.

Calibrating each generator impairment individually (Figure 6, far right)

Because performing accurate measurements at TP2 is difficult, this test point should be avoided whenever possible; TP1 should be used instead (see Figure 2).

Also consider that factory calibration (at least when using the Agilent N4903B) may be sufficient or even superior to in-situ calibration because often the test equipment or routines used for in-situ are inferior to the very diligent factory calibrations of the Agilent J-BERT.

However, if a jitter parameter shall be calibrated, then a clock/2 pattern (1010) should be used.

5. The DM-SI parameter definitely needs calibration within the actual setup. As with a sinusoidal frequency of 2.1 GHz, its amplitude at TP2 is influenced by the calibration channel in use, (see Figure 3, loss at 2.1 GHz is approximately 13 dB). The best suited "data-pattern" for this measurement, is a constant "1" or "0." This also applies for calibration of CM-SI also.

6. When the simulation is finished, the values of all resulting impairments are transferred to the now properly calibrated test generator.

7. The BERT PG is setup to stimulate the specified test pattern and a standard RX test utilizing loop back is performed.

Summary Chapters 2 and 3

- The role of the RX for proper system functionality became more important with the transfer rate of 8 GT/s of PCIe 3.0. Therefore, even the CEM specification defines the RX test for PCI Express rev. 3.0 as *normative*.
- The PCIe 3.0 base specification does not enforce a certain RX implementation. Silicon vendors can make their own choices with respect to equalization, package and receiver sensitivity/minimum acceptable width. However, the base specification reference RX defines the minimum eye opening of an RX input signal that must still be detected with the specified bit error ratio (BER) of 10^{-12}.
- The stressed eye is constructed using a simulator SW.
- The RX test procedure itself has not changed: the RX is still stimulated with a deliberately impaired test signal and the BER of the signal looped back is observed at the TX output.

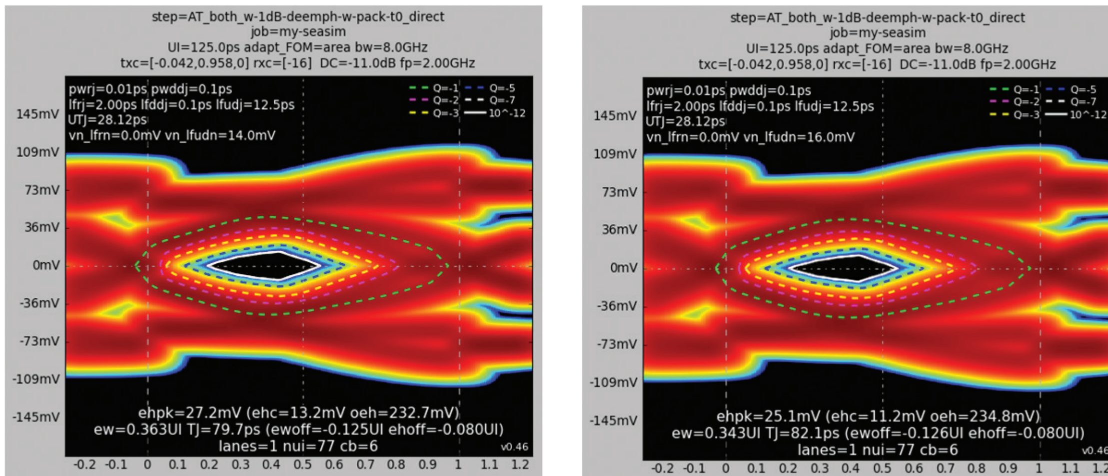


Figure 8. Result screens from Seasim with nominal DM-SI (left) and adapted DM-SI values

4. Practical Test Setup for Generation of Stressed Eye Test Signals

The test set-up depicted in Figure 9 uses Agilent's N4903B J-BERT for pattern generation and random- and sinusoidal- (RJ and PJ) jitter injection. The N4916B de-emphasis signal converter provides adjustable pre- and post-cursor de-emphasis. The signal is then passed through the selected calibration channel provided by Agilent's N4915A option 014[7]. J-BERT's option J20 is used for generation of DM-SI and addition of CM-SI[8]. The latter is generated by the Agilent 81150A dual channel function generator, which looks a bit like an overkill for something as trivial as the generation of the 120 MHz CM-SI.

However, there are two reasons for using this instrument in the set-up:

1. The specified CM-SI is relatively large compared to the necessary DM-SI (150 or 250 mV vs. approximately 10–20 mV, see Chapter 7.3), so that any unwanted CM → DM conversion through differences in attenuation and transit time in the "P" and "N" path must be avoided, or adjusted. That's exactly what can be achieved using two separate and individually adjustable sources as provided by the 81150A.
2. Furthermore, using passive splitters and/or power dividers (directional couplers are prohibitive because of their narrow bandwidth range) to distribute one CM-source into both "P" and "N" lanes would open a crosstalk path between those lanes.

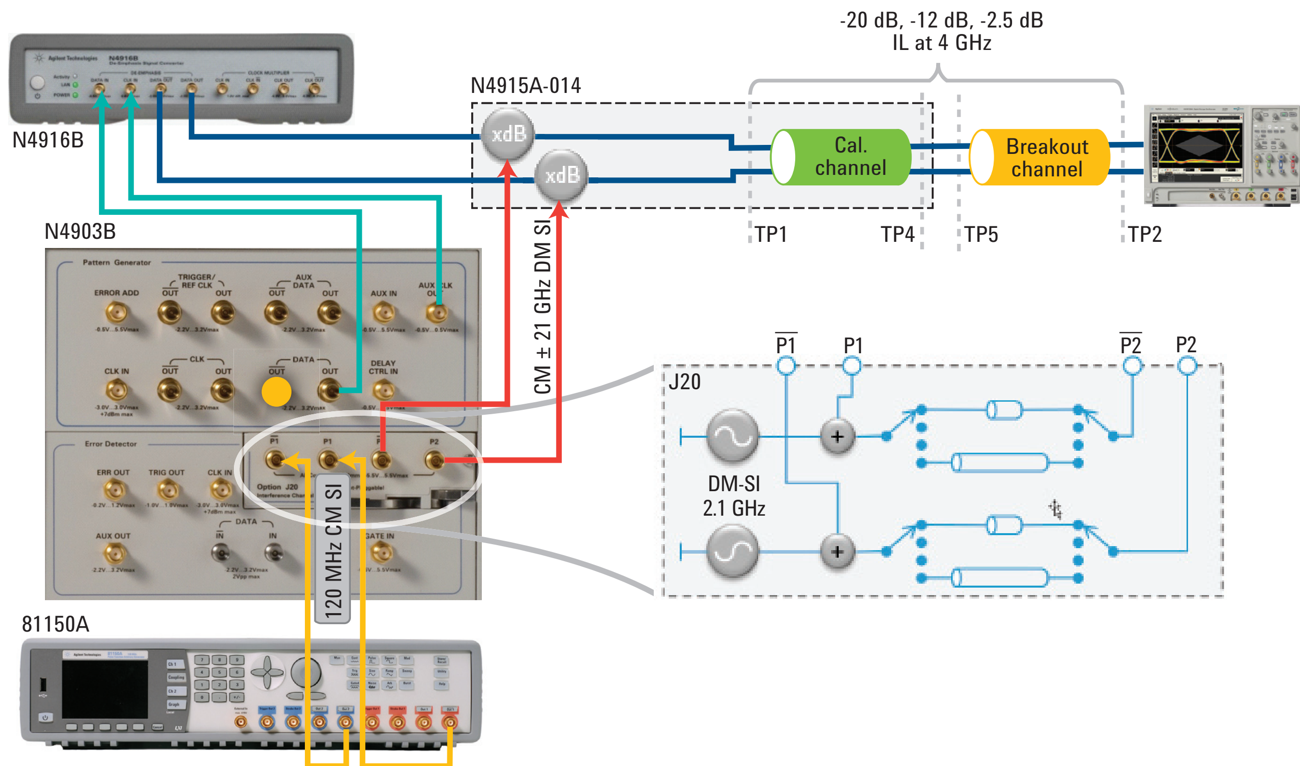


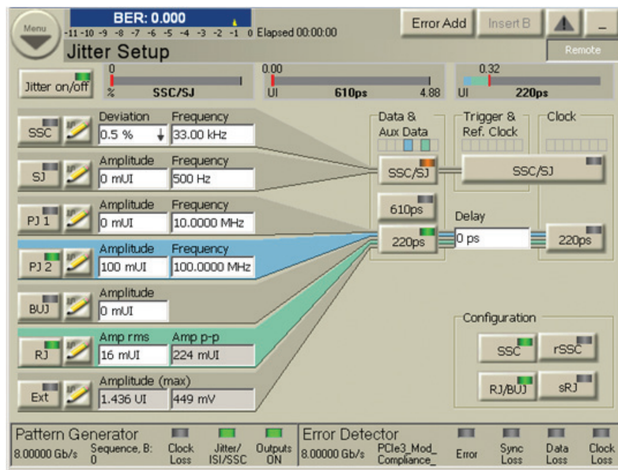
Figure 9. Test set-up for stressed voltage eye generation using the Agilent N4903B J-BERT, N4916B de-emphasis signal converter and N4915A option 014, calibration channels; lower right: simplified circuit diagram of option J20

7. *The loss of the PC-board traces inside the N4915-014 has deliberately been designed such that the desired total insertion loss of 9.5 dB and 17.5 dB (specified value w/o nominal loss of breakout-/replica channel) is achieved using relatively lossy cables between N4916B output and N4915A input and between TP4 and TP5. Should the set-up contain a switch for test automation, its higher loss can be compensated using lower loss cables.*
8. *Note that the data signal is not transmitted through the board traces of option J20, but through external traces specific for PCIe 3.0 instead (N4915A-014). Only the integrated adder and the DM-SI source of J20 are used in this set-up. Both sinusoidal signals are inevitably passing through (the shortest) interference channel. The resulting attenuation is calibrated during step 5 of Chapter 3.2.2.*

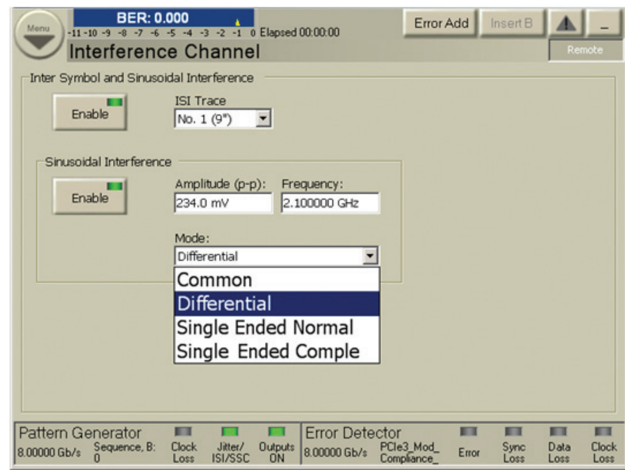
Figure 10 a–c shows how to set-up the impairments (jitter and DM-SI) on the Agilent J-BERT. Figure 10d shows how using its pattern sequencer simplifies the generation of the four different patterns required throughout the calibration and test procedure. Each pattern segment is looped until a break condition appears (either interactively, when the user presses the break button (encircled) or remotely when the break command is issued).

The four segments shown in Figure 10d are used for the following steps of the calibration and test procedure:

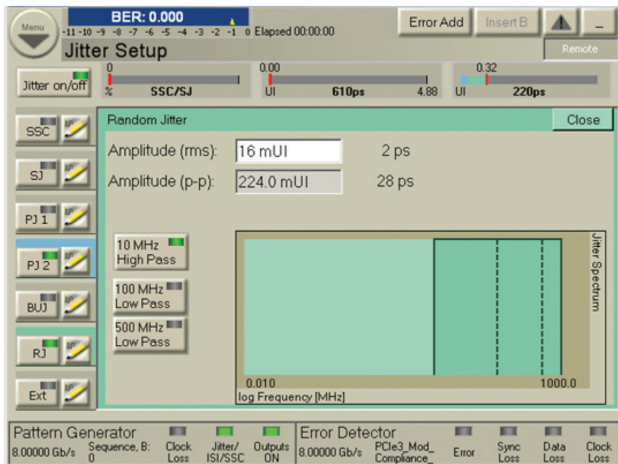
1. Measure "step response:" 128 x "1" and 128 x "0" = clock divided by 256
2. Calibrate DM- and CM- SI: data pattern = "0000" ((Pause0), constant output voltage. If no DC-blocks are used, additionally set amplitude to zero volts.
3. Calibrate jitter (if required at all): 1010-pattern = ½ rate clock
4. Perform the actual RX test: test pattern for BER measurement, modified compliance pattern



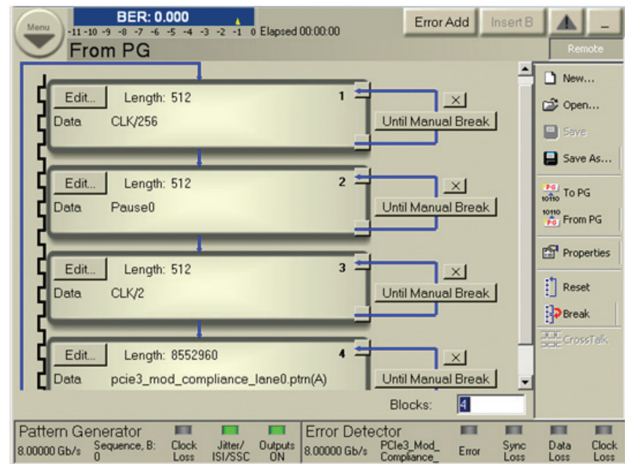
(10a)



(10b)



(10c)



(10d)

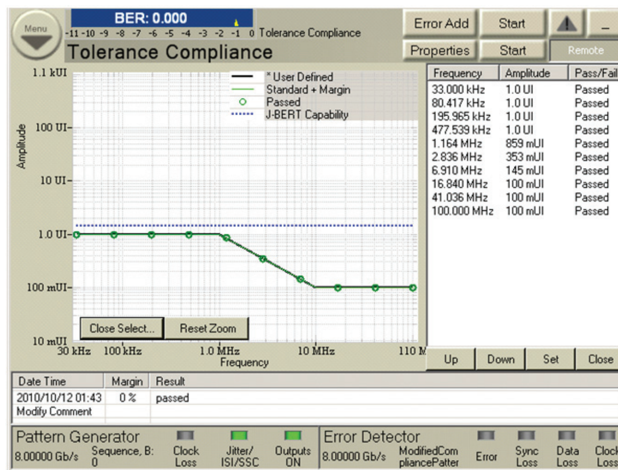
Figure 10. Screenshots from J-BERT-GUI showing set-up of: a) jitter cocktail for stressed jitter-eye (upper left), b) RJ of 3 ps$_{RMS}$ with specified 10 MHz high-pass filtering (both encircled) (upper right) c) DM-SI at 2.1 GHz (lower left) d) sequence editor with all patterns used for calibration (lower right)

The SJ sweeping required for stressed jitter test can easily be achieved using either the tolerance compliance measurement of J-BERT as shown in Figure 11 left, which delivers a pass/fail result for every jitter frequency step that was defined, or the variable amplitude sweep for PJ2 (Figure 11 right), which happens in the background.

Table 1 provides an overview of all jitter/interference requirements and the corresponding J-BERT capability.

Requirement	Solution
RJ 10 MHz to 1 GHz	N4903B, jitter setup, RJ with filtering
SJ 100 MHz	N4903B, jitter setup, PJ2
SJ "sweep" 33 kHz to 100 MHz	N4903B, "Tolerance Compliance" measurement or PJ2, variable amplitude sweep
DM-SI, 2.1 GHz	Option J20, DM-SI
CM-SI, 120 MHz	81150A
ISI	N4915-opt 001, calibration channels
Generator de-emphasis	N4916B de-emphasis signal converter

Table 1. List of required impairments and corresponding J-BERT solution



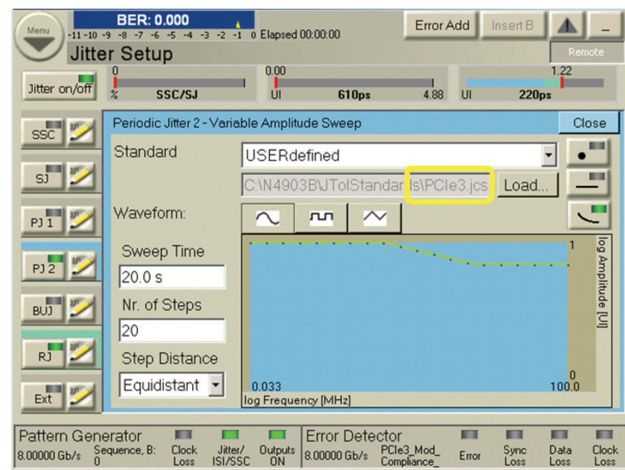


Figure 11. Tolerance compliance measurement (left) and background sweep of PJ2 (right)

5. Automation of Calibration Procedure with Agilent N5990A opt 101

Performing the described calibration procedure manually is time consuming and error prone. When finally achieved, only one point is calibrated. Using the N5990A opt 101 automation SW helps the user save time, increasing reliability and testing a wider variety of calibrated signal conditions.

Seasim is integrated and interaction between measurements and Seasim is provided.

Detailed description of the automation SW

The automation SW lets the user first check for a definable number (and range) of de-emphasis settings, if the insertion loss of the test set-up is within the specified tolerance band (see Figure 12). Next the recorded step response (with package model applied) will then be imported into Seasim.

Using Seasim, the automation SW calibrates the simulated amount of DM-SI or RJ vs the resulting eye opening (EH and EW) for the two different types of tests, stress voltage and stressed jitter (see Figure 13).

Furthermore, all signal parameters (signal amplitude, RJ, SJ, DM-SI, CM-SI) can be calibrated in-situ vs. instrument settings.

Having all of this data available enables the user to test the *compliance* of a DUT at the specified condition AND *characterize* its performance over *a wide range of parameter* settings.

Finally the user can run the RX test, either at the compliance or at any other previously calibrated point. The SW will program the connected test instruments' parameters accordingly, taking calibration data including the results from the S21 measurement into account.

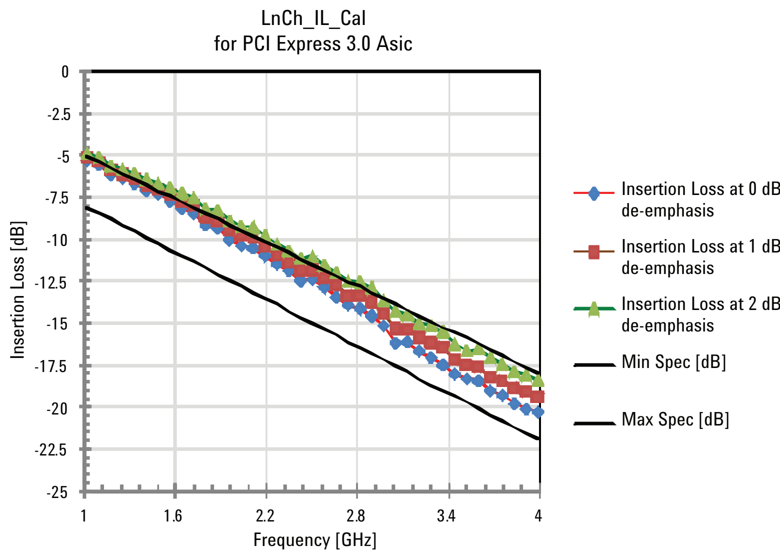


Figure 12. Insertion loss measurements with long calibration channel for three different settings of post-cursor de-emphasis

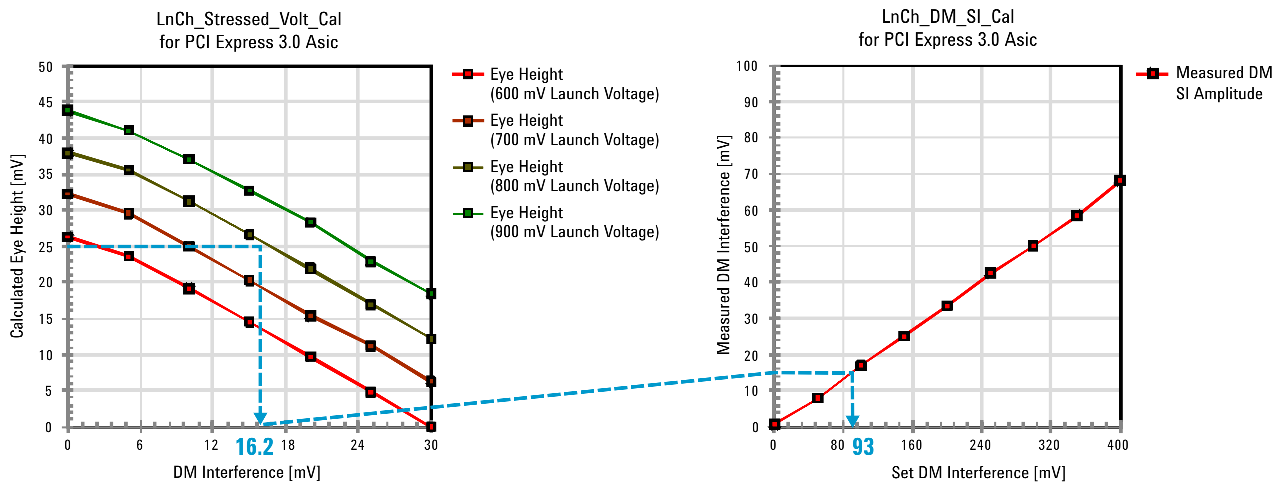


Figure 13. Calibration of (simulated) eye height vs. DM-SI (left) and actual DM-SI at TP2-P vs. setting on J-BERT (right); arrows show which setting of DM-SI on J-BERT is necessary to achieve desired EH of 25 mV

Summary Chapters 4 and 5

Agilent's accurate and repeatable PCIe 3.0 RX test solution as described in Chapters 4 and 5 provides:

- Pattern generator with
  - Injection of compliant RJ, SJ, SSC, DM-SI and de-emphasis
  - Pattern sequencer for simplified pattern switching and (modified) compliance pattern and PCIe 3.0-specific PRBS23
- PCIe 3.0 compliant calibration channels
- Automated and accurate stress calibration with Agilent RTO and RX test software

6. Summary

The RX is critical for error-free transmission in systems with transfer rates greater than 5 GT/s. Therefore, thorough RX testing is necessary, which requires well-calibrated stress-test signals for guaranteed interoperability. Specifying and measuring them can be challenging. The PCI electrical work group (EWG) recommends the construction of the test signal using a statistical simulation SW (Seasim) based on a measured step response. A suitable test set-up based on the Agilent J-BERT N4903B and automation of the calibration procedure is available with the N5990A option 101 automation SW.

7. Appendix

7.1. Equipment

The required instruments and accessories for building the setup according to Figure 9 are listed in Table 1.

Description	Number/Option	Qty
J-BERT high-performance serial BERT	N4903B	1
• 12.5 Gb/s BERT	C13	1
• AUX DATA output with PRBS and pattern	002	R[1]
• PJ, SJ, BUJ, RJ, s-RJ injection	J10	1
• SSC generation	J11	1
• Jitter tolerance compliance suite	J12	R[1]
• Interference channel (ISI, S.I.)	J20	1
• Bit recovery mode	A01	R[1]
De-emphasis signal converter	N4916B	1
• Matched cable kit for connecting N4916B with N4903B	N49156 option 010	1
PCIe 3.0 calibration channels	N4915 option 014	1
Digital signal analyzer with 13 GHz or higher bandwidth	DSAX91604A or higher	1
• Infinimax 12 GHz probe system	1169A	1
• Probe head for Infinimax II, 1160 series	N5380A	1
• SMA probe head support	N5380-64701	1
Test automation software platform core product	N5990A option 010	1
PCIe receiver test, includes Seasim software	N5990A option 101	1
Pulse function arbitrary noise generator	81150A option 002	1
Accessories		
• Coaxial cables, 3.5 mm, various lengths	N/A	10

R[1] Items not required to perform the basic measurements as described within this paper, but recommended because they will be very helpful during day-to-day work.

Table 2. Equipment for test setup according to Figure 9

7.2. PCIe 3.0, modified compliance pattern[9]

- Pattern consists of 256 sub-segments containing one "*control block*" followed by 256 "data blocks," as shown in Figure 14
  - first "*control block*" is EIEOS, which resets error counter and LFSR of scrambler
  - subsequent 255 "*control blocks*" consist of Skip Ordered Sets
  - all "data blocks" contain PCIe 3.0 specific PRBS-23 with different seeds/lane
- PRBS length:
  $128 \times 256 \times 256 = 2^7 \times 2^8 \times 2^8 = 2^{23}$
  PRBS is not truncated – fits exactly once (plus 1 bit)
- Total pattern length:
  130 x 257 x 256 = 8552960 = 16705 x 512 (fits into memory resolution of J-BERT)

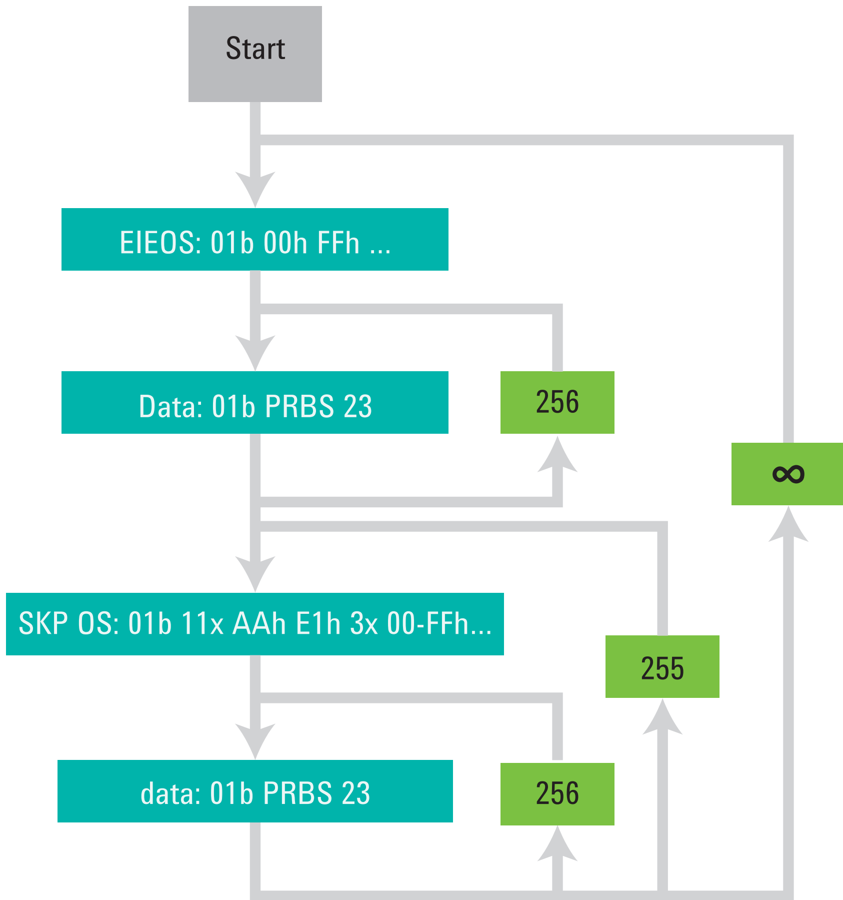


Figure 14. Modified compliance pattern as specified for RX test according to base spec rev 3

9. *SW rev 7.1 of N4903B delivers compliance- and modified compliance-pattern for TX and RX testing, as well as a PRBS-23-"P" with the PCIe 3.0 – specific polynomial*

7.3. Test setup and detailed specification for stressed voltage eye test

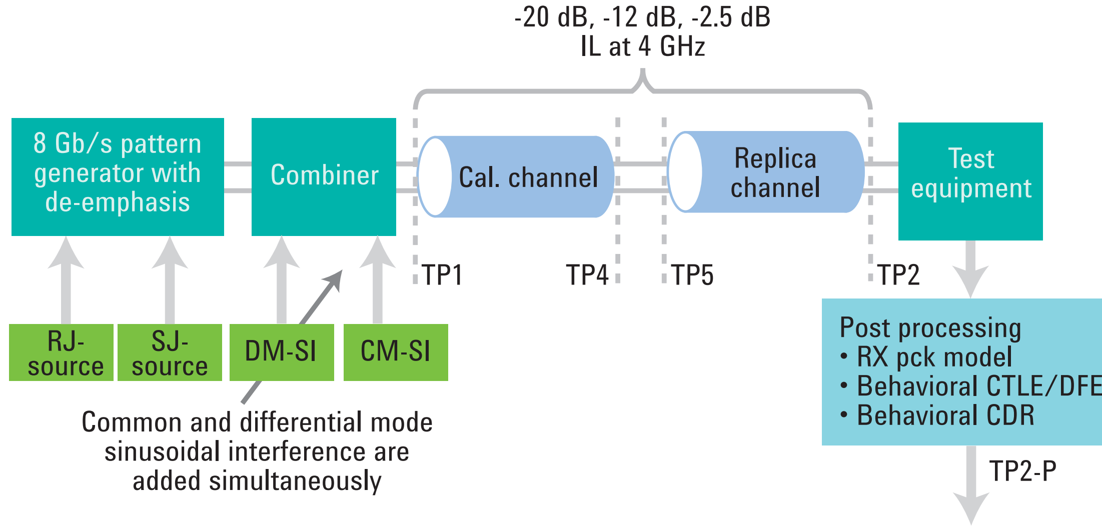


Figure 15. Test setup for stressed voltage eye test

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX\text{-}LAUNCH\text{-}8G}$	Generator launch voltage	800	mV_{PP}	Measured at TP1 Figure 3. $V_{RX\text{-}LAUNCH\text{-}8G}$ may be adjusted if necessary to yield the proper EH as long as the outside eye voltage at TP2 does not exceed 1300 mV_{PP}
$T_{RX\text{-}UI\text{-}8G}$	Unit interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC
$V_{RX\text{-}SV\text{-}8G}$	Eye height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mV_{PP}	Eye height @ BER = 10^{-12}
$T_{RX\text{-}SV\text{-}8G}$	Eye width at TP2P	0.3 to 0.35	UI	Eye width at BER = 10^{-12}
$V_{RX\text{-}SV\text{-}DIFF\text{-}8G}$	Differential mode interference	14 or greater	mV_{PP}	Adjusted to set EH; Frequency = 2.10 GHz
$V_{RX\text{-}SV\text{-}CM\text{-}8G}$	Rx AC common mode voltage at 120 MHz at TP2P	150 (EH < 100 mV_{PP}) 250 (EH ≥ 100 mV_{PP})	mV_{PP}	Defined for a single tone at 120 MHz
$T_{RX\text{-}SV\text{-}SJ\text{-}8G}$	Sinusoidal jitter at 100 MHz	0.1	UI_{PP}	Fixed at 100 MHz
$T_{RX\text{-}SV\text{-}\text{-}RJ\text{-}8G}$	Random jitter	2.0	ps_{RMS}	RJ spectrally flat before filtering

Table 3. Parameter limits

7.4. Test setup and detailed specification for stressed jitter eye test

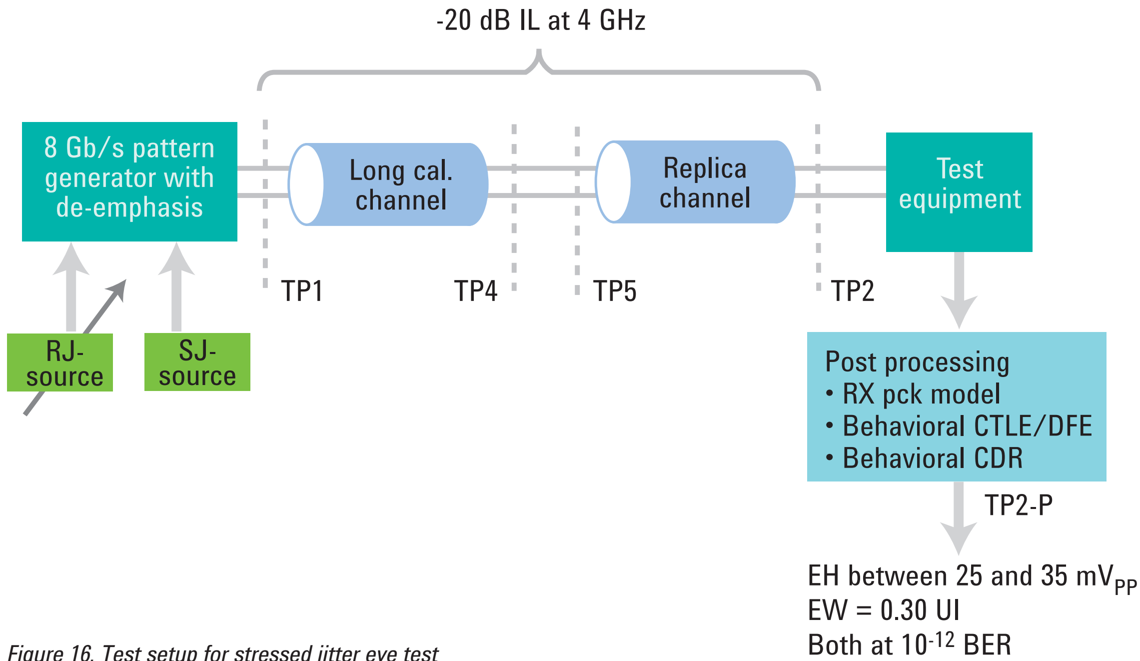


Figure 16. Test setup for stressed jitter eye test

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX\text{-}LAUNCH\text{-}8G}$	Generator launch voltage	800 (nominal)	mV_{PP}	Measured at TP1, see Figure 3
$T_{RX\text{-}UI\text{-}8G}$	Unit interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC
$V_{RX\text{-}SV\text{-}8G}$	Eye height at TP2P	25 (min) 35 (max)	mV_{PP}	At BER = 10^{-12}
$T_{RX\text{-}SV\text{-}8G}$	Eye width at TP2P	0.30	UI	At BER = 10^{-12}
$T_{RX\text{-}SV\text{-}SJ\text{-}8G}$	Sinusoidal jitter at 100 MHz	0.1 – 1.0	UI_{PP}	Measured at TP1, see Figure 11
$T_{RX\text{-}SV\text{-}RJ\text{-}8G}$	Random jitter	3.0	ps_{RMS}	RJ spectrally flat before filtering. Measured at TP1

Table 4. Parameter limits

7.5. Glossary

AIC	Add-in card
BER	Bit error ratio
BERT	Bit error ratio tester
CEM	Card electro-mechanical
CM-SI	Common mode sinusoidal interference
CR	Clock recovery
CTLE	Continuous time linear equalizer
DDJ	Data dependant jitter
DFE	Decision feedback equalizer
DM-SI	Differential mode sinusoidal interference
EH	Eye height
EIEOS	Electrical idle exit ordered set
EW	Eye-width
EWG	Electrical work group
ISI	Inter-symbol interference
LFSR	Linear feedback shift register
LTSSM	Link training and status state machine
PG	Pattern generator
RJ	Random jitter
RTO	Real time oscilloscopes
RX	Receiver
Seasim	Statistical eye analysis simulator
SEG	Serial enabling group
SJ	Sinusoidal jitter
TTC	Transition time converter
TX	Transmitter

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