Programming Micron P8P Parallel PCM Flash using Serial Peripheral Interface (SPI) on Agilent *Medalist* i3070 In-Circuit Tester

White Paper

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The Micron phase change memory (PCM) technology is a new generation of non volatile memory with the benefits of byte-alterability, or overwrite capability and one million write cycle endurance. The listed features deliver a flash memory solution that improves overall performance.
A secondary serial peripheral interface (SPI) has been added on Micron P8P PCM to enable low cost, low pin count on-board programming. This interface gives access to the P8P memory by using only seven signals, instead of a conventional parallel interface that may take 45 signals or more. The seven signals consist of six SPI-only signals plus one signal that is shared with the conventional interface.

Figure 1. PCM SPI Flash programming on Agilent Medalist i3070 in-circuit tester

When the SPI mode is enabled, all non-SPI P8P output signals are tri-stated, and all non-SPI P8P inputs signals are ignored (made "don't care"). When the conventional interface is enabled, the SPI-only output is tri-stated, and the SPI-only inputs are ignored (made "don't care").

Note: The SPI interface can only be enabled upon power-up, and to enable this interface, the SERIAL pin must be tied to VCC for the interface to be functional. Once the SPI interface is enabled, it is the only interface that can be accessed until the part is powered down.

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Table 1 shows the SPI pin out and description of a Micron P8P Parallel PCM flash device. The SPI Clock (C) determines the read and write synchronization speed of the data during SPI operation. The SPI data input (D) and SPI data output (Q) are the most important part of SPI as these pins carries the communication protocol wherein data can be transferred serially at the same time on both D and Q pins.

In order to generate the P8P PCM SPI flash test on Agilent *Medalist* i3070 ICT system, a digital library has to be setup which includes the pin assignment based on 56 leads TSOP package. The data in hex format can be converted by a contrib. script which breaks the data into two files. The address and the data content of the hex file are separated into two serial binary files.

The device also offers some new programming features which allow users to perform the programming operations more effectively. Details of these new programming modes can be found in Table 2.

Table 1. Micron P8P Parallel PCM Flash (56 lead TSOP) SPI pin description

Pin	Symbol	Description
30	S#	SPI Select: S# low activates command writes to the SPI interface. Rising S# to VIH completes (or terminates) the SPI command cycle; it also sets Q to high-Z.
32	HOLD#	SPI HOLD#: When asserted, suspends the current cycle and sets Q to high-Z until de-asserted.
45	C	SPI Clock: Synchronization clock for input and output data
46	D	SPI Data Input: Serial data input for Op Codes, address and program data bytes. Input data is clocked in on the rising edge of C, starting with the MSB.
56	Q	SPI Data Output: Serial data output for read data. Output data is clocked out, triggered by the falling edge of C, starting with the MSB.
27	SERIAL	SPI Enable: SERIAL is a port select switching between the normal parallel or serial interface. When Vss, the normal (non-SPI) Micron P8P PCM interface is enabled; all other SPI inputs are Don't Care, and Q is at High-Z. When Vcc, SPI mode is enabled, all non-SPI inputs are Don't Care, and all outputs are at High-Z. This pin has an internal weak pull down resistor to select the normal parallel interface when users leave the pin floating. A CAM can be used to permanently disable this feature.

Table 2. Micron P8P Parallel PCM SPI Instruction set

Instructions	Description	One Byte Instruction	Code	Address Bytes	Dummy Bytes	Data Bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
PP	Page program (Legacy)	0000 0010	02h	3	0	1 to 64
	Page program (Bit-alterable)	0010 0010	22h	3	0	1 to 64
	Page program (on all 1's)	1101 0001	D1h	3	0	1 to 64
SE	Sector Erase	1101 1000	D8h	3	0	0

One of the useful features is the Bit-Alterable programming mode which allows users to simply overwrite whatever data in the targeted memory address without needing to erase it to 0xFF first.

In most cases, the i3070 digital library for an SPI device uses the Address/Data block syntax to pass the programming data and addresses into the library. i3070 users whom have the Flash70 feature license may also choose to use the "FF" stripping command in the attempt to shorten the programming time. When using this command, the system assumes that the targeted device is blank (0xFF) and will only program those addresses in the data file that is not FF. In this case, all the address that has data "FF" will be skipped.

Therefore, if the user is using FF stripping or the Program on all 1's command, user needs to ensure that the device is fully blank before programming it. Else, there may be a possibility of some address holding the wrong data because it was skipped during the programming sequence.

Table 3. P8P PCM SPI Flash programming time on Agilent Medalist i3070 ICT

All timings in seconds	1 MB Data	16 MB Data
Program	3.98	30.9
Verify	2.157	33.08
Erase	1.3	15.9
Total	7.44	79.88

Agilent *Medalist* i3070 ICT system SPI serial flash programming using the hybrid card to drive signals to the PCM SPI Flash pins.

Too further increase the beat rate of the SPI flash programming to match the production beat rate, the following option can be implemented:

1. Agilent *Medalist* i3070 throughput multiplier
2. Agilent *Medalist* i3070 dual well
3. Agilent *Medalist* i3070 panel test

Below is the recommended Agilent *Medalist* i3070 hardware configuration to ensure best throughput.

1. ASRU N card
2. Control XTP card
3. Hybrid standard (6 MPS)/ Advanced (12 MPS) pin cards
4. Agilent *Medalist* i3070 08.00p software revision

Taking the data on table 3 for the P8P PCM flash device which is running at 1up single will then convert into a 2up dual well fixture the following test time can be achieved.

Table 4. P8P PCM SPI Flash programming throughput using different fixture type

All timings in seconds	1-up Single well fixture	2-up single well fixture	2-up dual well fixture
Program	30.9	15.45	15.45
Verify	33.08	16.54	16.54
Erase	15.9	7.92	7.92
Handling Time*	3	3	0
Total	82.88	42.91	39.91
Board tested per hr	44	84	90

**Note:* Handling time is based on the time the operator is changing the board to test from the fixture.

Design for Test (DFT) consideration:

It is important that proper DFT is done before doing P8P Parallel PCM programming using the Agilent *Medalist* i3070 ICT system.

Upstream disabling to prevent signal conflicts

The upstream device connected to P8P Parallel PCM should be properly disabled to avoid signal conflict that might cause potential damages to the device. Proper DFT or disabling upstream device will also ensure a stable programming test during In-circuit test.

In most applications of a memory device, the memory device is usually connected downstream of a Control IC. This is usually the case whereby the memory device is designed to store certain information which the controller IC requires. When power is applied on to the board, it will power on all the ICs on the board, including the Control IC and the memory device. The Control IC usually will attempt to access the memory device at this time and may force its signal to a certain state after power on.

Now if the i3070 tester is now trying to drive its own test patterns into the memory device, this will cause a signal contention scenario whereby the Control IC is trying to maintain a certain state on the signal but the i3070 tester is trying to drive it to the opposite state. This will result to unstable tests or even damaged devices.

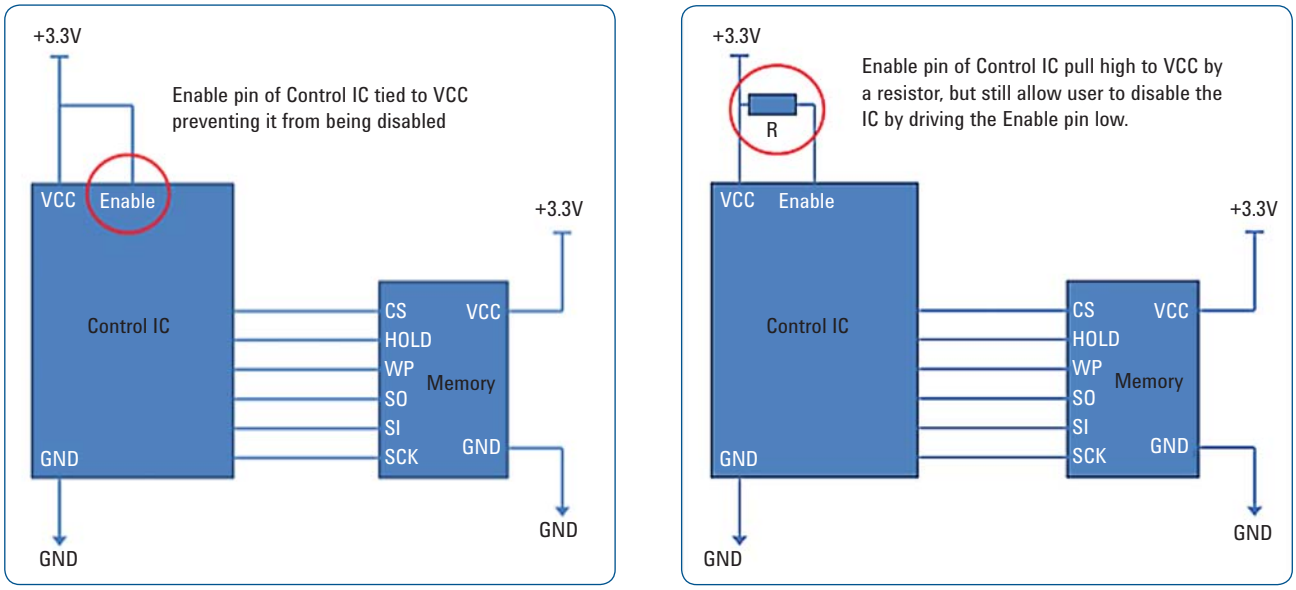

Figure 2. Upstream Disabling to prevent signal contention

Allow disabling of on board clock sources

During the execution of any digital test pattern, the presence of noise will affect the stability and could force the user to execute at a much slower pattern rate. Therefore, it is required to disable all possible noise sources on the board prior to any digital pattern executions. Potential sources of noise could be free-running clocks and or oscillators on the board. The free running clocks generated by these devices can cause signal contention with the digital test patterns run on the i3070 during test. The method of disabling is similar to that of an upstream device. Allowing user to be able to disable these devices will minimize the level of noise that may interfere with the programming patterns.

Ensuring signal integrity on fixture wiring

A critical node and twisted pair wire assignment on SPI pins during i3070 test development will help to ensure that short wire and twisted wire are assigned on SPI nodes in the fixture is used that will help reduce noise and ensure stability of the programming.

Reference

1. Micron P8P Parallel PCM datasheet from Micron– Released April 2010

2. Agilent *Medalist* i3070 ICT on line help – 08.00p

3. SMTA/TMAG Testability Guidelines TP-101D 2008

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