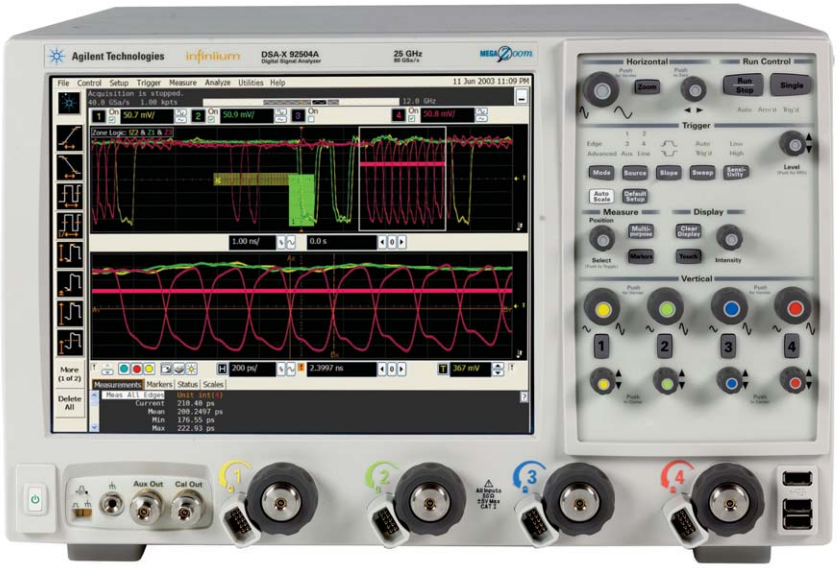
Making Accurate Measurements on GDDR5 Memory Systems

Application note

Who should read this application note?

Memory designers and test engineers working on high-speed GDDR5 memory buses will find the application note helpful.



Introduction

GDDR5 (Graphics Double Data Rate, version 5) is a high performance dynamic random-access graphics card memory designed for applications requiring high bandwidth. GDDR5 technology offers higher data rates (up to 4x that of GDDR4) which enables more bandwidth over a narrower memory interface for superior performance. GDDDR5 design innovations and challenges involve working with a reduced size chip, 170 FBGA packages and use of data optimization with data and address bit inversion to improve signal quality. This also reduces the supply noise induced jitter. GDDR5 also adopts jitter control technology which filters high frequency jitter and realigns clock phase when its input duty is distorted. The challenges in physical layer testing and validation requires a true analog bandwidth oscilloscope with low noise floor for making accurate jitter measurement at data rate of 5Gbits/s or higher. Like other DDR memory technology, one of the biggest challenges that many designers face is to separate the read and write cycles to make data eye diagram measurement. This article describes the latest GDDR5 measurement techniques and debug tools available for general troubleshooting purposes and compliance testing. It will focus on the areas in the specifications that require specific and unique capability of a true analog bandwidth oscilloscope.

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Accurate forward clock (WCK) jitter measurement with true analog bandwidth oscilloscope

The GDDR5 SGRAM operates from a differential clock CK and CK#. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of CK#. GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK/WCK#) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

One of the sources of jitter in a GDDR5 system is the random jitter on WCK to WCK(int) path where the jitter is filtered by a input delay and a clock tree. An analog oscilloscope is the tool of choice to measure the allowable random jitter on WCK input. The dual dirac model method is used to separate the random jitter component. There are two modes applied to the jitter measurement which is the PLL on and PLL off mode with clock data recovery (CDR) capability applied to DRAM reads.

Jitter is defined as the deviation of a signal transition from its ideal time. It closes the data valid window of the read and write data at high speed data rate which causes sampling error and higher bit error rate.

When operating at high date rate such as 5 Gb/s or higher, the data valid window is very small. The noise in the system or crosstalk from adjacent electrical signals or even electromagnetic interference could easily distort the signal integrity which could result in data sampling error. Hence, it is very important to note the performance of the measurement tool used to characterize the GDDR5 system. In this case, the margin of your system could easily be used up by the oscilloscope you use to measure the clock jitter of your GDDR5 system. The error contributed by the oscilloscope affects a great deal of measurement accuracy on your system. Noise and jitter contributed by the oscilloscope reduce the design margin that your system originally has. The system designers go through multiple cycles of engineering effort to maximize the system margin and it is important to use not only a high bandwidth oscilloscope that will support the high speed data rate, it is also key to have the a low noise oscilloscope to make the most accurate measurement to reduce design cycles and ultimately get to market faster.

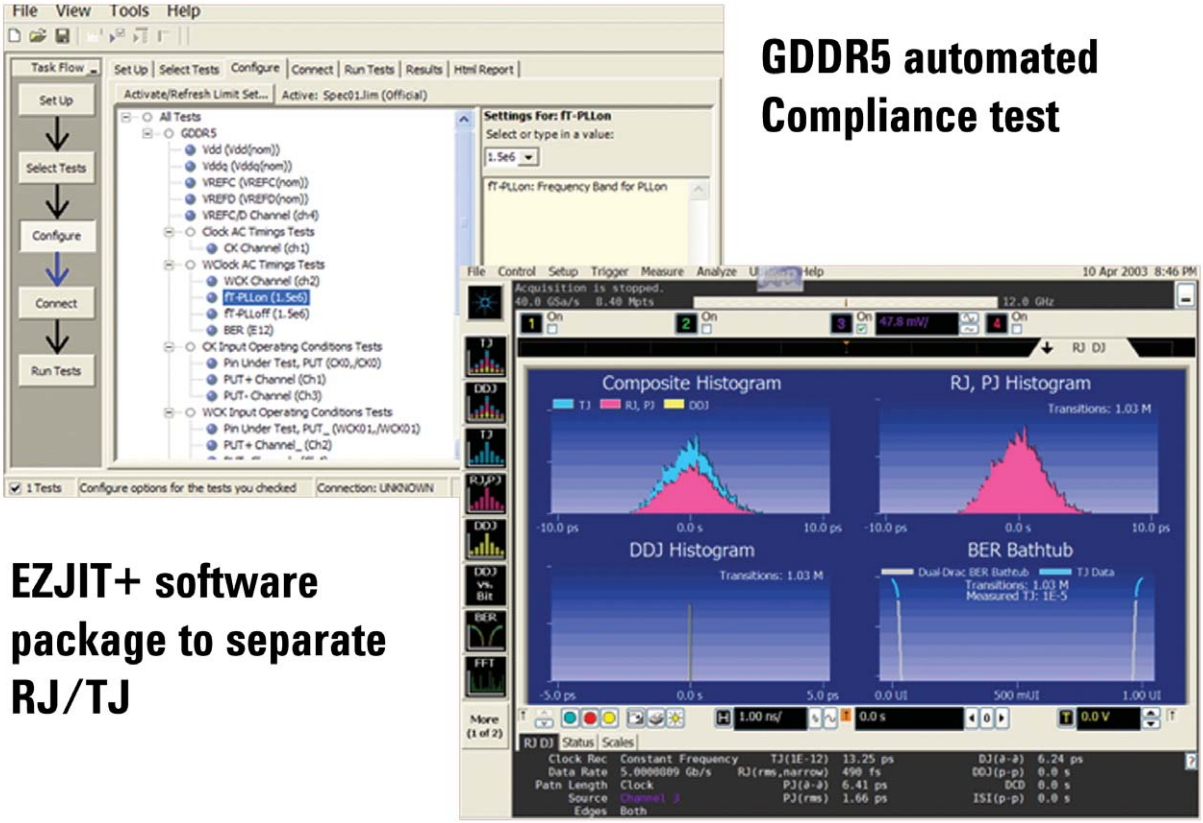


Figure 1: The 90000X series true analog bandwidth oscilloscope is a tool of choice to separate TJ/RJ measurement with an automated compliance test application with EZJIT+ jitter tool.

Read and Write data separation for eye diagram testing

Read and write data access to the GDDR5 SGRAM are burst oriented; an access starts at a selected location and consists of a total of eight data words. The state flow begins with an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising CK# edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK# edge are used to select the bank and the column location for the burst access. One of the key challenges that designers faced in memory device debug is separating read and write cycles for data eye diagram testing. In GDDR5, this step is necessary to measure the data valid window. One method to do this is to trigger on a valid command of read or write with a mixed signal oscilloscope. A mixed signal oscilloscope typically has 16 digital channels and 4 analog channels. The digital channels would be connected to CK (clock), RAS (row address), CAS (column address), WE (write enabled) and CS (chip select) buses on a GDDR5 device and the analog channel on the oscilloscope would be connected to DQ (data) to find the correspondent data associated with the read or write command. This method however is pretty tedious when it comes to trying to access a total of 6 signals on the GDDR5 device and especially when there is not enough board space for easy access.

Separate the read and write command with 4 channels of your true analog bandwidth oscilloscope

The most highly recommended way to separate read and write is with using Agilent's InfiniiScan+ tool. This unique tool allows you to trigger on a specific pattern with zone qualify trigger option. We can derive the following conditions from the GDDR5 command truth table:

- Read command: CAS# is low and WE# is high
- Write command: CAS# is low and WE# is low
- Load FIFO, Deselect, Refresh, Self Refresh, Power Down: CAS# = X (don't care), WE# = X

Operation	Symbol	CKE#		CS#	RAS#	CAS#	WE#
		Previous cycle	Current cycle				
DESELECT (NOP)	DES	L	X	H	X	X	X
NO OPERATION (NOP)	NOP	L	X	L	H	H	H
MODE REGISTER SET	MRS	L	L	L	L	L	L
ACTIVE (Select bank & activate row)	ACT	L	L	L	L	H	H
READ (Select bank and column, & start burst)	RD	L	L	L	H	L	H
READ with Autoprecharge	RDA	L	L	L	H	L	H
Load FIFO	LDFF	L	L	L	H	L	H
READ Training	RDTR	L	L	L	H	L	H
WRITE without Mask (Select bank and column, & start burst)	WOM	L	L	L	H	L	L
WRITE without Mask with Autoprecharge	WOMA	L	L	L	H	L	L
WRITE with single-byte mask	WSM	L	L	L	H	L	L
WRITE with single-byte mask with Autoprecharge	WSMA	L	L	L	H	L	L
WRITE with double-byte mask (WDM)	WDM	L	L	L	H	L	L
WRITE with double-byte mask with Autoprecharge	WDMA	L	L	L	H	L	L
WRITE Training	WRTR	L	L	L	H	L	L
PRECHARGE (Deactivate row in bank or banks)	PRE	L	L	L	L	H	L
PRECHARGE ALL	PREALL	L	L	L	L	H	L
REFRESH	REF	L	L	L	L	L	H
POWER DOWN ENTRY	PDE	L	H	H	X	X	X
				L	H	H	H
POWER DOWN EXIT	PDX	H	L	H	X	X	X
				L	H	H	H
SELF REFRESH ENTRY	SRE	L	H	L	L	L	H
SELF REFRESH EXIT	SRX	H	L	H	X	X	X
				L	H	H	H

Figure 2: GDDR5 command truth table

Here, you would connect CAS#, WE#, WCK and data (DQ) to the analog channels of the oscilloscopes. Clearly a mixed signal oscilloscope is not required because there're enough channels on a standard 4 channel analog oscilloscope. To separate a read from a write cycle, you would need to use hardware trigger on CAS# signal to find the first transition of CAS# from high to low state. Then, turn on InfiniiScan+ and draw the first trigger zone 1 on WE# signal to only trigger when WE# is high. This will omit any trigger on a write command. You can then place zone 2 and zone 3 of InfiniiScan+ on DQ after a certain read latency. Zone 2 and Zone 3 will also eliminate possibilities of triggering on a Load FIFO, Deselect, Refresh, Self Refresh, Power Down because during these command cycles, DQ is either high or in high impedance state.

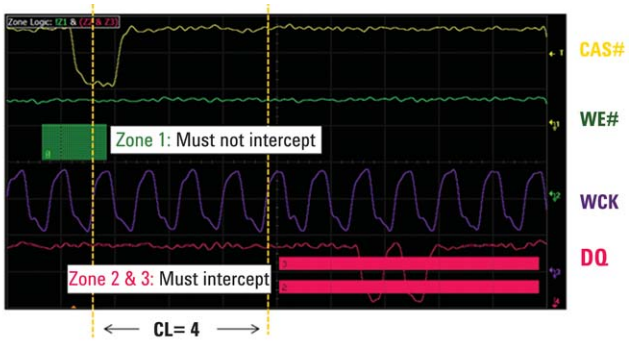


Figure 3: Separate Read command with InfiniiScan+ zone qualify trigger tool

To separate a write from a read cycle, use hardware trigger to trigger on CAS# transitioning from high to low state and then draw the first zone to trigger on WE# low. You can then place zone 2 and zone 3 of InfiniiScan+ on DQ after certain write latency value.

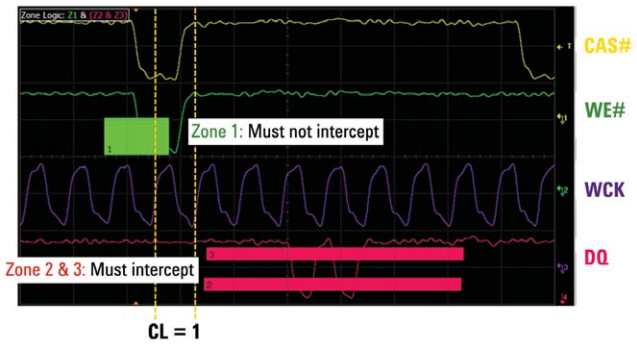


Figure 4: Separate Write command with InfiniiScan+ zone qualify trigger tool

A successful read or write command separation will allow you to make data valid window measurement. tDIVW in the JEDEC GDDR5 specification defines the time region when input data must be valid for reliable data capture at the receiver for one worst case channel. The measurement will include jitter between data and clock at the latching point. All other additional jitter added into the system before the DRAM pad will need to be measured in the final timing budget along with the PLL/DLL mode and bandwidth. A highest true analog bandwidth oscilloscope will ensure the most accurate representation of the fast edge. The lowest oscilloscope noise floor will get you the most representation of the voltage level for threshold placement and lastly the lowest real time oscilloscope jitter will allow you to maximize your jitter budget on your design and not the oscilloscope.

Write data separation with InfiniiScan

Write data eye diagram

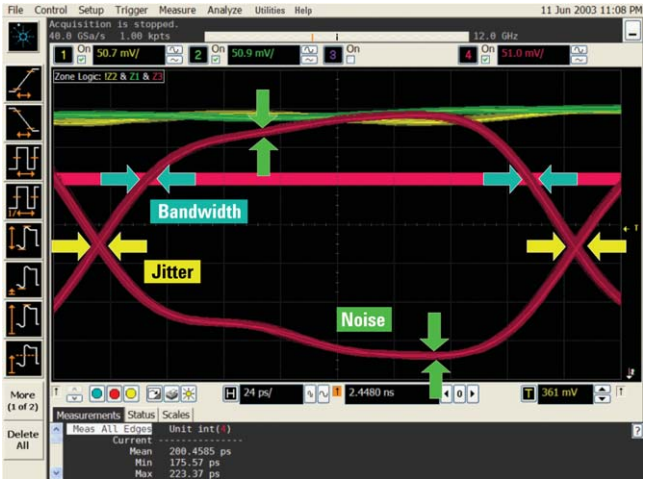


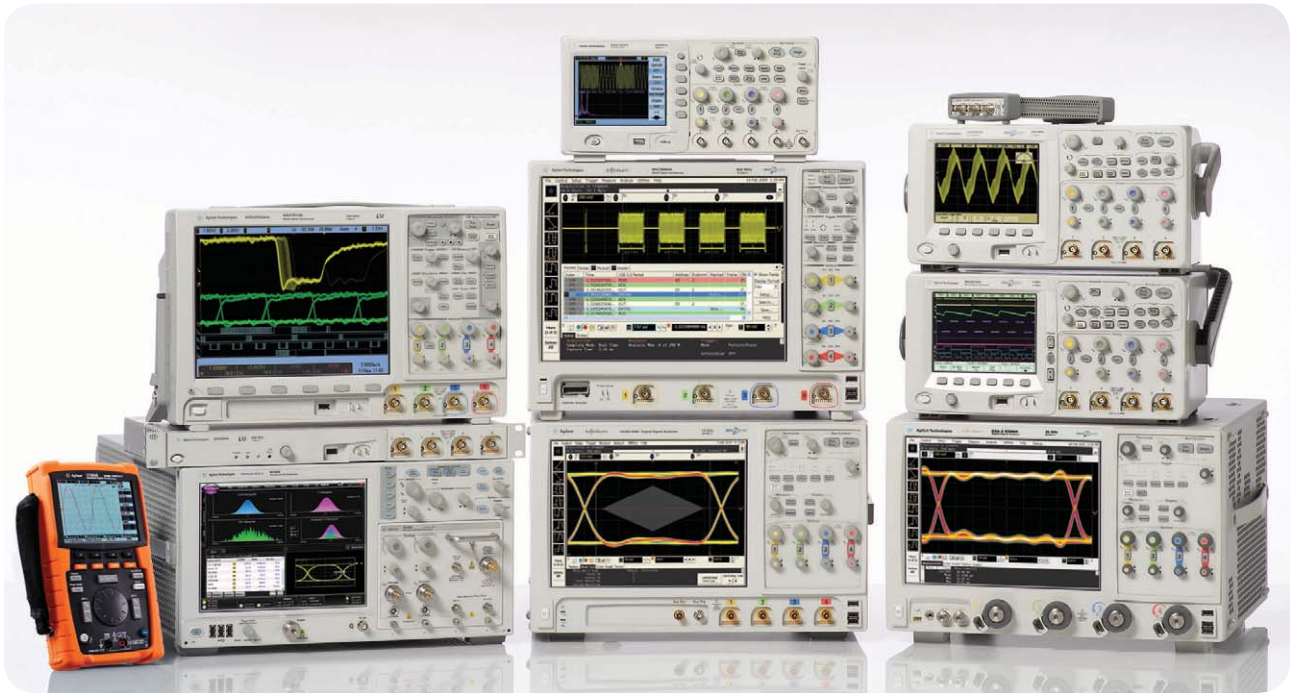
Figure 5: Write data eye diagram measurement after a successful write command separation with unique InfiniiScan+ trigger tool. Highest bandwidth, lowest noise floor and lowest real time oscilloscope jitter with the 90000X series oscilloscope opens up the eye for accurate data valid window measurement.

Summary

As GDDR5 technology reaches higher data rate of 5Gb/s or higher, the signal amplitude and data valid window becomes smaller. The measurement tool that you choose to characterize your system will have a significant impact of your measurement accuracy. How much margin you have on your GDDR5 design is very dependent on how much noise and jitter is your oscilloscope contributing to the design. Many engineers go through several design cycles to improve the margin of the design and this has high implication on efficiency and overall research and development cost. Hence, a true analog bandwidth scope with highest bandwidth, lowest noise floor and lowest jitter measurement floor is highly desirable to ensure higher design margin and faster design compliance for first to market release.

Related literature

Publication title	Publication type	Publication number
Infiniium 90000X Series Oscilloscopes	Data sheet	5990-5271EN



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