IEEE 1149.6 Standard Boundary Scan Testing on Agilent *Medalist* i3070 In Circuit Systems

White Paper

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Abtract:
This paper outlines the Boundary Scan test suite in the Agilent *Medalist* i3070 In-Circuit Test (ICT) system. It also introduces the latest advancements in Boundary Scan test capabilities on the Agilent *Medalist* i3070 ICT platform that supports the testing of IEEE 1149.6-compliant devices.

The World of High Speed Signals

Have you ever wondered how technology has advanced whenever you watch an online video or access a radio station over the internet, and you are able to enjoy both audio and visual quality comparable to those provided by your conventional television or radio sets? Have you talked to someone on the other side of the world using Internet Phone or chatted with someone using a webcam with crisp clarity?

These vast improvements in audio and visual quality for such web-based media are made possible with the use of high speed signals, using low voltage differential signaling (LVDS). LVDS usage is everywhere – from your computer motherboard right to the most sophisticated computer server which transmits and processes every single bit of data; or from helping to push your emails to letting you watch a program on your 42" HDTV LCD screen through your home cable broadband connection. All these are made possible with high speed LVDS which now support speeds of up to 10 Giga Hertz (GHz).

Just how fast is a GHz signal? A speed of 1 GHz means that there are about one billion events occurring in one second. Let's examine this analogy: Imagine a car running at 100km/hr. That means it will take you 1 hour to reach a 100-kilometer distance between point A and point B. If we use 100 km/hr on our computer technology today, it will take 6 days for an email sent from Singapore to reach its intended recipient in New York!

As high-speed LVDS usage proliferates into high volume electronics products, millions of printed circuit board assemblies (PCBA) will be manufactured daily, creating a dilemma for test engineers on how they can effectively conduct in-circuit test in the high volume environment. Testing PCBAs for manufacturing defect at GHz speed will be complicated or next to impossible as current in-circuit test speed is only 6Mega hertz (Mhz).

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Catching Up with Testing Needs

Currently, the most viable ICT option in testing LVDS on the manufacturing floor is by using Boundary Scan test (Figu 1) for testing digital devices commonly conforming to the IEEE 1149.1 Boundary Scan standard.

During Boundary Scan, the output boundary cell will drive a single-ended DC signal, which will be received by another device with a receiver boundary cell connected to it. (See Figure 2).

In the IEEE 1149.1 Boundary Scan interconnect test, the connection between device pins are tested without the need for a test probe for each connection (see Figure 3), enabling a reduction in the number of test probes needed. This helps to overcome test access challenges caused by shrinking geometry of PCBAs, which limits the number of access points to test all the devices in the PCBA.

The propagation of high speed signals has prevented board designers from putting test points on a PCB due to loss in signal integrity. Again, the 1149.1 Boundary Scan interconnect test helps overcome this challenge.

Implementation of IEEE 1149.1 Boundary Scan test on In Circuit Test (ICT) is one of the important capabilities that enables Boundary Scan testing on a high volume ICT testing. The Agilent Medalist i3070 Boundary Scan suite has the following test capabilities:

- Powered Short Test
- Bus Wire Test
- Connect Test

These capabilities provide greater Boundary Scan test coverage which conventional ICT systems and stand alone Boundary Scan tools cannot achieve.

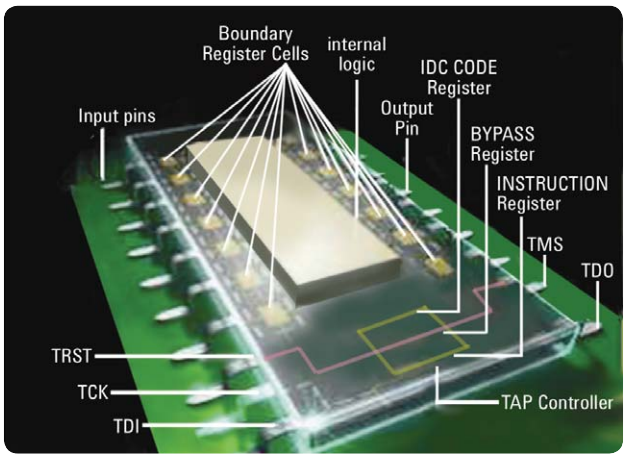

Figure 1. A boundary scan device

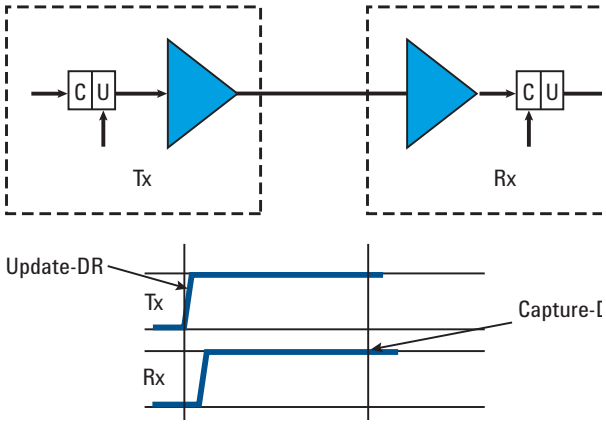

Figure 2. Typical 1149.1 output and input boundary scan cell connection.

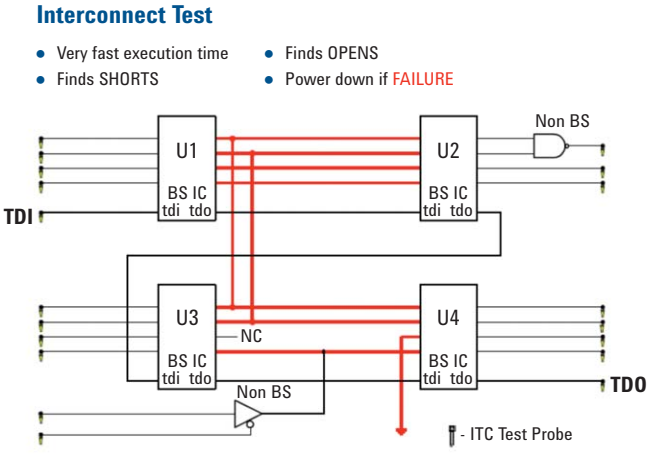

Figure 3. Interconnect Test checks connections for most shorts and some opens within the chain.

Powered Short Test

In the Agilent *Medalist* i3070 Powered Short Test, the Boundary Scan cell on device pins without test probes can detect a possible short on adjacent pins of a device with test probes (see figure 4) . In the Agilent Powered Shorts Test generation, the data from the board component x,y location of the devices pins is captured to determine the relative adjacencies for each device pins. The adjacencies are automatically identified by the Agilent *Medalist* i3070 test development software, which then generate a Powered short test which lists devices pins possible shorts occurrence with respect to the Boundary Scan nodes.

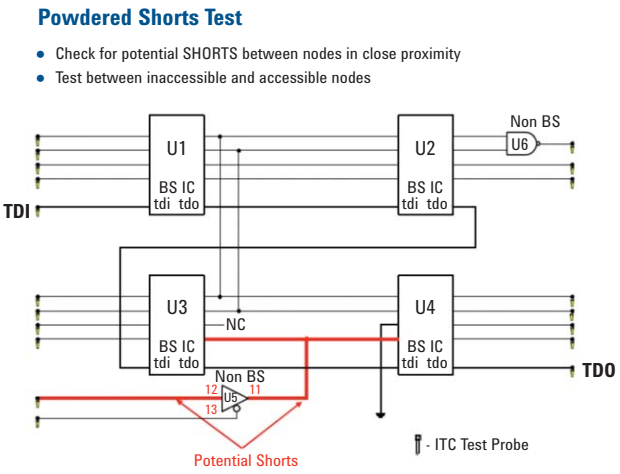

Figure 4. Agilent's Powered Shorts test checks for shorts between boundary-scan nodes without test probe and any nearby non Boundary Scan node with test probes.

Bus Wire Test

The Agilent *Medalist* i3070 provides additional coverage in the form of the Bus Wire Test which detects opens on bussed devices p'ins. Device pin shorts are not a concern because these would have been tested for by the shorts, powered shorts, and interconnect tests, which are executed earlier than the Bus Wire Test. In Bus wire test. The Boundary Scan drivers for devices are tested one at a time to ensure that all possible situations for which opens could occur are tested (see Figure 5).

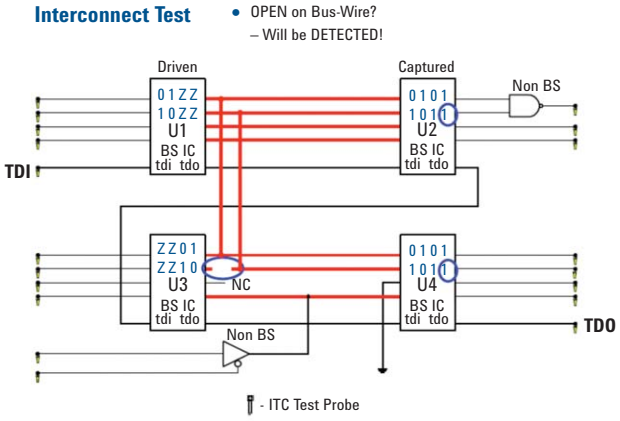

Figure 5. Bus Wire Test verifies connections on bussed nodes.

Connect Test

The Connect Test allows you to test for opens on the inputs and outputs pins of the Boundary Scan cell device that have physical test probes assigned to them. Shorts between pins with testhead access are detected by the unpowered shorts test. Connect Tests are run sequentially, from the first device in the chain (u1) to the last device in the chain (u4) until all devices have been tested. (see Figure 6)

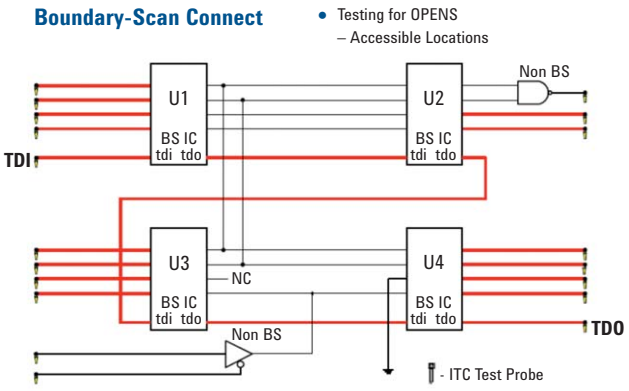

Figure 6. Connect Test checks the connections of each device in a chain.

Testing High Speed LVDS

The proliferation of High Speed LVDS in today's PCBA designs has put a limitation to the current standard IEEE 1149.1 Boundary Scan test. The current IEEE 1149.1 standard will not be able to provide coverage for differential signals due to the presence of a capacitor which is commonly known as AC differential signals (See figure 7). The presence of the capacitor on the differential signal blocks the Boundary Scan DC signal from reaching the Boundary Scan cell receiver, hence preventing it from detecting the presence of the DC signal which will result in its inability to detect manufacturing defects such as shorts and opens during testing.

The limitations of the IEEE 1149.1 Boundary Scan in testing AC differential signals led to the creation of the IEEE 1149.6 Standard – a milestone for Boundary Scan testing of advanced digital networks to cover AC differential testing.

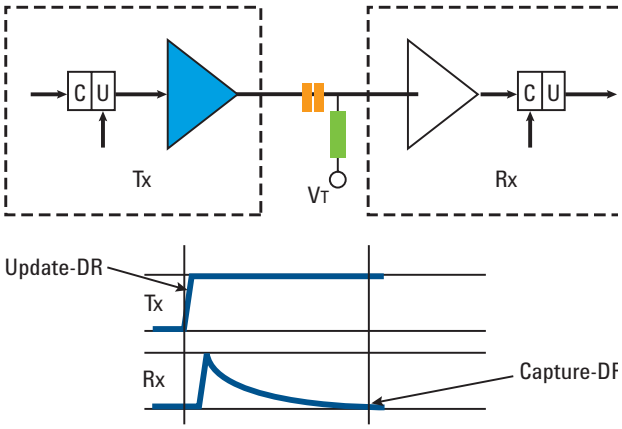

Figure 7. Differential Signal with AC coupling.

The Agilent *Medalist* i3070 Boundary Scan test suite supports both the IEEE 1149.6 standards with the following tests:

- Interconnect Test
- Shorted Capacitor Test
- Powered Short Test
- Bus Wire Test
- Connect Test (Differential DC coverage only)

Interconnect Test

The Agilent *Medalist* i3070 Interconnect Test covers the following devices (see fig 8):

- 1149.6 Boundary Scan cell connected to another 1149.6 Boundary Scan cell with or without AC differential coupling
- 1149.6 Boundary Scan cell connection to 1149.1 Boundary Scan cell with DC differential coupling.

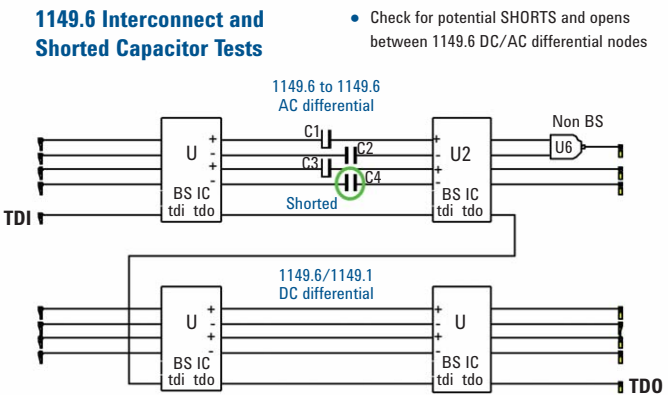

Figure 8. Agilent Medalist i3070 interconnect test and shorted capacitor test on 1149.6 DC/AC differential signals.

Shorted Capacitor Test

To enhance the Interconnect Test implementation, Agilent introduced the Shorted Capacitor Test in between 1149.6 Boundary Scan cell (See Figure 8). This is an important development for 1149.6 Boundary Scan implementation since no test coverage are available at In Circuit testing to detect the occurrence of any shorted capacitor in between the differential signals due to the absence of test access to this nodes.

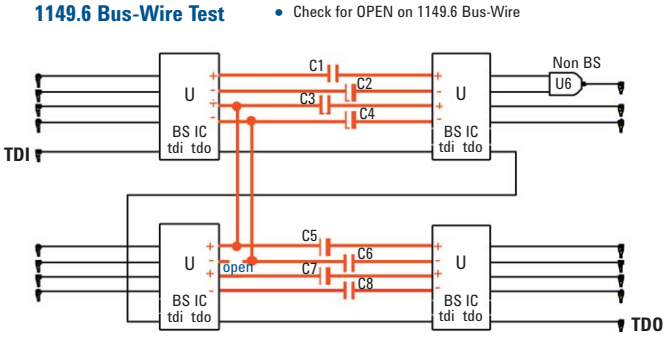

Figure 9. Agilent Medalist i3070 Bus wire test on 1149.6 DC/AC differential signals.

Bus Wire & Powered Short Test

The Bus Wire Test checks for opens on bussed differential signals (See figure 9) while the Powered Short Test detects possible shorts in the differential signals between a non accessible Boundary Scan cell and a non Boundary Scan cell with physical test probes. (See figure 10).

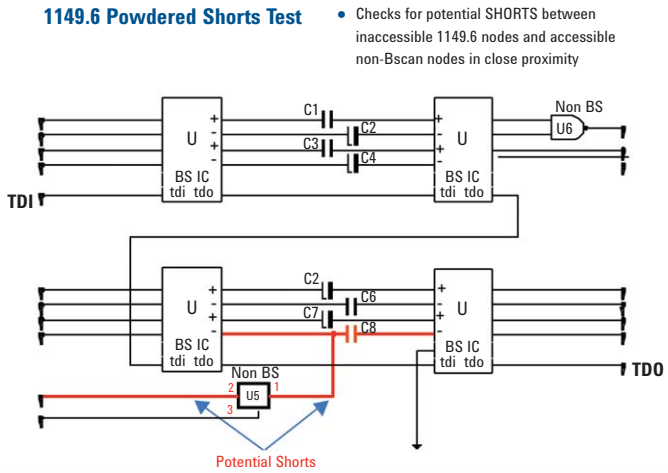

Figure 10. Agilent Medalist i3070 Powered short test on 1149.6 DC/AC differential signals.

Connect Test for DC Differential Signals

The last important coverage tool in the Agilent *Medalist* i3070 Boundary Scan suite is the inclusion of the 1149.1/1149.6 DC differential signals test which checks for opens on a 1149.1/1149.6 differential signals connection with test probes (see figure 11).

The 1149.6/1149.1 Connect Test currently does not include coverage on pins that have AC couplings. However, the following Agilent *Medalist* i3070 test strategy can be implemented to regain the lost coverage (see Figure 12).

The actual LVDS applications consist of the Transmit signal pair (positive and negative) as well as the Receive signal pair which normally terminate on a backplane connector. The *Medalist* i3070 software will be able to generate Boundary Scan interconnect tests by changing the component connection between the connector pins transmit (Tx) and Receive (Rx) pin in the board file information. Then during the actual testing a loop-back connector inserted on the backplane connector (see figure 12) will enable the Boundary Scan coverage on 1149.6 interconnect test where connect test was not able to test.

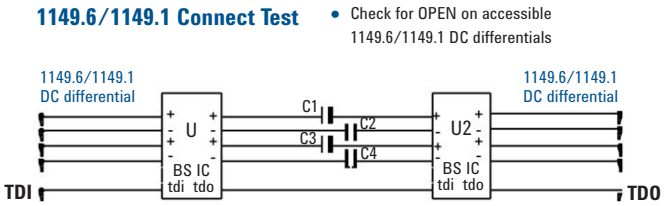

Figure 11. Agilent Medalist i3070 connect test on 1149.6/1149.1 DC differential only.

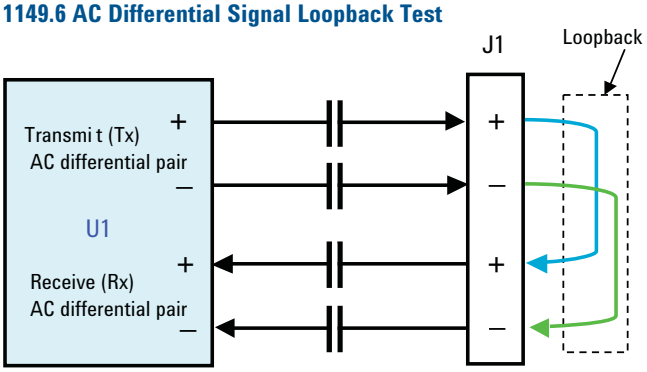

Figure 12. 1149.6 AC Differential Loopback testing

Conclusion

The Agilent *Medalist* i3070 Software Release 07.20p enhances support for the IEEE standard 1149.6 for Boundary Scan testing which now includes interconnect test, shorted capacitor test, Bus wire and Powered short testing of the 1149.6 AC-Coupled differential nets. This allows additional test coverage for many devices in today's printed circuit board assemblies.

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