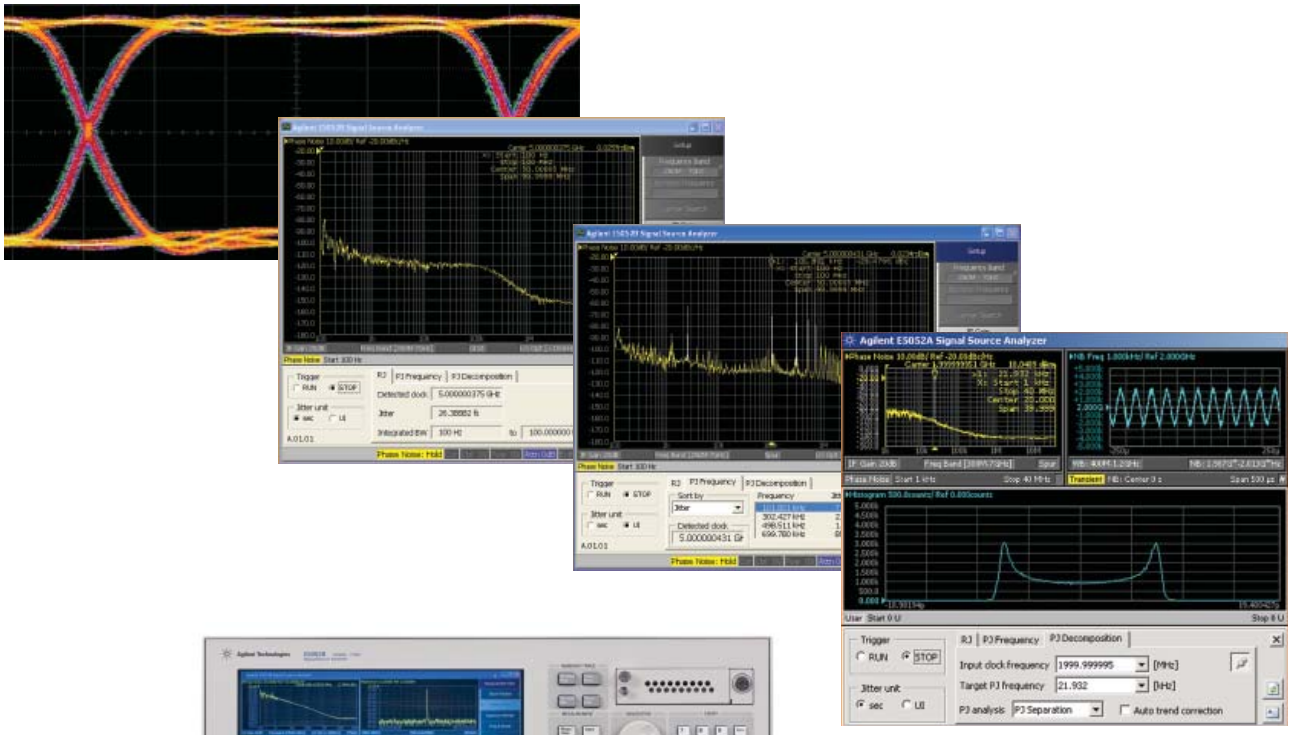
Accelerate Design Verification by Characterizing Clock Jitter Using Phase Noise Measurements

White Paper



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Introduction

Clock jitter analysis has become more necessary as data rates have increased. In high-speed serial data links clock jitter affects data jitter at the transmitter, in the transmission line, and at the receiver. Measurements of clock quality assurance have also evolved; now the emphasis is on directly relating clock performance to system performance in terms of the bit error ratio (BER).

This white paper reviews the role of the reference clock, the effect of clock jitter on data jitter, and discusses a new measurement technique using the Agilent E5001A precision clock jitter analysis application on the E5052B signal source analyzer (SSA). This new method of measurement delivers unprecedented measurement accuracy for ultra-low random jitter (RJ) measurements and real-time jitter spectrum analysis on both the RJ and periodic jitter (PJ) of components, enabling you to improve your design quality.

A real-time measurement capability of the new solution that speeds up your design verification process is also discussed.

The role of reference clocks in high-speed serial applications

Figure 1 shows the major components of a high-speed serial data link. The transmitter usually serializes a set of lower rate parallel signals into a serial data stream. The transmission channel through which the signal propagates is a combination of backplanes and cables. The receiver interprets incoming serial data, re-clocks it and, usually, de-serializes it back into a parallel data stream. In many high-speed serial communication systems, the reference clock is considered more of a constituent than a key player, but in high-speed serial data systems where system bit-rate can be in the multi-gigabit range, the reference clock becomes a key component. Typically the reference clock oscillates at a rate much lower than the data rate and is multiplied up in the transmitter. The transmitter uses the reference clock to define the timing of logic transitions in the serial data stream. The character of the reference clock is included in the data transmitted. At the receiver, two different things can happen. If the reference clock is not distributed, then the receiver recovers a clock from the data stream – using, for example, a phase locked loop (PLL) – and uses that clock to position the sampling point in time. If the reference clock is distributed, then the receiver uses both the data signal and the reference clock to position the sampling point.

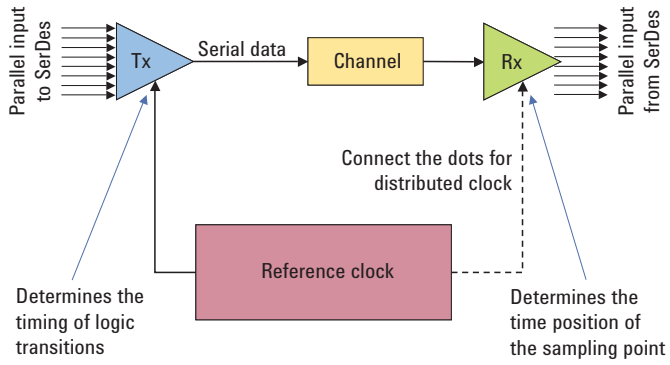

Figure 1. Role of the reference clock

Effects of clock jitter on data jitter from the transmitter

The reference clock is the ultimate source of system timing. It provides the time base for the transmitter and, in both distributed and undistributed clock systems, the character of the reference clock is reproduced in the clock recovery circuit at the receiver. Now, we'll examine how the clock jitter is propagated in the transmitter of the system.

To define the timing of logic transitions, the transmitter must multiply the reference clock by an appropriate factor to get the data rate. For example, for a 100 MHz reference clock and a 5 Gb/s output signal, the transmitter would use a PLL to multiply the reference clock by a factor of fifty. The PLL multiplier both amplifies the jitter on the clock and introduces its own jitter, primarily RJ from the PLL voltage controlled oscillator (VCO). The effect of frequency multiplication by a factor of n is to multiply the phase noise power to the carrier ratio by n^2, so the jitter rate goes up fast.

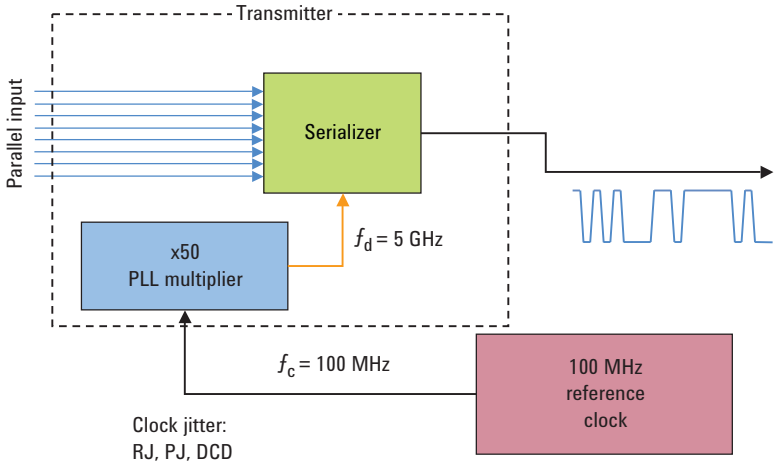

Figure 2. Effect of clock jitter on transmitter

The PLL multiplier in the transmitter has a certain frequency response, typically a second order response as shown in Figure 3. The non-uniform frequency response raises an interesting question: What clock-jitter actually matters? If the PLL were perfect and had zero bandwidth, then it would filter out all the clock jitter and provide the transmitter with a jitter-free time-base. Of course, zero bandwidth means infinite lock time, so we have to compromise, but the narrower the PLL bandwidth, the less jitter from the reference clock makes it into the data. Determining whether or not a clock will function in a system at the desired BER requires careful testing of the jitter frequency spectrum.

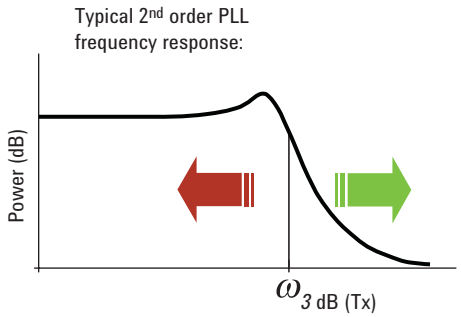

Figure 3. PLL frequency response

Jitter sources in the real world

If you look at a high-speed digital circuit in the real world, there are many jitter sources, as shown in Figure 4. As we reviewed previously, the clock signal is often distributed to multiple ICs and the clock frequency may be multiplied and/or divided. Even assuming that the reference clock coming from a crystal oscillator has low jitter, the output clock when multiplied or divided may be not clean due to the additive noise of ICs or interference from other devices.

One of the major contamination sources is the noise coming from switching power supply whose switching frequency is typically between 100 kHz and 1 MHz. The switching power supply noise may be injected into the clock signal line and it is observed as PJ, shown in the left bottom graph of Figure 4.

Other periodic jitter sources may be interferences from data or clock lines, or inter-modulation products that fall into the clock line. (See Figure 4.) As long as PJ components appear far away from the clock frequency, it is practically possible to insert a band-pass filter (or a low-pass filter) to suppress them. However, it is a problem when periodic jitter falls close to clock frequency because high-Q filters at high frequencies are not very available. Also, a clock divider can add broadband noise to the reference clock which could result in increased RJ of the output clock signal.

When diagnosing problems, you should characterize clock jitter on the physical layout of the circuit and/or under the operating conditions.

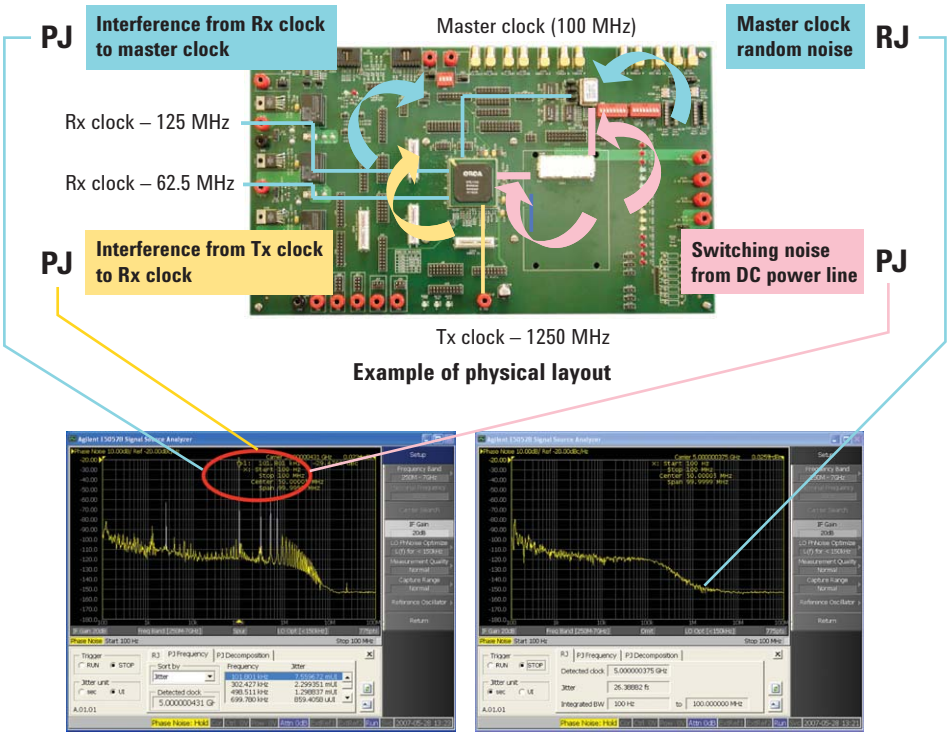

Figure 4. Jitter sources in the real world

Characterizing clock jitter using the phase noise measurement technique

Thorough analysis of a clock signal requires femto second accuracy which can only be achieved using a phase noise measurement technique. Phase noise analysis provides two key measurements, phase spectral density, $S\varphi$, ($f\varphi$), and phase noise, $\varphi(t)$, which harbor all the phase information of the clock up to the limit of the phase noise measurement bandwidth.

Two important goals can be achieved by analyzing RJ on a phase noise analyzer. First, by integrating the RJ spectrum, the width of the corresponding RJ Gaussian distribution is extracted within the bandwidth of interest. Second, the major causes of RJ can be isolated by analyzing the power-series behavior of $S\varphi$, ($f\varphi$). (See Figure 5.)

PJ components are observed as spurs on the phase noise spectrum. Knowledge of the PJ components in frequency is a terrific help in diagnosing problems. Referring a PJ rms of each PJ component in frequency will also help you understand the contribution of each PJ component to the total clock jitter allowing you to determine what part of the total jitter has become a major PJ component and needs to be removed. (See Figure 6.)

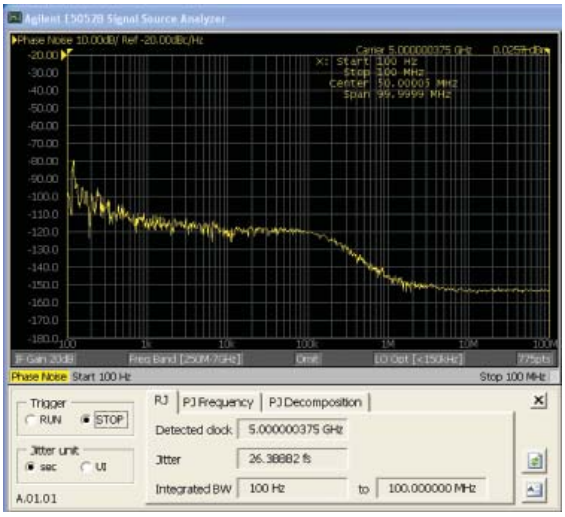

Figure 5. Analyzing RJ on a phase noise measurement

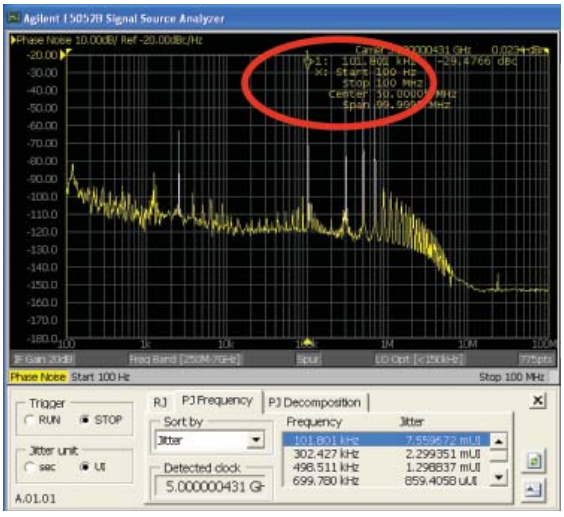

Figure 6. PJ components in frequency on a phase noise measurement

Real-time jitter measurement using the advanced architecture of the E5052B SSA

Unlike the traditional jitter measurement paradigm, the E5052B SSA with the E5001A software offers real-time jitter analysis of phase-noise measurements. The instrument employs PLL using a reference source method. It automatically detects the clock frequency and tunes a built-in reference source to the clock frequency in just a few milliseconds, and then it measures the noise signal coming out of the phase detector while maintaining PLL. The noise signals are captured at 250 MSa/s with an analog-to-digital converter (ADC) enabling up to 100 MHz jitter bandwidth measurements, and real-time fast-Fourier transformation (FFT) for obtaining frequency domain data; this dramatically improves the speed of the measurement. For example, it takes only 0.3 second per measurement from 1 kHz to 100 MHz bandwidth.

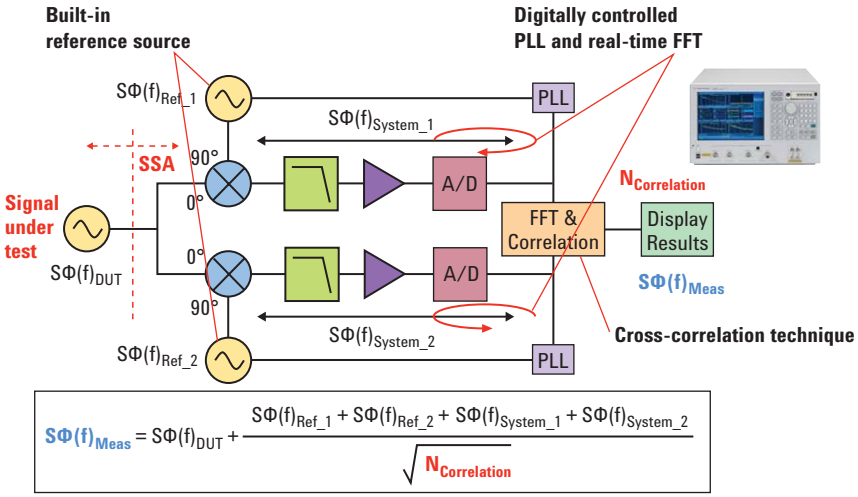

Figure 7. Advanced architecture of Agilent E5052B signal source analyzer

Unprecedented low jitter noise floor with cross-correlation technique

The E5052B jitter-measurement resolution and noise floor are exceptionally low, typically on the order of a few femto-seconds of RJ noise floor at a 10 Gbps rate. A typical high-performance (real-time or sampling) oscilloscope has a jitter noise-floor above one hundred femto-seconds due to the limited dynamic range of the ADC and the relatively large residual jitter of its internal reference time base. The E5052B has a quiet time base and maintains wide dynamic range by detecting phase noise at baseband where a large carrier signal is cancelled out. The E5052B SSA can extend the jitter measurement limit to below the residual jitter of its internal time base by using a unique cross-correlation technique between two independent internal measurement channels. (See Figure 7.) Using this cross-correlation technique, the E5052B achieves 100 to 1,000 times lower jitter noise floor compared to today's high performance oscilloscopes. (See Figure 8.)

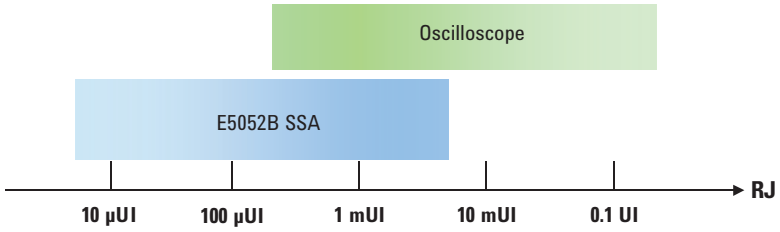

Figure 8. Ultimate jitter noise floor with cross-correlation technique

Emulate PLL response in real-time

Figure 9 shows an example of the effect of a PLL response function applied directly to the phase noise signal of a reference clock. You can see how different parts of the spectra are suppressed; this allows you to analyze the jitter transfer function relevant to the application. The E5052B's real-time jitter analysis of phase noise measurements speeds up your design process. Any PLL response functions can be imported to the E5052B SSA enabling you to emulate the jitter transfer function from device to device very easily and quickly.

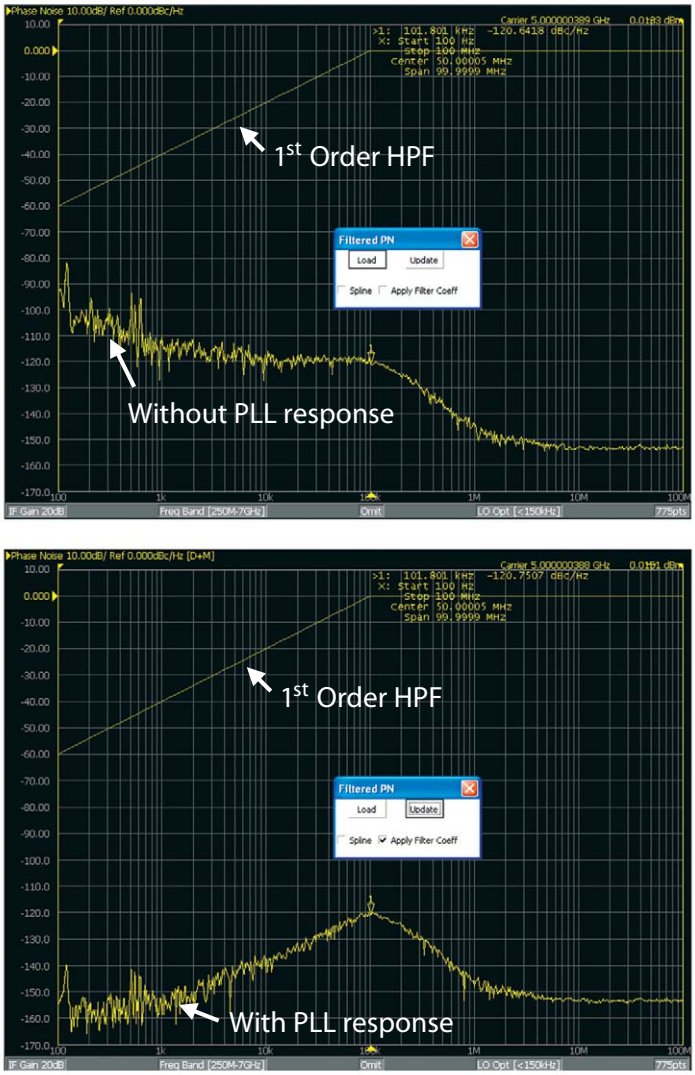

Figure 9. Emulation of the PLL response

Summary

For high-speed serial data applications the primary goal of clock-jitter analysis is to determine the effect that the jitter of the reference clock has on the bit error ratio of the system. The most accurate approach is to apply the transfer functions of the worst case transmitter (and receiver) for the application to the clock and measure the resulting clock RJ and PJ. E5001A precision clock jitter analysis software running on the E5052B SSA changes the traditional jitter measurement paradigm. It not only offers thorough analysis of your clock jitter with femto second resolution, but also improves ease-of-use and real-time jitter analysis helping you speed up the design verification process.

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