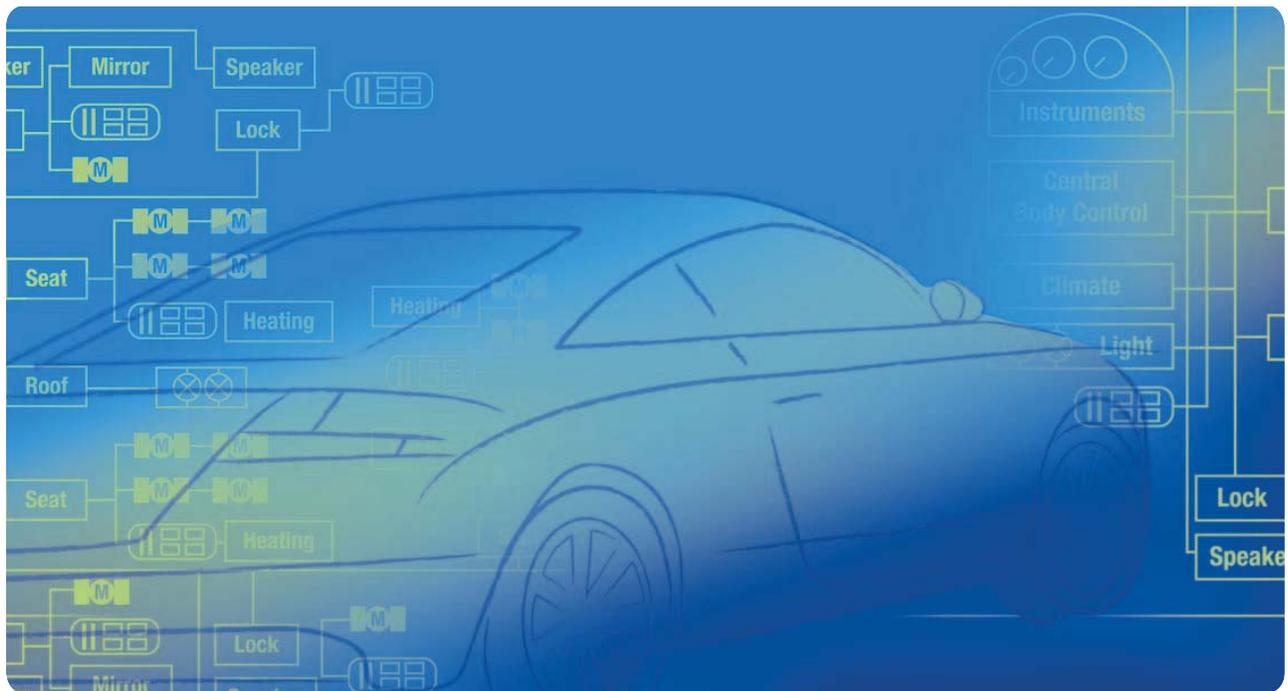# Evaluation Methods for Automotive Network Topologies

Signal integrity and bit error ratio depend on several issues within a network topology

Application Note
Version 1.0

Abstract

As the bandwidth of in-car networks increases, it is not enough to rely on certified bus controllers and just focus on the protocol layer and the application layer as defined in the OSI (Open Systems Interconnection) network layer model. This paper provides theoretical background for quantitative and qualitative methods to validate reliability of the physical layer of network topologies connecting Embedded Control Units (ECUs).

Motivation

Many electronic assistants in the car of the future will help the driver to have a full 360 degrees view: a technical challenge – especially for the networks, see [1]. Video, infrared and short range radars will support safe driving. The speed of the automotive networks will need to adopt speeds used to connect multimedia networks.

Definition of the Physical Layer

The physical layer is the first level of the seven levels in the OSI model (see [2]) of computer networks (see figure 1). It is also in the 4th or 5th layers of the TCP/IP reference model. The physical layer refers to network hardware and physical cabling. It deals with electrical specifications, collision control and other physical level functions.

The physical layer is responsible for transmitting the raw bits, while maximizing immunity against any errors. Another important issue is the generation and distribution of clocking signals.

Goals for successful data transmission

1. The transmitter (TX) provides a clean signal: sharp transitions and stable levels, minimum overshoot and ringing. This has to be provided into the load of the media.

2. The media will transport the TX signal without degradation. In reality some degradations always exist, which are limited and known.

3. The receiver (RX) understands the real-world degraded signal. This means the RX processes the incoming data correctly. For testing purposes we can verify the correctness of the received data at a certain point of the receiver output.

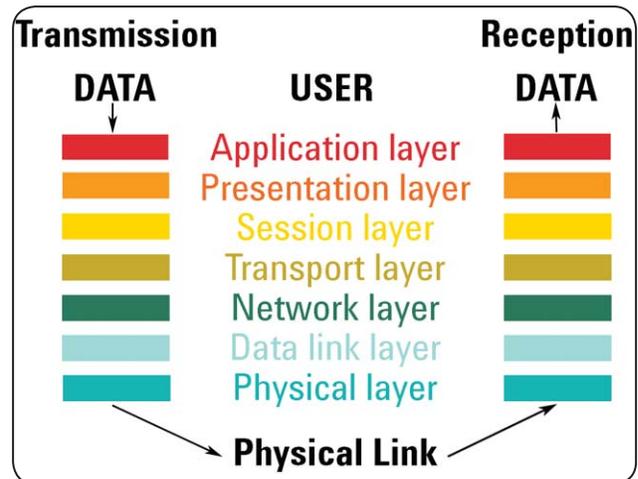The focus of this paper will be on issues 1 and 3. For more details on the second issue, see [3] and [4].
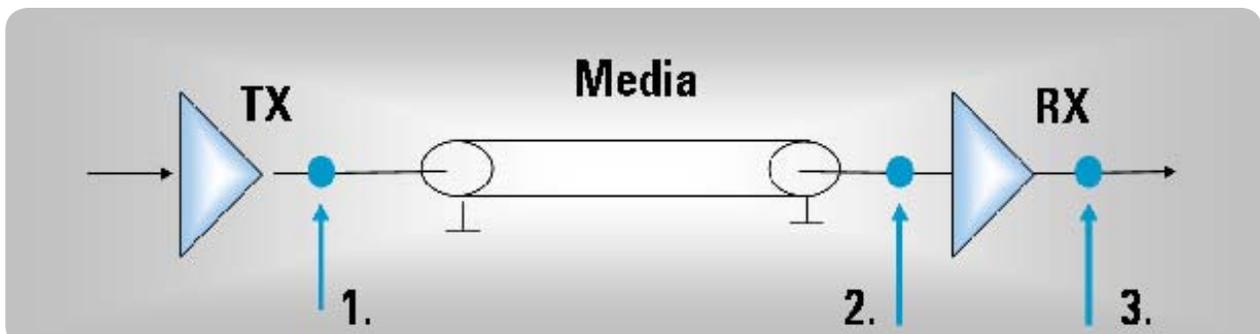

Figure 1: The OSI model

Figure 2: Simple transmission model

The Digital Signal

A digital signal consists of a stream of "0"s and "1"s, called bits. The scope view in figure 3 shows this as voltage over time. The bit content is represented as high (Vhigh) and low level (Vlow). The length of a single bit is measured in time and is called data rate, period or unit interval (UI).

A very important parameter of the digital signal is the transition time. It defines how fast the change from "0" to "1" (rise time) or "1" to "0" (fall time) occurs. The transition time is measured typically from 10% to 90% or from 20% to 80% of the voltage levels. A fast transition time makes the waveform rectangular.

Another view of a digital signal is the eye diagram, as shown in figure 4. The triggering is now on every bit. We obtain the overlay of all signal traces. The eye opening is specified in time and voltage.

The digital signal shown here in figures 3 to 5 has the following parameters: data rate = 10 Mb/s (period = 100 ns), Vlow = 0 V, Vhigh = 200 mV, tt = 3 ns. The pattern used is a PRBS 2^7-1.

Spectral view

Figure 5 provides a totally different view of a digital signal. The view displays frequency on the x axis and energy on the y axis.

The x axis' metric is the center frequency (in the middle) and the frequency span, which is the frequency increase per interval. The y axis is typically logarithmic; the unit here is dB.

A 10 Mb/s data signal has its fundamental frequency at 5 MHz. At 10 MHz and all even harmonics (k4 = 20 MHz, k6...) there is minimal energy. Maxima appear at the odd harmonics (k3 = 15 MHz, k5.., k7...) and extend to high frequencies. Faster transition times put more energy in the odd harmonics.
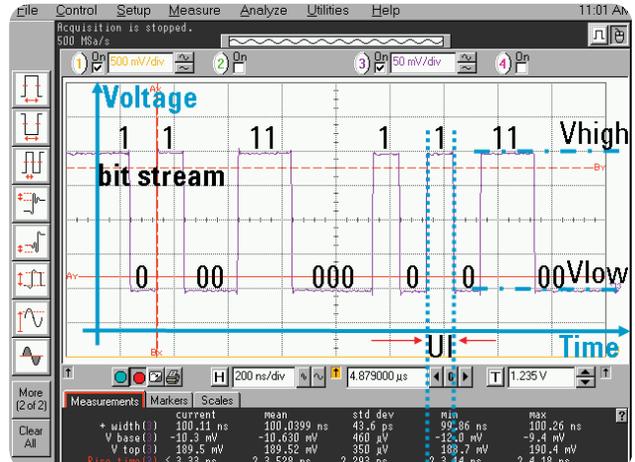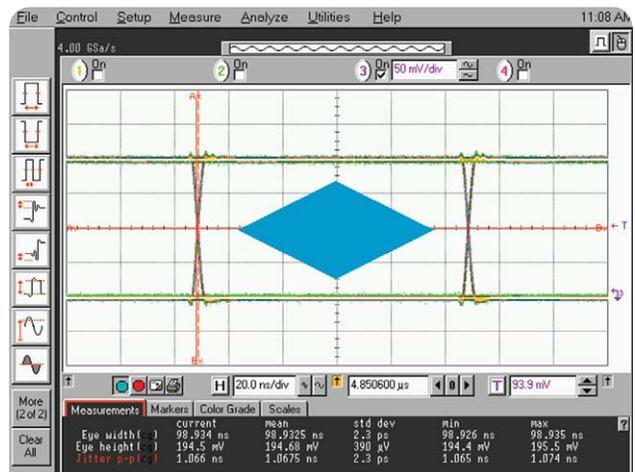

Figure 3: Digital signal (1): scope view

Figure 4: Digital signal (2): eye diagram. Eye opening in time, voltage and jitter - mask.
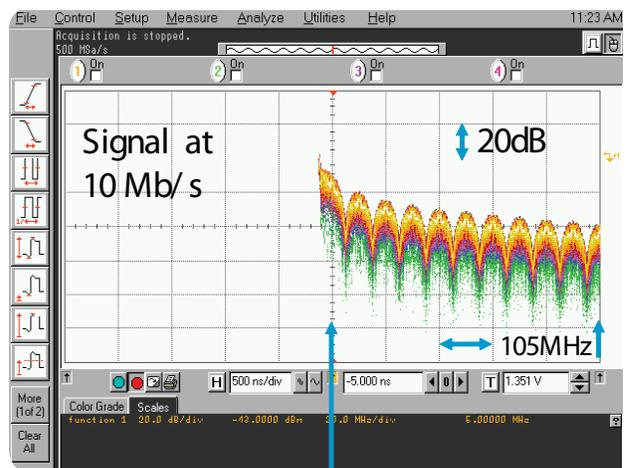

Figure 5: Digital signal (1): spectral view. Center frequency 5 MHz, span 20 MHz/div.
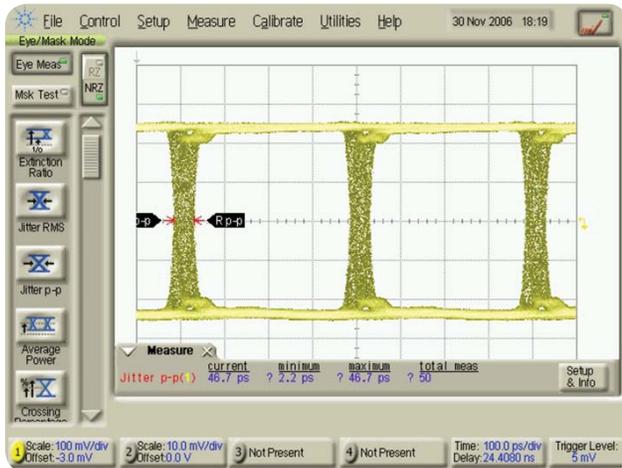
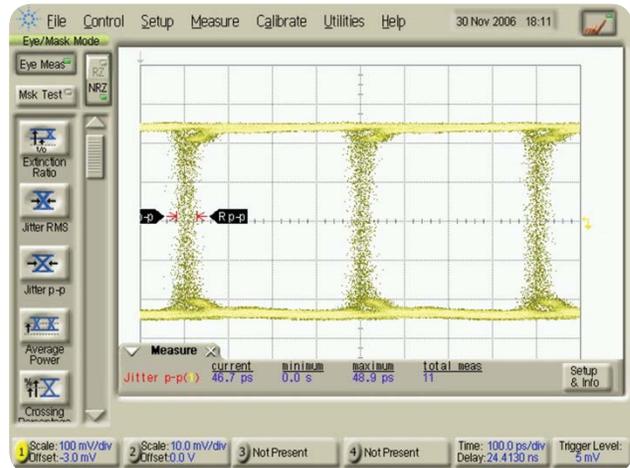Figure 6: Eye diagram of measurement with DJ. Jitter pp: 46.7 ps

Figure 7: Eye diagram of measurement with RJ, 11 samples taken. Jitter pp: 46.7 ps

The Eye Diagram as Quality Criteria

The eye diagram is a very valuable tool for judging signal integrity. We see the eye opening with time and voltage. All the eye closures are called jitter. In figures 6 to 8 we have two jitter scenarios. One is based on random jitter (RJ) and the other is based on deterministic jitter (DJ). Both include the same amount of jitter. The question is: which example would you prefer?

The difference between figure 7 and figure 8 is the measurement time. Allowing more time increases the amount of jitter. For the RJ example, the amount of DJ does not change. So we need a specification for the measurement time if we look for jitter in the eye diagram. Unfortunately, if we specify time, we depend on the tool, some scopes having faster sampling techniques than others. So the best choice is to specify how many bits are evaluated. This leads to the bit error ratio (BER) definition of the eye diagram (see figure 9).

BER is the real-time comparison of the received bits and the BER ratio is the number of errors divided by the total number of processed bits. The view in figure 8 provides double information: first, the chart shows measured data: in the dark grey area of the eye diagram the BER is greater than 1e-3 and in the wider light grey area the BER is larger than 1e-6 (lower BER figure -> more jitter peak-to-peak). Second, the chart provides extrapolated information for the eye openings at BER < 1e-6 depending on the selected options in the right part of the chart down to BER 1 e-15. The extrapolation is based on the algorithm of RJ/DJ separation.

Specifying eye diagrams based on a BER figure is the ultimate solution. This also helps defining error correction requirements.
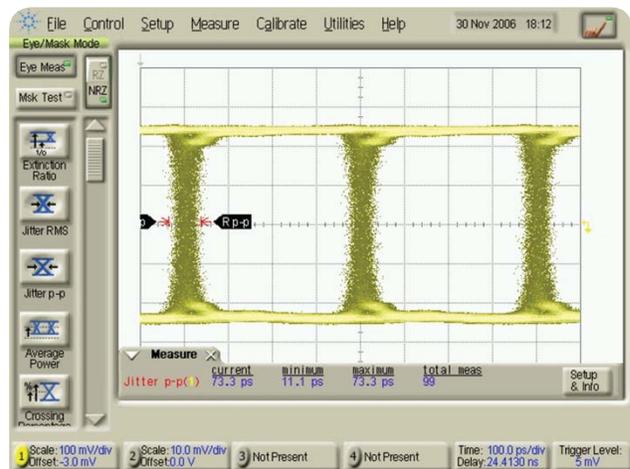

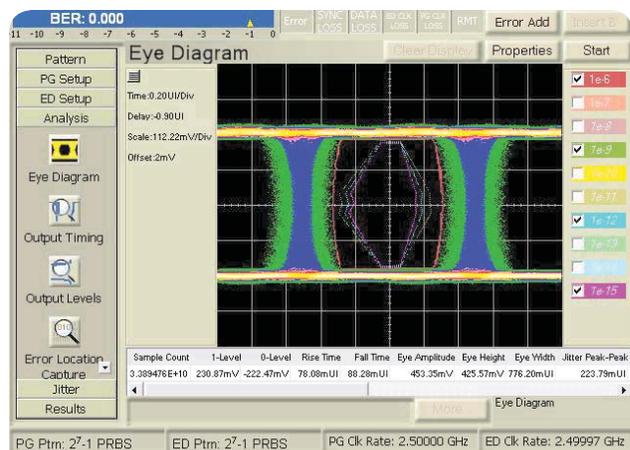Figure 8: Eye diagram of measurement with RJ, 99 samples taken. Jitter pp: 73.3 ps

Figure 9: Eye diagram based on the BER.

Evaluation Methods for Automotive Network Topologies Application Note

The Channel

Transmission line (TML)
Current, by definition, is the flow of charge. As current flows down a wire, the charge density at any point along the wire changes as a function of the current at that point in time. This charge density creates an electric field that radiates as a vector directly away from the wire.

When current flows, there is also a magnetic field that is generated around the wire. This magnetic field radiates away from the wire in a circular fashion. The combination of these two fields is what we call an electromagnetic field. Every time we have a current we have an electromagnetic field. We can not have a current flow without an electromagnetic field. And the three elements must track together. The magnetic field can not get out in front of or lag behind the electric field. The electrons can not get in front of or lag behind either field. All three must travel together, that is what we call a wave.

The bottom part of figure 10 shows electric and magnetic field lines for differential traces. There is a difference in coupling for traces far away (left) and close (right) to the underlying ground plane. Impedance is the generalization of the concept of resistance from DC to AC. It is a way to represent how much current will flow with a specified AC voltage across the impedance.

Signal propagation time is determined by how fast the electromagnetic field can travel in the medium it travels through.

Loss is a function of serial and parallel resistance as well as radiation by electromagnetic interference (EMI).

A terminated transmission line absorbs the electromagnetic wave at its end. The wave is converted back into AC voltage and current across the resistor. The energy stored in the wave is basically converted into heat.
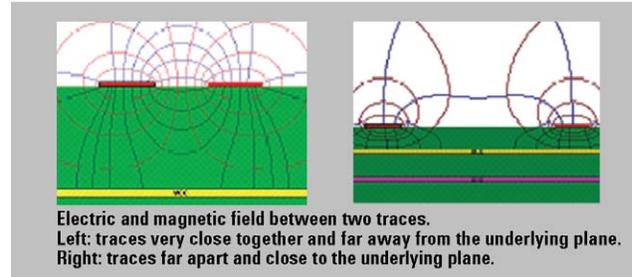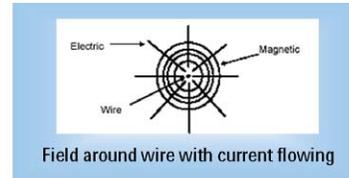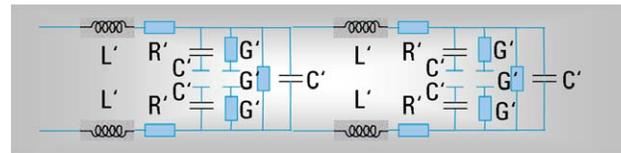

Field around wire with current flowing

Electric and magnetic field between two traces.
Left: traces very close together and far away from the underlying plane.
Right: traces far apart and close to the underlying plane.

Figure 10: TML and the electromagnetic field

$$Z_L = \sqrt{\frac{L'}{C'}}$$

$$\nu \approx \frac{1}{\sqrt{L'C'}} = \frac{1}{\sqrt{\epsilon_r \epsilon_o \mu_o}}$$

$$\text{Loss} = f(R', G')$$

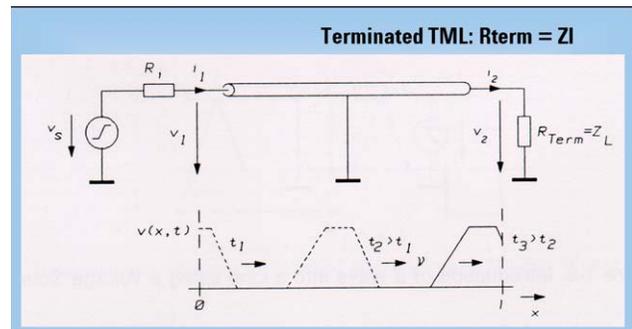Figure 11: Impedence, propagation delay and loss

Terminated TML: Rterm = Zl

Figure 12: Propagation of a wave with ideal termination at the end of the TML

Differential termination
Using a 100 Ohm resister across the differential lines is a good terminator for the differential data signal on the differential line, but this differential resistor does not provide termination for common mode signals. These are not necessarily generated by the transmitter (TX), but are coupled into the line by EMI. Common mode causes both lines to carry the same signal at the same time.

Theoretically, a receiver (RX) is not sensitive to these common mode signals as the differential signal is not affected by the common mode noise. In reality a RX has a limited common mode rejection and a problem might occur when the un-terminated common mode noise creates a standing wave with large amplitudes on the line.

The solution for reducing the common mode influence is shown in the lower part of figure 12: the 100 Ohm differential resistor is divided into 2 x 50 Ohm with the center tapping 25 Ohm resistor (Rs), resulting in a 50 Ohm termination for common mode signals.

Reflections
Impedance mismatch by inhomogeneous media or discrete parasitic elements (L, C) causes reflections (see figure 13). The traveling wave is split into a forwarding and back-warding part. The back-warding part is an energy loss of the original wave. The signal integrity is affected when two or more mismatching points occur within a TML system.

Network topology with stubs
A network topology with stubs inherently suffers from signal integrity problems caused by reflections (see figure 14). The following experiments provide some more details.
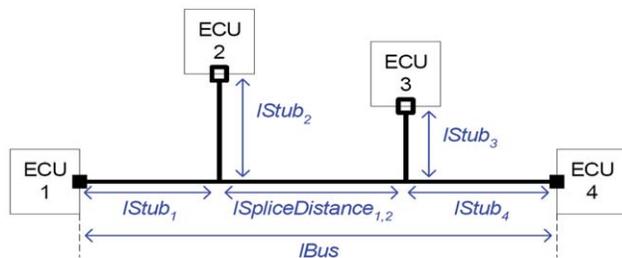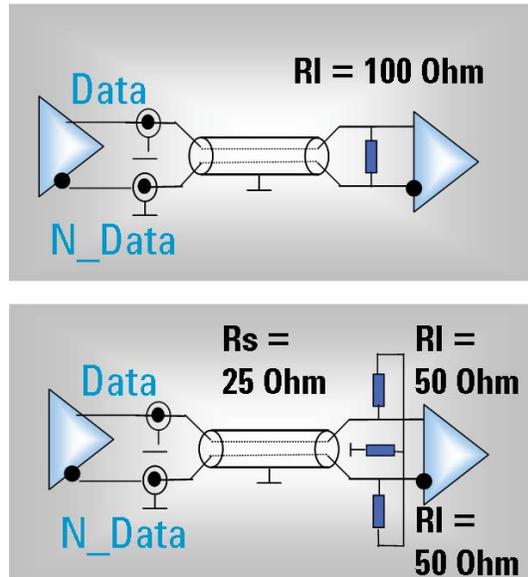

Figure 13: Differential termination w/o (top) and with common mode reduction (bottom)
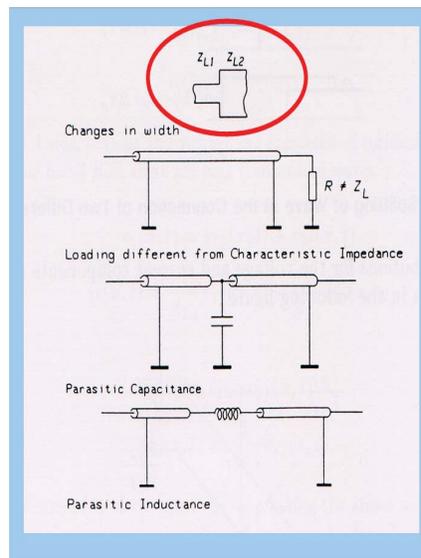
Figure 14: Reflections by impedance discontinuities and discrete parasitics

Figure 15: Network topology with stubs, see [1]

Experiments

The experiments are performed with the help of a pattern generator and an oscilloscope (see figure 16). The pattern generator provides data at 10 Mb/s either differentially or by two channels in normal and complement mode. The scope needs a minimum of two inputs with a 50 Ohm termination. This ensures proper termination for both ends of the test device.

The device-under-test (DUT) is a twisted ribbon cable with multiple pairs. The cable's total length is 12 m, the bus length of 24 m is emulated by injecting the signal into one pair and then returning the signal on another pair. The cable provides flat sections where it is easy to crimp connectors into the cable. This allows the connection of stubs at 3 m from both ends of the cable. The stubs are made by a twisted pair cable attached to plugs fitted into the crimp connectors. The cable length of the stubs is 1 m if not otherwise noted. All stub cables have an open end, except one which is prepared to attach a high impedance scope probe. Thus a measurement at the unterminated end of a stub is possible.

Experiments at 10 Mb/s
Figure 17 shows the reference measurement. This is the pattern generator output connected with standard coaxial cables to the scope. The coaxial cables do not affect the signal integrity. The eye opening is at 100% and the transition time is 3 ns (measured from 10% to 90%).

Figure 18 shows the measurement of the signal at the terminated cable end. The signal shows a degradation as the transition becomes round. Another name for this rounding is a droop. The droop slows down the transition time to roughly 27 ns (measured from 10% to 90%).

Fortunately the signal settles mostly at 100% within the data cycle of 100 ns and the eye opening is at 98.5%.

The droop can be explained by the loss in the cable. The loss is frequency dependent, as the higher the frequency is, the more attenuation occurs. This corresponds to the spectral view of figure 5, page 3.
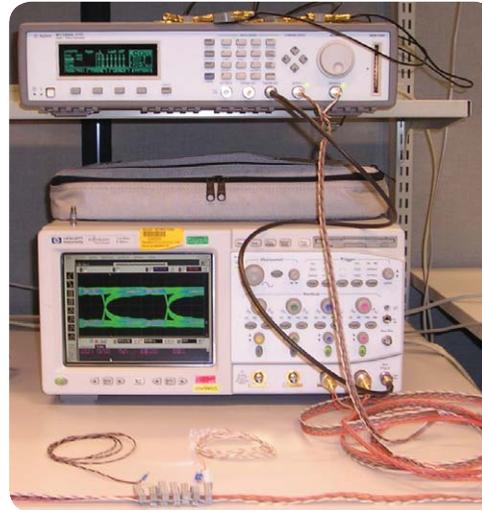

Figure 16: Setup for the experiments: pulse pattern generator and scope real-time/sampling, 24 m twisted pair ribbon cable with up to 7 possible stubs 3 m/21 m.
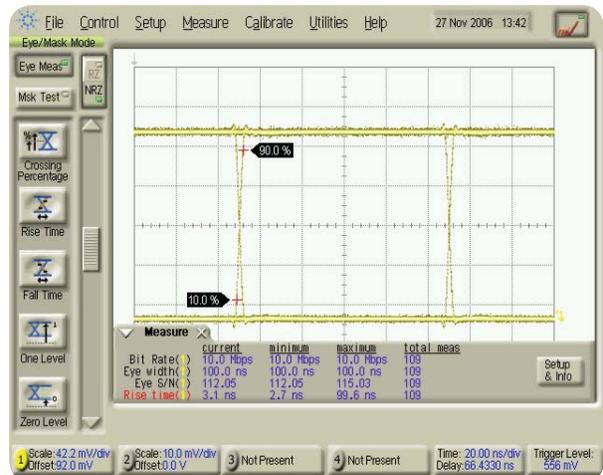

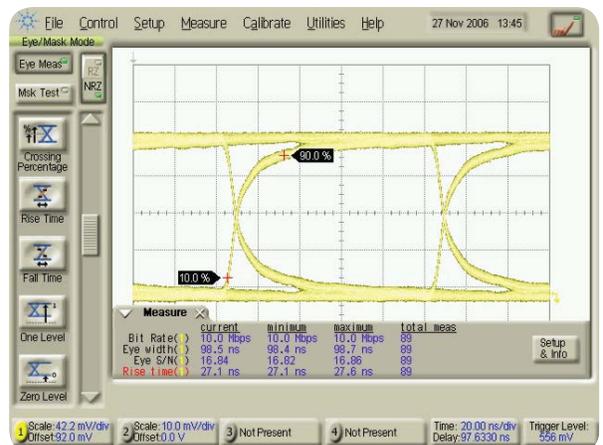Figure 17: Reference measurement 10 Mb/s

Figure 18: Signal measurement at the terminated cable output 10 Mb/s, no stub

Next step is to add stubs. In figure 19 one stub is added, in figure 20 six stubs are added. Both figures provide the signal measurement at the terminated end of the cable. Figure 21 shows the measurement for the six stubs scenario at the end of the un-terminated stub.

A stub causes the electromagnetic wave to split into three parts: one part travels back to the source, one part runs into the stub and one part continues to travel along the cable. As in the un-terminated stub, the wave is returned after a while and the signal at the end consists of the initial wave and multiple reflection from the stub. This causes the degradation of the transition time as well as the settling in steps. In case of multiple stubs the signal looks like there is more droop/loss.

Worse can be the signal at the end of the stub: here it needs multiple reflections to obtain the settling of the signal. The waveform measured depends heavily on the arrangement of the stubs, the example in figure 21 is one of the worst found.

As a short summary, the results show that the stubbed network topology is feasible at 10 Mb/s, but what is highly recommended is to check the signal integrity carefully at each node, especially the un-terminated ones.
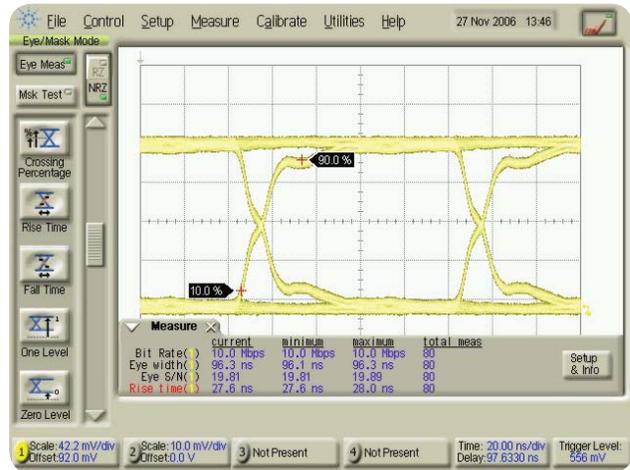

Figure 19: Signal measurement at 10 Mb/s with one 1 m stub, measured at the terminated end of the cable.
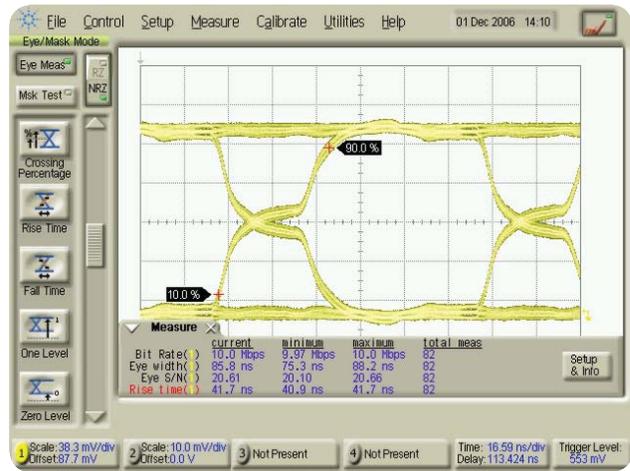

Figure 20: Signal measurement at 10 Mb/s with six 1 m stubs, measured at the terminated end of the cable.

Figure 21: Signal measurement at 10 Mb/s with six 1m stubs, measured at the un-terminated end of a stub.

Evaluation Methods for Automotive Network Topologies Application Note

Experiments at 50 Mb/s

The experiments at 50 Mb/s use the same setup as shown in figure 15, except that the pattern generator provides the data signal at the given rate and that the scope has sufficient bandwidth.

Figure 22 shows the reference measurement. The transition time of 3 ns provided by the pattern generator makes the signal look like an eye. The eye is clean and fast enough for the experiments to be completed.

Figure 23 shows the 50 Mb/s data signal at the terminated end of the cable without any stubs. Now the losses are much more obvious. No more will the droop allow a signal to settle at 100%. The edge for the following data cycle is started earlier if there is a transition at the beginning of the data cycle. This causes edge displacement and we call this jitter. It is data content dependent jitter and this type of jitter is called intersymbol interference (ISI).

Figures 24 and 25 compare a spectral view of the reference signal (left) and the signal at the end of the terminated cable (right). We compare the magnitude of the ninth harmonic in reference to the fundamental frequency: at the end of the cable it is 6.2 dB lower than in the reference. A similar attenuation applies to all harmonics, of course.

The ISI in the cable (see figure 23) causes a jitter of 2.5 ns, which corresponds to 12.5% of the unit interval. This can be too much to be neglected in a system.
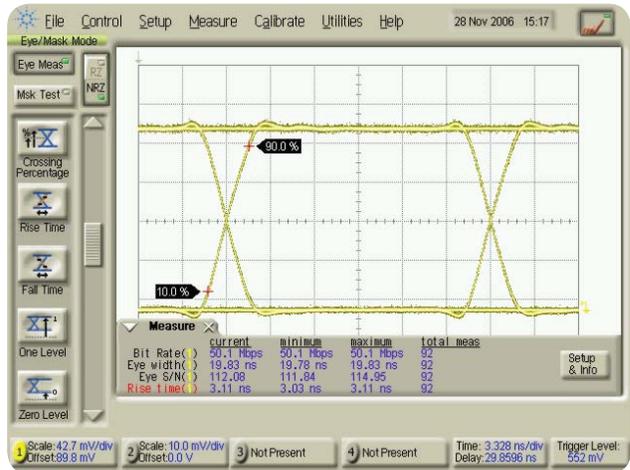

Figure 22: Reference measurement at 50 Mb/s
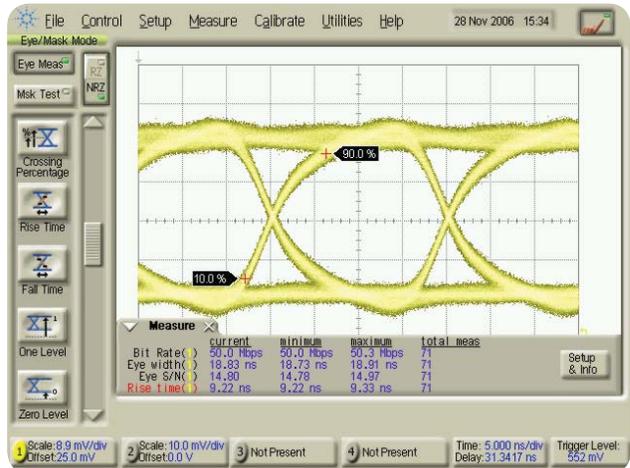

Figure 23: Measurement at 50 Mb/s at the terminated cable end
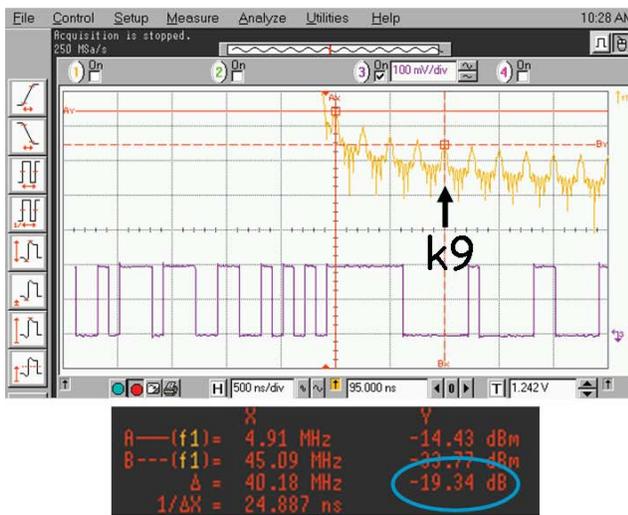

Figure 24: Spectral view of the reference signal

Figure 25: Spectral view of the signal at the end of the cable, the harmonic K9 is reduced by 6.2 dB.

There is a method of compensating these losses by creating a de-emphasized signal as shown in figure 26. The de-emphasized signal adds a post cursor to the main data signal. We obtain a signal with four levels. The de-emphasized signal has a higher amplitude (16 dB) after a data transition and the amplitude is reduced when no transition occurs at the next data cycle. This compensates for the ISI as can be seen in figure 27: the eye opens from 17.5 ns to 19 ns and the transition time improves from 16 ns to 9 ns (compared to the results from figure 23).

Now we add stubs: figure 28 shows the signal at the terminated end of the cable after adding 6 stubs. This is the same setup as used for figure 20, but at a higher speed. The reflections close the eye totally and there is no way to reverse this again.

Following are the conclusions from the measurements at 50 Mb/s:
• The loss of the media cannot be neglected anymore, therefore a compensation method is needed.
• A terminated environment becomes a must. Unterminated stubs cannot be used anymore, the reflections can no longer be tolerated.
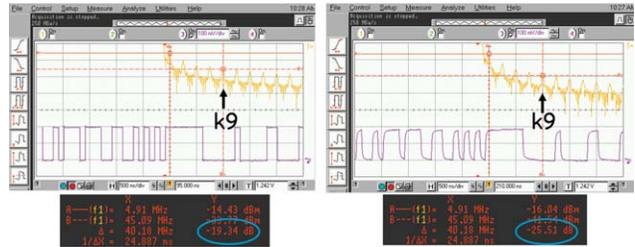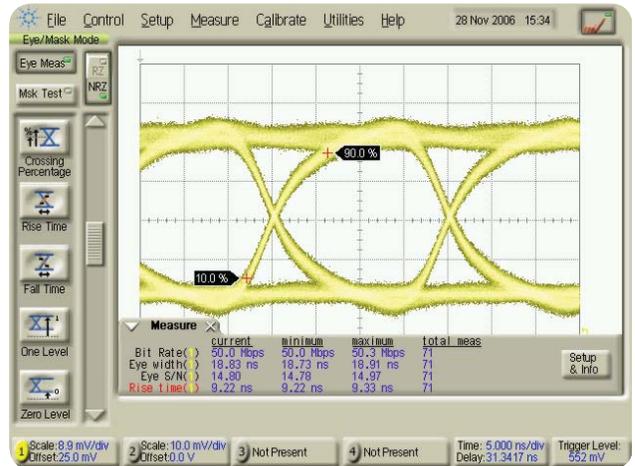

Figure 26: De-emphasized signal (16 dB)

Figure 27: Signal measurement at 50 Mb/s at end of cable with de-emphasized signal applied

Figure 28: Signal measurement at 50 Mb/s at terminated end of cable with 6 stubs added

What is Jitter?

Jitter components

This is the complete picture of the jitter components: total jitter consists of random and deterministic jitter.

RJ is statistical, so it is unbounded. It can be modeled by the Gaussian distribution with the rms value. The longer you wait the wider it becomes (see figure 7, 8 and 30). RJ is caused by thermal effects.

The next layer separates the deterministic jitter (DJ):
- Periodic jitter (PJ) displaces the timing of rising and falling edges with a periodic pattern. As the origin of this type of jitter is sinusoidal modulation, it is also called SJ (see figure 31).
- Data dependent jitter (DDJ) is correlated to the bit patterns.
- Bounded uncorrelated jitter BUJ is caused by interference with asynchronous signals: crosstalk between sub-circuits, power supply noise and electro-magnetic interference (EMI).

The DDJ can be separated into:
- Duty cycle distortion (DCD), caused by voltage offsets between differential inputs and differences between transition times within a system.
- Intersymbol interference (ISI), caused by the different symbols (long and short bit cycles). This can be explained by bandwidth limitations which occur from AC coupling (low frequency cut-off) or from high frequency roll-off (but this is from filters with non-linear phase characteristic only, linear filters, like Bessel filters, do not cause jitter).

DCD and ISI jitter are bit pattern dependent. The jitter appears when changing the pattern from a clock-like pattern to real data. PRBS type patterns are good for testing as they contain many frequency components.
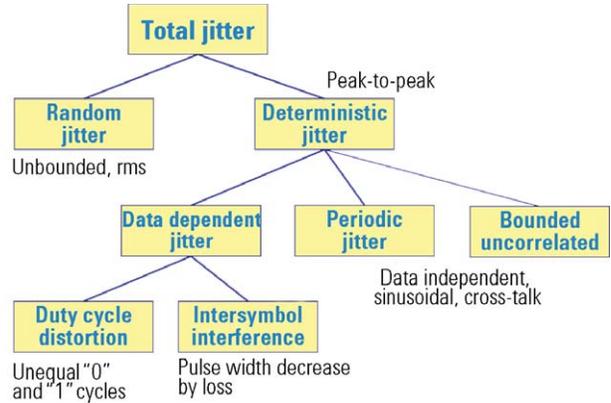

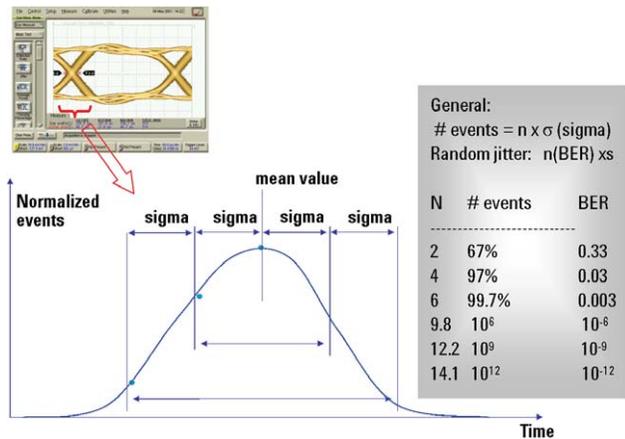Figure 29: Jitter separation model
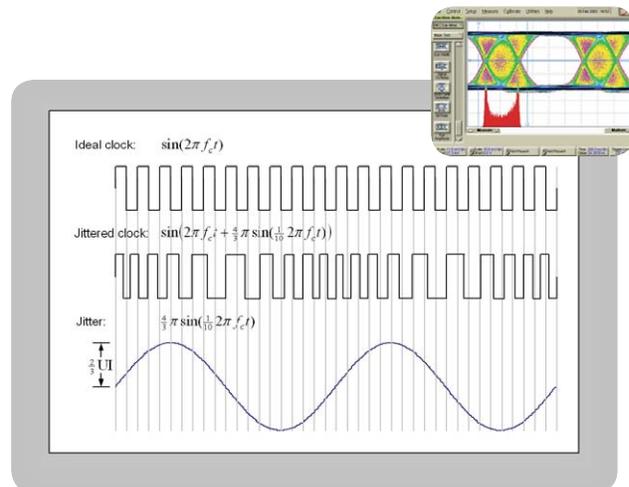

Figure 30: Random jitter (RJ)

Figure 31: Periodic/sinuosidal jitter (SJ/PJ)

The role of a CDR

A clock data recovery (CDR) is a building block which extracts a clock signal embedded into a data signal. This eliminates the need of routing a clock signal between two devices. But there is a second - much more important - issue: the CDR reduces jitter (see figure 33).

At low frequencies a CDR can track any jitter. The tracking means receiving the recovered clock in phase to the data. The sampling occurs at the sweet spot of the eye and with a high probability of no bit error. Above the cut-off frequency, the CDR cannot follow the jitter frequency, the tracking decreases and so the high frequency jitter components cause a closing of the eye. Designers have to worry about the high frequency jitter components.

A test system should behave similarly. Jitter measurements based on a reference clock may deliver wrong results, as the low frequency jitter components are included. So the better results (better = lower figure and truer value) are achieved using a CDR (see figure 33).

The generation of calibrated jitter

The various jitter components can be generated in several different ways (see figure 34):
- Clock jitter is created by sinusoidal clock modulation (PJ/SJ).
- High frequency periodic jitter (PJ) is created by edge modulation with help of the delay line.
- Random jitter (RJ) is created with the help of the delay line driven by a noise source.
- Common/differential mode noise (DM/CM crosstalk) is created by adding a sinusoidal signal to the data lines.
- ISI jitter is created by switching filters consisting of "lossy" delay lines.
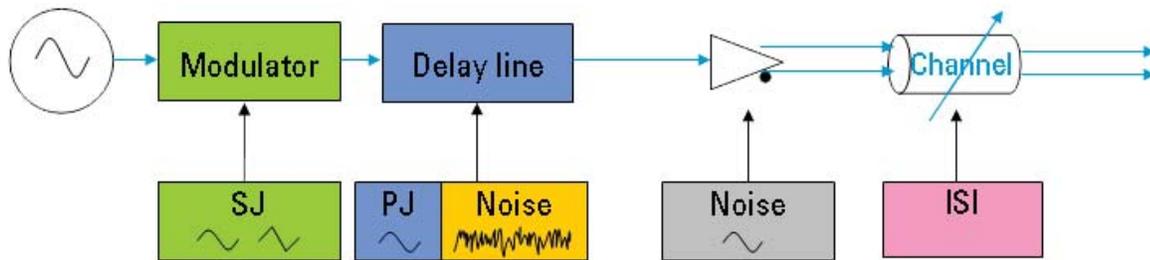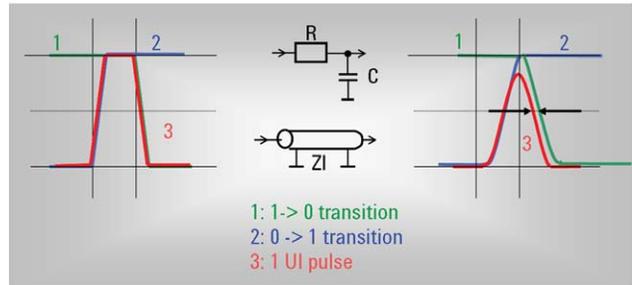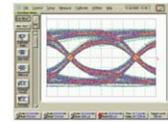

Figure 32: Intersymbol interference (ISI)

Figure 33: Importance of the CDR for jitter reduction
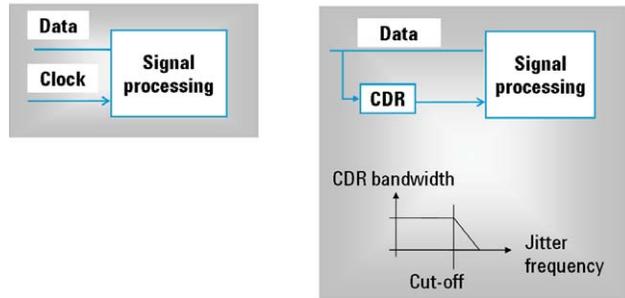

Figure 34: Generation of calibrated jitter

RX Test

Traditionally the RX test was traded: when the RX, supplied with a reasonable TX signal, performed properly, the RX was believed to operate fine. A pragmatic but probably dangerous approach!

Figure 35 details the RX input architecture.
The building blocks of an RX input and their typical sensitivity to jitter are:
• Eye opening filter -> ISI
• Limiting amplifier -> pulse width
• Sampler -> duty cycle variation, high
          frequency PJ
• CDR -> pattern dependency

Receivers must tolerate degraded signals. Impaired data streams are needed to verify the receiver's robustness. Calibrated composition of various types of jitter (RJ, PJ, BUJ, ISI, SI) create real-world stress conditions. This is not all.

For receiver testing we need to consider three more requirements:
• Stimulate a known bit pattern
• Access a point to loop-back the received bits
• Compare the stimulated and the received pattern bit by bit and count the non-matching bits (error count)

For loop-back two scenarios are possible (see figure 37):
• Near-end: this is close to the output of the sampling circuit
• Far-end: this is further down in the circuit and may include the buffering

The further down in the circuit the loop-back point is implemented, the more testability issues have to be considered. Including the buffering requires a mechanism to switch between the clocks to suppress clock speed tolerances.

For the characterization of the RX input, the near-end loop-back is optimal. But this is only usable on a test bench.
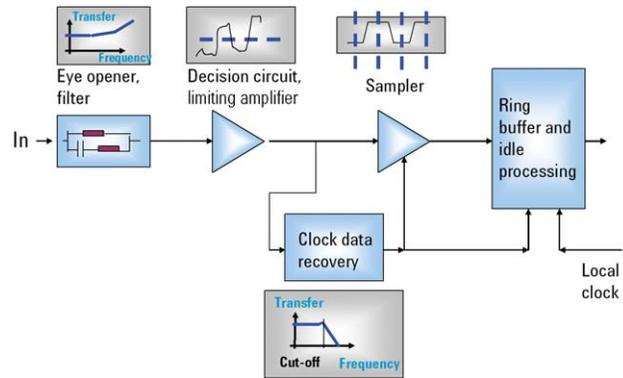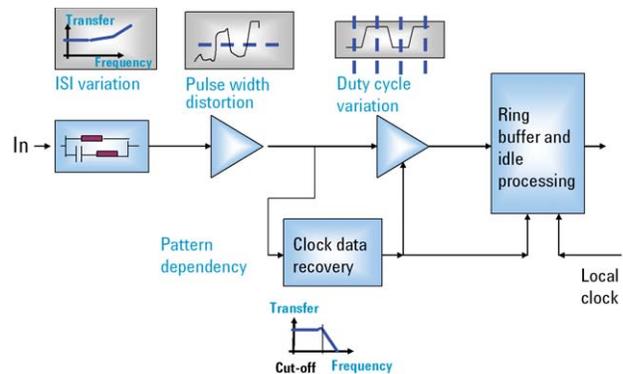

Figure 35: RX input architecture
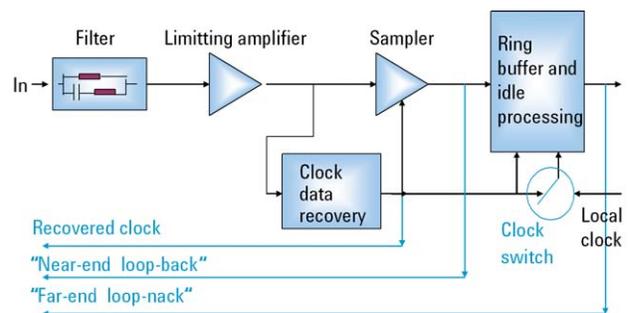

Figure 36: RX sensitivity to jitter

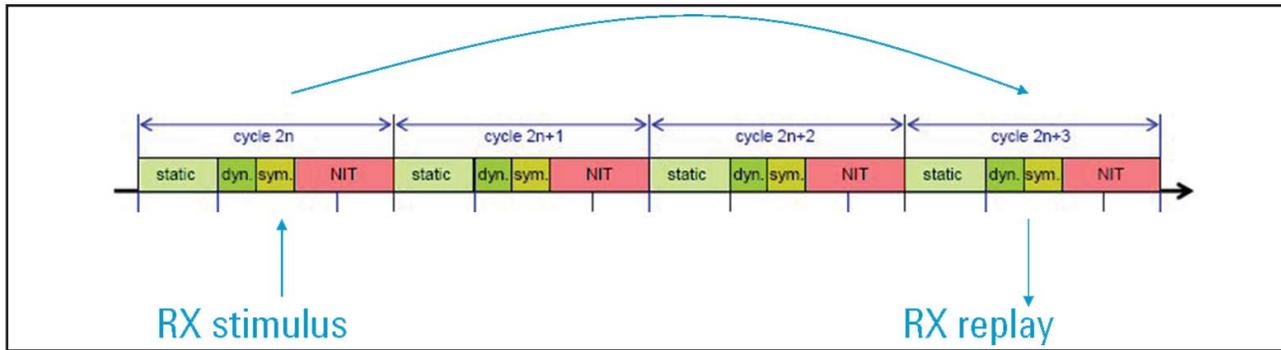Figure 37: Recommendations for loop-back

Figure 38: Recommendation for a dedicated RX-replay slot in the TDMA environment

In the TDMA environment a loop-back becomes complicated. A possible solution could be a concept with a RX replay slot, as shown in figure 38. Under normal operation this slot is optional. [5] When a receiver is configured into loop-back, it will replay its stimulus during this slot. This allows the examination of the replayed data with external equipment as well as with the built-in-self test (BIST) method. BIST adds circuits to the chip which provide stimulus pattern generation as well as pattern checking for at least the functional verification of the building blocks put together in a system.

As a consequence, the RX test can be more cost and time efficient, if we choose a hierarchical approach (see table 1):
• The characterization (variable stress) is performed on the test bench at the chip level. All kind of controlled stress can be applied to the input, using loop-back.
• A conformance test is performed in the actual system. With help of a golden TX we apply the worst case signal to the RX input point. The golden TX needs to be calibrated in a golden system with help of the characterization equipment.
• A functional test is done in the system with help of BIST at specific operating conditions, e.g. power-up or diagnosis request. A positive consequence: a manufacturing test can be achieved very efficiently with help of the BIST hardware.

Figure 39 outlines the setup on the test bench using the RX in loop-back and the equipment generating all kind of stress signals, and analyzing the received bits. Based on the BER, the RX performance can be characterized. (The TX performance can also be evaluated with the same equipment, saving investment). [6]

Table 1: Hierarchical RX test

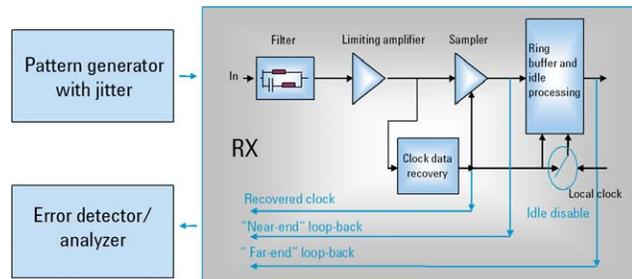|	Characterization	Conformance	Functional Test
Test Signals	All kind of stress	Golden TX	BIST
Environment	Bench test	System calibrated in reference system	System
Equipment	BERT and scope	Scope	Master unit

Figure 39: RX characterization at the test bench

A Brief View in the "World of Standards"

1. Ethernet: 1 Mb/s, 10 Mb/s, 100 Mb/s, 1 Gb/s, 10 Gb/s
   - at 1 Mb/s stubbed ring
   - from 10 Mb/s duplex point-to-point connection

2. PCIe: 2.5 Gb/s, -> 5 Gb/s
   - Multiple duplex point-to point connections
   - Very detailed RX test scenario for jitter conditioning

3. PON: passive optical network (10 Mb/s) 155 Mb/s to 2.5 Gb/s
   - TDMA with passive optical splitter 1:32
   - Single fiber with bi-directional traffic
   - Rough guard time calibration, frame format allows collision
   - Collision phase for CDR alignment

Measurement Tools for the Physical Layer

Signal integrity TX and media:
- Pattern generator, AWG and scope

Signal integrity RX:
- Bit error ratio tester (BERT), logic analyzer, loop-back, BIST

Media /transmission line, impedance and loss:
- TDR: time domain reflectometry (T-Parameter)
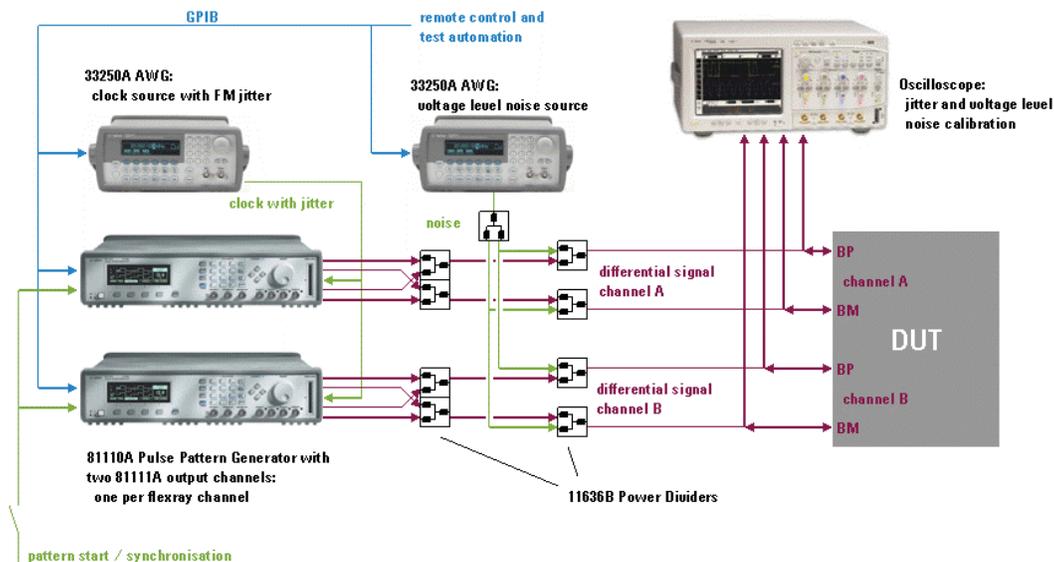- Network analyzer (frequency domain, S-Parameter) [7]

Outline for the RX Stress Test based on Today's Equipment (w/o loop-back)

RX stress test applies the stress signal to the FlexRay and detects whether the receiver is able to read the signal properly. This involves sending a known pattern to the FlexRay receiver to compare it with the received results:
- Injecting jitter creates horizontal closure of the eye
- Reducing the amplitude closes the eye vertically
- Adding noise closes the eye further

The data pattern to be used depends mainly on the DUT. Physical layer testing should not use a pattern that complies with the protocol. Industry standard stress patterns, such as PRBS or CJTPAT should be considered. If a DUT can only handle the FlexRay protocol, the pattern generators provide memory to load a framed pattern. [8]

Figure 40: RX stress test outline

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[1] FlexRay Communications System, Electrical Physical Layer Specification, Version 2.1, Revision A
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[4] Flexray—A Standard becomes Reality, Lutz Leutelt, Philips Semiconductors, Paper on Convergence 2006
[5] FlexRay—Exploitation as a Standard and Future Prospects, Josef Berwanger, BMW, paper on Convergence 2006
[6] Determination of Bit Error Rates for CAN and FlexRay under electromagnetic Interference, Wolfgang Mickisch, TÜV Nord, paper on FlexRay Product Day, 30. November 2006, Böblingen
[7] Steckverbinder-Systeme für Flexray-Netzwerke, ATZ 11/2006
[8] Agilent Technologies, Application Outline 5989-5834EN: Receiver Stress Test for Flexray Devices Using the Agilent 81110A Pulse Pattern Generator

Related Literature   Pub. No.

Options for Automotive Applications   **5989-6220EN**
Using Agilent's 6000 Series Oscilloscopes
Data Sheet

Agilent Automotive Electronics: 10 Applications Notes   **5989-6283EN**
on Design Debug and Fundctional Test

Test & Measurement for Automotive Electronics   **5989-6236EEE**
Product Selection Guide

Receiver Sterss Test for Flexray Devices Using   **5989-5834EN**
the Agilent 81110A Pulse Pattern Generator
Application Note

> **www.agilent.com/find/automotive-test**

> **www.agilent.com/find/BERT**

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